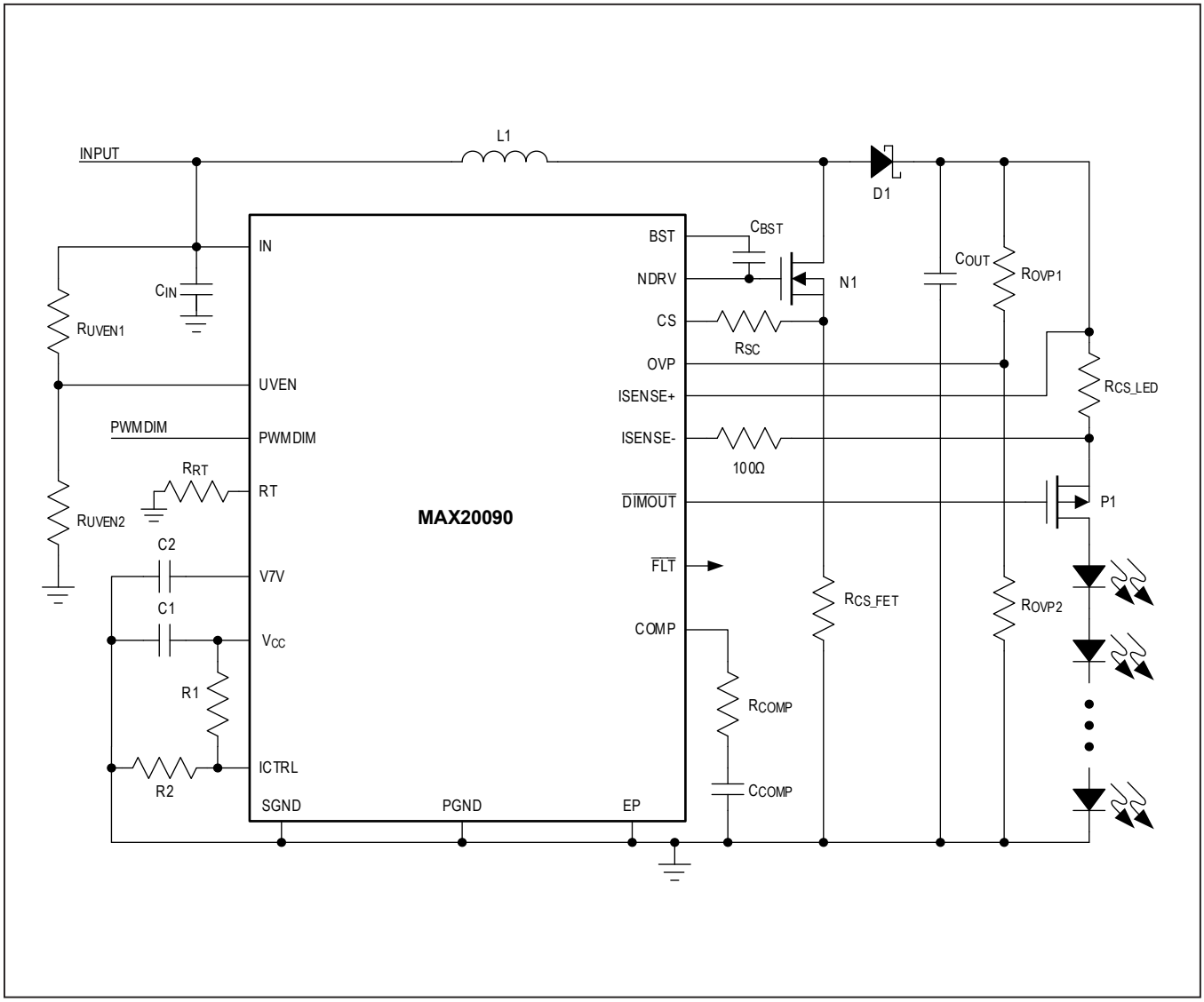
Simplified Schematic



Absolute Maximum Ratings

IN to PGND .....-0.3V to +70V
ISENSE+, ISENSE-, $\overline{DIMOUT}$ to PGND .....-0.3V to +70V
$\overline{DIMOUT}$ to ISENSE+ .....-8.5V to +0.3V
ISENSE- to ISENSE+ .....-0.3V to +0.3V
PGND to SGND .....-0.6V to +0.3V
V_{CC}, UVEN to PGND .....-0.3V to +6V
V7V to PGND .....-0.3V to +9V
BST to PGND .....-0.3V to V7V + 5V
BST to NDRV .....-0.3V to +6V
NDRV to PGND .....-0.3V to +7.3V
OVP, PWMDIM, ICTRL, $\overline{FLT}$ to PGND .....-0.3V to +6V
COMP, RT, CS to PGND .....-0.3V to +V_{CC}
Continuous Current on IN 100mA
Peak Current on NDRV .....+2A
Continuous Current on NDRV .....+50mA
Continuous Power Dissipation (T_A = +70°C) (Note 1)
20-pin TSSOP
(derate 26.1mW/°C above +70°C) .....2089 mW
20-pin TQFN
(derate 25.6mW/°C above +70°C) 2051mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....37°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....2°C/W

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....33°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

V_{IN} = 12V, R_{RT} = 85.4kΩ, C_{IN} = C_{VCC} = 1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
Input Voltage Range	V_{IN}		5.0		65	V
Supply Current	I_{INQ}	V_{OVP} = 1.5V, no switching		1.8	5.0	mA
UNDERVOLTAGE LOCKOUT						
Undervoltage-Lockout Rising	V_{UVEN_THUP}	V_{UVEN} rising	1.12	1.24	1.37	V
Hysteresis				106		mV
Shutdown Current	I_{SHTDN}	V_{UVEN} = 0V, V_{IN} = 12V		15	26	µA
V_{CC} REGULATOR						
Output Voltage	V_{CC}	Load 0.1mA to 15mA, 6.0V < V_{IN} < 16V	4.875	5	5.125	V
Dropout Voltage	$V_{CC\ DROP}$	V_{IN} = 4.5V, I_{VCC} = 5mA		0.07	0.16	V
V_{CC} UVLO Rising	$V_{CC\ UVLOR}$	Rising		4.0		V
Hysteresis				0.4		V

Electrical Characteristics (continued)

V_{IN} = 12V, R_{RT} = 85.4kΩ, C_{IN} = C_{VCC} = 1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V7V REGULATOR						
Output Voltage	V7V	0.1mA ≤ I_{VCC} ≤ 50mA, 9V ≤ V_{IN} ≤ 12V	6.72	7.0	7.28	V
		12V ≤ V_{IN} ≤ 65V, I_{VCC} = 10mA	6.72	7.0	7.28	
Dropout Voltage	$V7V_{DROPOUT}$	V_{IN} = 5.0V, I_{V7V} = 50mA		0.175	0.42	V
V7V UVLO Rising	$V7V_{UVLO\_R}$	Rising		4.33	4.7	V
Hysteresis				0.36		V
Short-Circuit Current Limit	I_{V7VSC}	V_{7V} shorted to GND, V_{IN} = 5V	55			mA
BOOTSTRAP SUPPLY						
BST Input Current	I_{BST_OFF}			0.02		mA
OSCILLATOR (RT)						
Switching-Frequency Range	f_{SW}		200		2200	kHz
Bias Voltage at RT	V_{RT}			1.25		V
Minimum Off-Time	t_{OFF_MIN}	V_{COMP} = high, V_{CS} = 0V		85		ns
Oscillator Frequency Accuracy		Dither disabled	-10		+10	%
Frequency Dither	f_{DITH}	Dither enabled, f_{SW} = 200kHz to 2.2MHz		±6		%
SLOPE COMPENSATION						
Slope-Compensation Current-Ramp Height	I_{SLOPE}	Peak current ramp added to CS input per switching cycle	42.5	50	57.5	µA
ANALOG DIMMING						
ICTRL Input Control-Voltage Range	$ICTRL_{RNG}$		0.2		1.2	V
ICTRL Zero-Current Threshold	$ICTRL_{ZC\_VTH}$	($V_{ISENSE+}$ - $V_{ISENSE-}$) < 5mV	0.16	0.18	0.200	V
ICTRL Clamp Voltage	ICTRLCLMP	ICTRL sink = 1µA	1.25	1.30	1.35	V
ICTRL Input Bias Current	$ICTRLI_{IN}$	V_{ICTRL} = 0 to 5.5V		20	500	nA
LED CURRENT-SENSE AMPLIFIER						
Common-Mode Input Range			-0.2		+65	V
Differential Signal Range			0		225	mV
$I_{SENSE+/-}$ Input Bias Current	$IB_{ISENSE+}$	$V_{ISENSE+}$ - $V_{ISENSE-}$ = 200mV, $V_{ISENSE+}$ = 60V		350	550	µA
	$IB_{ISENSE-}$	$V_{ISENSE+}$ - $V_{ISENSE-}$ = 200mV, $V_{ISENSE+}$ = 60V		22	60	
Input Offset Voltage		T_J = +25°C, $V_{ISENSE+}$, $V_{ISENSE-}$ = 3V to 60V		-0.1		mV
		3V < $V_{ISENSE+}$, $V_{ISENSE-}$ < 60V		-0.1		

Electrical Characteristics (continued)

V_{IN} = 12V, R_{RT} = 85.4kΩ, C_{IN} = C_{VCC} = 1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain		($V_{ISENSE+}$ - $V_{ISENSE-}$) = 200mV, 3V < $V_{ISENSE+}$, $V_{ISENSE-}$ < 60V	4.90	5.0	5.1	V/V
LED Current-Sense Regulation Voltage	V_{SENSE}	V_{ICTRL} = 1.3V, 3V < ($V_{ISENSE+}$, $V_{ISENSE-}$) < 60V	213.8	220	226.2	mV
		V_{ICTRL} = 1.2V, 3V < ($V_{ISENSE+}$, $V_{ISENSE-}$) < 60V	194.0	200	206.0	
		V_{ICTRL} = 0.4V, 3V < ($V_{ISENSE+}$, $V_{ISENSE-}$) < 60V	37.0	40	43.0	
LED Current-Sense Regulation Voltage (Low Range)		V_{ICTRL} = 1.2V, 0V < ($V_{ISENSE+}$, $V_{ISENSE-}$) < 3V	192	200	208	mV
		V_{ICTRL} = 0.4V, 0V < ($V_{ISENSE+}$, $V_{ISENSE-}$) < 3V	35	40	45	
Common-Mode Input Range Selector	RNG_{SEL}	$V_{ISENSE+}$ rising	2.72	2.85	2.98	V
		$V_{ISENSE+}$ falling	2.48	2.6	2.72	
ERROR AMP						
Transconductance	g_M	$V_{ISENSE+}$ - $V_{ISENSE-}$ = 200mV	1170	1800	2430	µS
COMP Sink Current	$COMPI_{SINK}$	V_{COMP} = 5V		300		µA
COMP Source Current	$COMP_{ISRC}$	V_{COMP} = 0V		300		µA
PWM COMPARATOR						
Input Offset Voltage				1		V
PWM-to-NDRV Propagation Delay		Includes leading-edge blanking time		90		ns
CS LIMIT COMPARATOR						
Current-Limit Threshold	V_{CS_LIMIT}		388	418	448	mV
GATE DRIVER (NDRV)						
$R_{DS(ON)}$ Pullup nMOS	R_{NDRVON}		0.3	0.6	1.3	Ω
$R_{DS(ON)}$ Pulldown nMOS	$R_{NDRVOFF}$	V_{COMP} = 0V, I_{SINK} = 100mA	0.3	0.6	1.3	Ω
Rise Time	t_R	C_{NDRV} = 10nF		40		ns
Fall Time	t_F	C_{NDRV} = 10nF		40		ns
PWM DIMMING						
Internal Ramp Frequency	f_{RAMP}		160	200	240	Hz
External Sync-Frequency Range	f_{DIM}		60		2000	Hz
External Sync Low-Level Voltage	V_{LTH}				0.4	V
External Sync High-Level Voltage	V_{HTH}		2			V
DIM Comparator Offset Voltage	V_{DIMOFS}		170	200	230	mV
DIM Voltage for 100% Duty Cycle			3.3			V

Electrical Characteristics (continued)

V_{IN} = 12V, R_{RT} = 85.4kΩ, C_{IN} = C_{VCC} = 1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25C (Note 2)

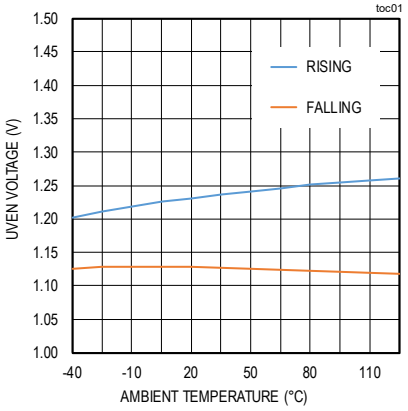
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWMDIM-Low to NDRV-Low Delay				70		ns
PWMDIM-High to NDRV-High Delay				40		ns
PWMDIM-to-LED Turn-Off Time		PWMDIM falling edge to rising edge on $\overline{DIMOUT}$, $C_{\overline{DIMOUT}}$ = 10nF		2		µs
PWMDIM-to-LED Turn-On Time		PWMDIM rising edge to falling edge on $\overline{DIMOUT}$, $C_{\overline{DIMOUT}}$ = 10nF		3		µs
pMOS GATE DRIVER ($\overline{DIMOUT}$)						
Peak Pullup Current	$I_{DIMOUTPU}$	PWMDIM = 0V, ($V_{ISENSE+}$ - $V_{\overline{DIMOUT}}$) = 7V	40	73	120	mA
Peak Pulldown Current	$I_{DIMOUTPD}$	($V_{ISENSE+}$ - $V_{\overline{DIMOUT}}$) = 0V	15	35	65	mA
$\overline{DIMOUT}$ Low Voltage with Respect to ISENSE+			-8.4	-7.4	-6.1	V
OVERVOLTAGE PROTECTION (OVP)						
OVP Threshold Rising	V_{OVP}	Output rising	1.17	1.23	1.29	V
Hysteresis				70		mV
Input Bias Current	I_{BOVP}	V_{OVP} = 1.235V	-500		+500	nA
SHORT-CIRCUIT HICCUP MODE						
Short-Circuit Threshold	$V_{SHORT-HIC}$	($V_{ISENSE+}$ - $V_{ISENSE-}$), V_{OVP} < 0.15V	369	398	427	mV
Hiccup Time	t_{HICCUP}			8192		Clock Cycle
SHORT-CIRCUIT VOLTAGE DETECT						
Short-Circuit Voltage Detect Threshold (MAX20090 only)	$V_{SHORT-VOUT}$	($V_{ISENSE+}$ - V_{IN}) falling, V_{IN} = 12V	1.15	1.55	1.95	V
OPEN-DRAIN FAULT ($\overline{FLT}$)						
Output-Voltage Low	$V_{OL-\overline{FLT}}$	V_{IN} = 4.75V, V_{OVP} = 2V, and I_{SINK} = 5mA		68.6	200	mV
Output Leakage Current		$V_{\overline{FLT}}$ = 5V			1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	$T_{SHUTDOWN}$	Temperature rising		165		°C
Thermal-Shutdown Hysteresis	T_{HYS}			10		°C

Note 2: All devices are 100% tested at T_A = T_J = +125°C, Limits over temperature are guaranteed by design.

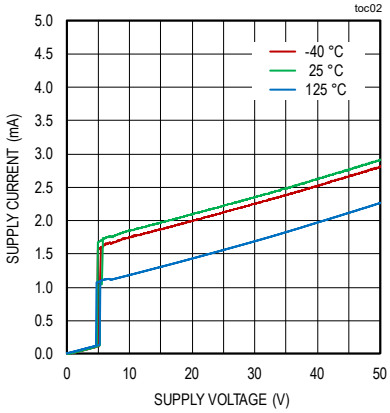
Typical Operating Characteristics

(V_{IN} = V_{EN} = 12V, T_A = +25°C, unless otherwise noted.)

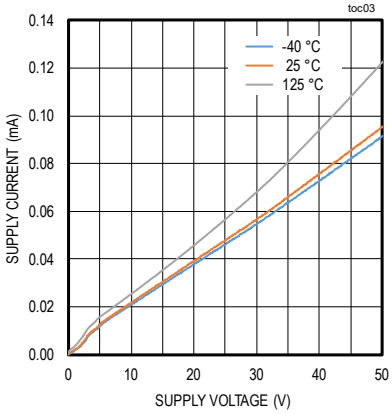
UVEN vs. TEMPERATURE



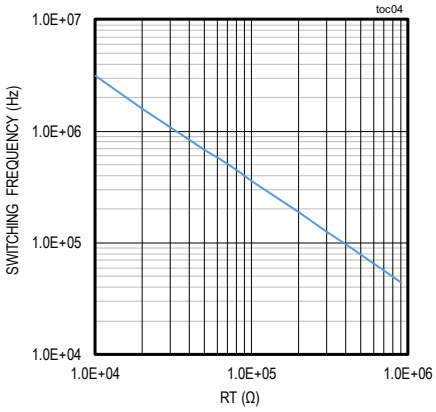
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



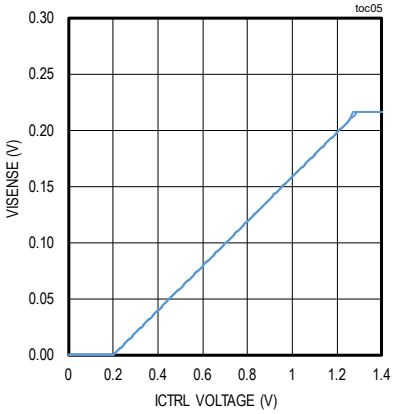
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



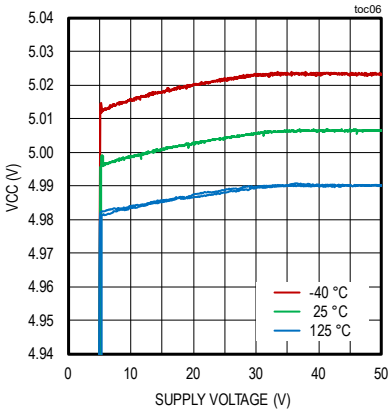
SWITCHING FREQUENCY vs. RT



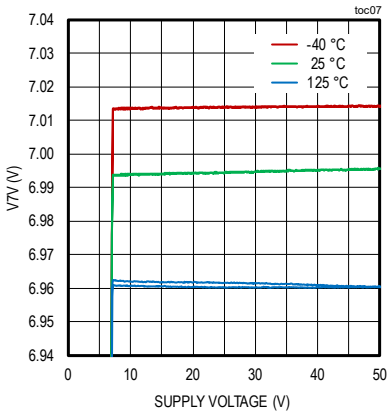
VISENSE vs. VICTRL



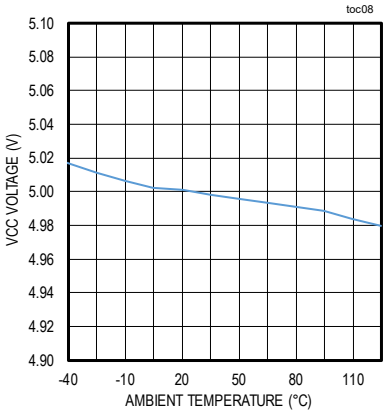
VCC vs. SUPPLY VOLTAGE



V7V vs. SUPPLY VOLTAGE



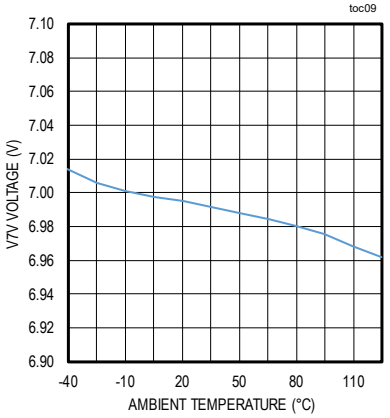
VCC vs. TEMPERATURE



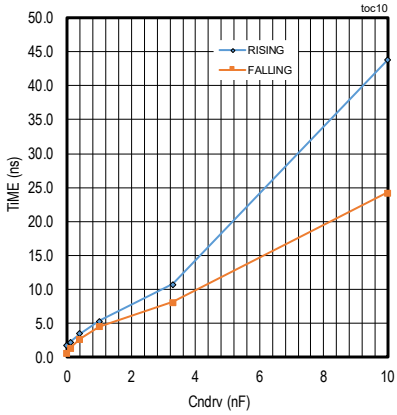
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 12V, T_A = +25°C, unless otherwise noted.)

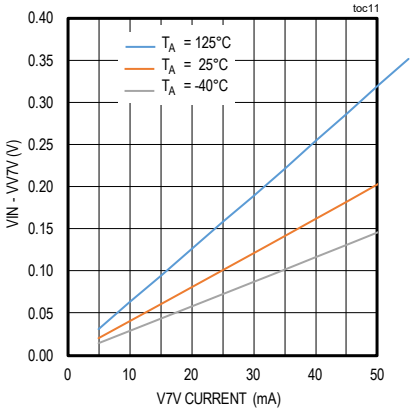
V7V vs. TEMPERATURE



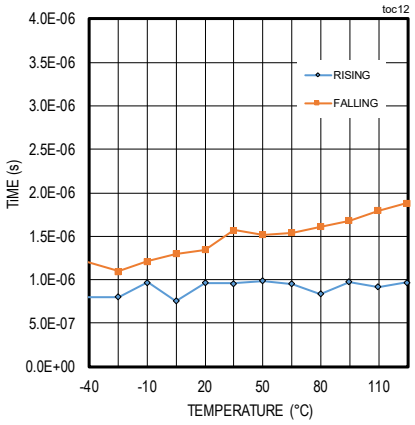
NDRV RISE AND FALL TIMES vs. NDRV CAPACITANCE



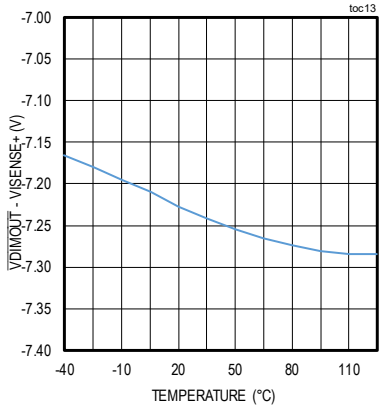
V7V DROPOUT VOLTAGE vs. V7V LOAD CURRENT



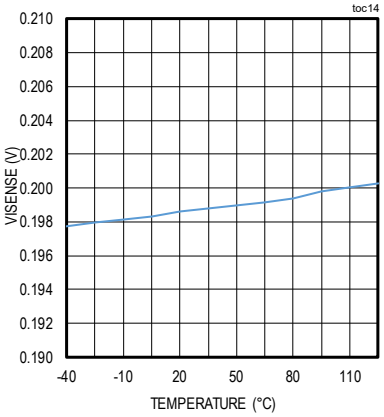
$\overline{DIMOUT}$ RISE AND FALL TIMES vs. NDRV TEMPERATURE



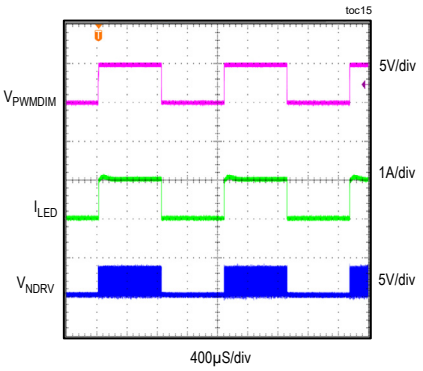
$\overline{VDIMOUTB}$ - VISENSE+ vs. TEMPERATURE



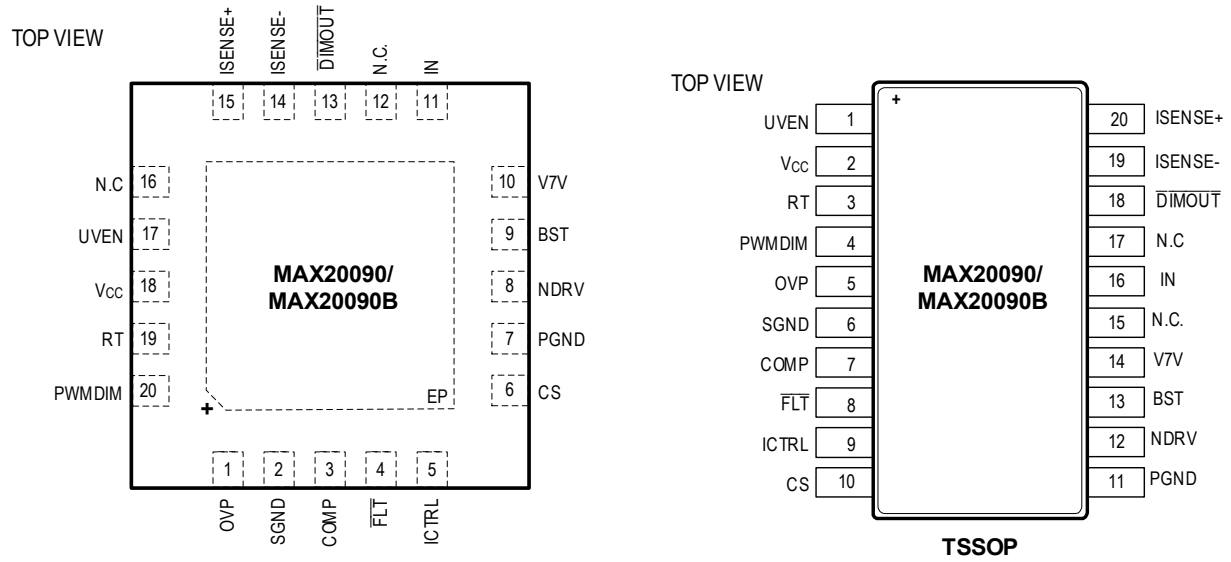
VISENSE vs. TEMPERATURE



600Hz DIMMING OPERATION



Pin Configurations



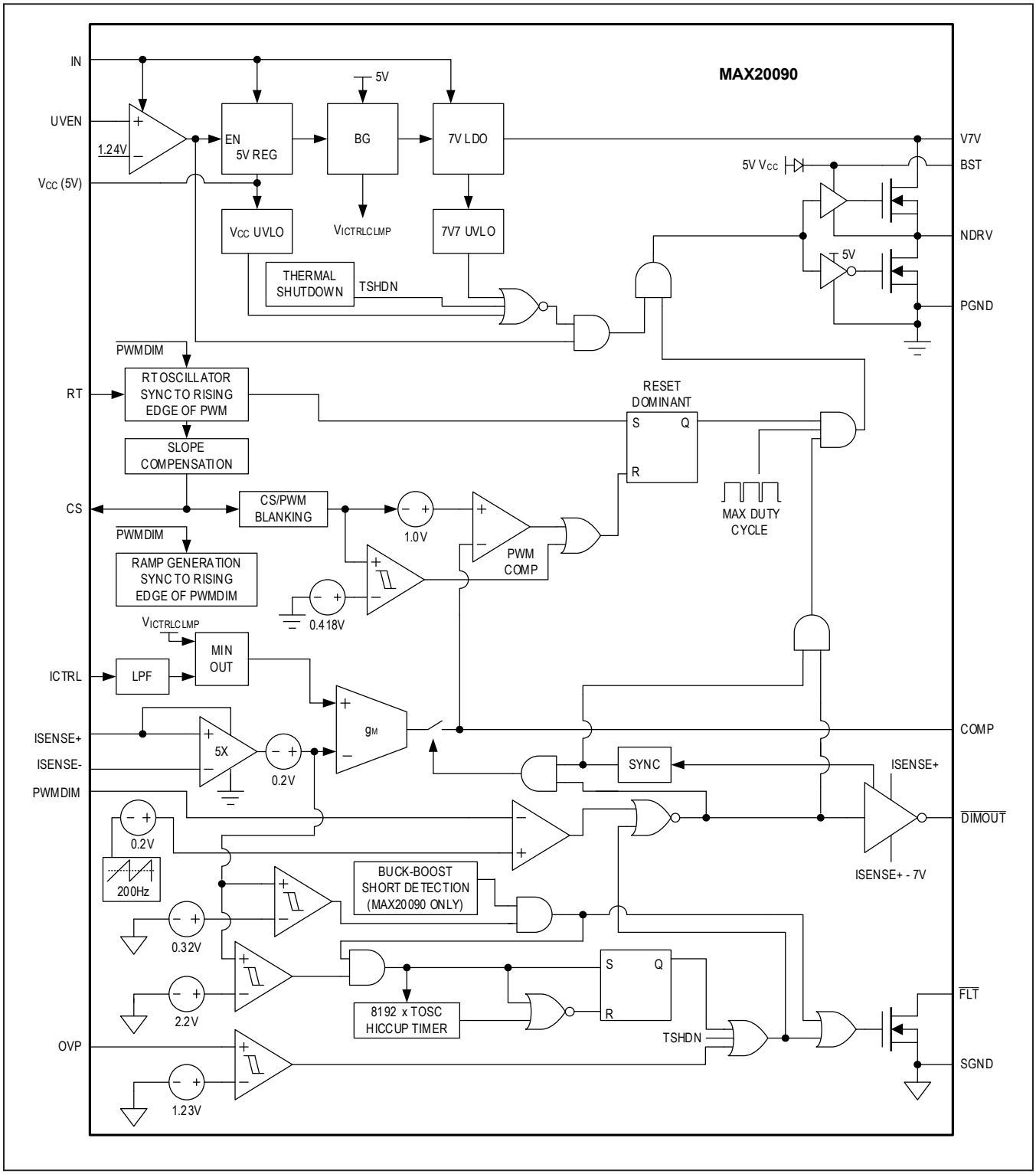
Pin Description

PIN		NAME	FUNCTION
TSSOP	TQFN		
1	17	UVEN	Undervoltage-Lockout (UVEN) Threshold/Enable Input. UVEN is a dual-function adjustable UVLO threshold input with an enable feature. Connect UVEN to V_{IN} through a resistive voltage-divider to program the UVLO threshold. Observe the absolute maximum value for this pin.
2	18	V_{CC}	5V Supply
3	19	RT	PWM Switching-Frequency Programming. Connect a resistor (R_{RT}) from RT to SGND to set the internal clock frequency. f_{OSC} (kHz) = 34200/R_{RT} (kΩ).
4	20	PWMDIM	Dimming-Control Input. Connect PWMDIM to an external PWM signal for PWM dimming. For analog voltage-controlled PWM dimming, connect PWMDIM to V_{CC} through a resistive voltage-divider. The dimming frequency is 200Hz under these conditions. Connect PWMDIM to SGND to turn off the LEDs.
5	1	OVP	Overvoltage-Protection Input for the LED String. Connect a resistive divider between the boost output, OVP, and PGND. When the voltage on OVP exceeds 1.23V, a fast-acting comparator immediately stops PWM switching. This comparator has hysteresis of 70mV.
6	2	SGND	Signal Ground

Pin Description (continued)

PIN		NAME	FUNCTION
TSSOP	TQFN		
7	3	COMP	Compensation-Network Connection. For proper compensation, connect a suitable RC network from COMP to SGND.
8	4	$\overline{FLT}$	Active-Low, Open-Drain Fault Indicator Output. See the *Fault Indicator (FLT)* section.
9	5	ICTRL	Analog Dimming Control Input. Connect an analog voltage from 0 to 1.2V for analog dimming of LED current.
10	6	CS	Current-Sense Amplifier Positive Input for the Switching Regulator. Add a resistor from CS to the switching-MOSFET current-sense resistor terminal for programming the slope compensation.
11	7	PGND	Power Ground
12	8	NDRV	External n-Channel Gate-Driver Output
13	9	BST	Connect a minimum of 0.01µF capacitor from BST to NDRV to provide power supply for the gate driver.
14	10	V7V	7V Low-Dropout Voltage-Regulator Output. Bypass V7V to PGND with a 1µF (min) ceramic capacitor.
15, 17	12, 16	N.C	No Connection
16	11	IN	Positive Power-Supply Input. Bypass IN to PGND with at least a 1µF ceramic capacitor.
18	13	$\overline{DIMOUT}$	External Dimming p-Channel MOSFET Gate Driver
19	14	ISENSE-	Negative LED Current-Sense Input
20	15	ISENSE+	Positive LED Current-Sense Input. The voltage between ISENSE+ and ISENSE- is proportionally regulated to the lesser of (ICTRL, 1.3V).
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP **must** be connected to GND.

Block Diagram



Detailed Description

The MAX20090 is a single-channel HB LED driver for automotive front-light applications such as high beam, low beam, daytime-running lights (DRLs), turn indicators, fog lights, and other LED lights. It can take an input voltage from 5V to 65V and drive a string of LEDs with a maximum output voltage of 65V.

The device senses output current at the high side of the LED string. High-side current sensing is required to protect for shorts from the output to the ground or battery input. It is also the most flexible scheme for driving LEDs, allowing boost, high-side buck, SEPIC mode, or buck-boost-mode configurations. The PWM input provides LED dimming ratios of up to 1000:1, and the ICTRL input provides additional analog-dimming capability in the device. The device also includes a fault flag ($\overline{FLT}$) that indicates open string, shorted string, and thermal shutdown. The device has built-in spread-spectrum modulation for improved electromagnetic-compatibility performance. The device can also be used in zeta and Ćuk converter configurations, if necessary in some applications.

Functional Operation of the MAX20090

The operation of the device is best understood by referring to the *Block Diagram*. The device is enabled when the UVEN pin goes above 1.24V (typ). In addition to the UVEN input, the 5V regulator and the 7V regulator inputs also need to be above their respective UVLO limits, before switching on NDRV can begin. The device is a constant-frequency, current-mode controller with a low-side nMOS gate driver. The nMOS gate-drive voltage is enhanced to 7V by the V7V pin. The control circuitry inside the device uses a 5V supply, but the gate driver has a 7V output. This can be seen from the *Block Diagram*. When PWMDIM goes high, switching is initiated. The RT oscillator can be programmed from 200kHz to 2.2MHz by the resistor on the RT pin (R_{RT}). Additional spread-spectrum dithering is added to the oscillator to alleviate EMI problems in the LED driver. The RT oscillator is synchronized to the positive-going edge of the PWM pulse. This means that the NDRV pulse goes high at the same instant as the positive-going pulse on PWMDIM. Synchronizing the RT oscillator to the PWMDIM pulse also guarantees that the switching-frequency variation over a period of a PWMDIM pulse is the same from one PWMDIM pulse to the next. This prevents flicker during PWM dimming when spread spectrum is added to the RT oscillator.

Once PWMDIM goes high, the external switching MOSFET is turned on. A current flows through the external switching MOSFET and this current is sensed by the voltage across the current-sense resistor from the source of the external MOSFET to PGND. The source of the external MOSFET is connected to the CS pin of the device through a slope-compensation resistor (R_{SC}) (see the *Simplified Schematic*). The slope-compensation current flows out of the CS pin into the R_{SC} resistor. The voltage on CS is the voltage across the current-sense resistor (R_{CS_FET}) + slope-compensation current x R_{SC}. The slope compensation prevents subharmonic oscillation when the duty cycle exceeds 50%. The current in the external inductor increases steadily when the external MOSFET is on. The voltage on CS is fed to a current-limit comparator. This current-limit comparator is used to protect the external switch from overcurrents, and causes switching to stop for that particular cycle if the CS voltage exceeds 0.418V. An offset of 1.0V is added to the CS voltage, and this voltage is fed to the positive input of a PWM comparator. The negative input of this comparator is a control voltage from the error amplifier that regulates the LED current. When the positive input of the PWM comparator exceeds the control voltage from the error amplifier, the switching is stopped for that particular cycle and the external nMOS stays off until the next switching cycle. When the external MOSFET is turned off, the inductor current decays. When the next switching cycle starts and the external MOSFET is turned on, the inductor current starts ramping back up. Through this repetitive action, the PWM-control algorithm establishes a switching duty cycle to regulate current to the LED load.

When PWMDIM goes high, the external dimming MOSFET driven by $\overline{DIMOUT}$ is also tuned on. This external dimming MOSFET is a p-channel MOSFET and is connected on the high side. The source of this pMOS is connected to ISENSE- and the gate is connected to $\overline{DIMOUT}$. The drain of this MOSFET is connected to the anode of the external LED string. In certain applications, it is not necessary to use this dimming MOSFET and in these cases, the $\overline{DIMOUT}$ pin is left open. The external pMOS is turned on when PWMDIM is high and is turned off when PWMDIM is low. During normal operation when PWMDIM is high, the voltage across the resistor from ISENSE+ to ISENSE- is regulated to a programmed voltage. This programmed voltage is 0.2 x ($V_{(ICTRL)}$ - 0.2). The external pMOS switch is also used for fault protection as well. Once a fault condition is detected, the $\overline{DIMOUT}$ pin is pulled high to turn off the pMOS switch. This isolates the LED string from the fault condition and prevents excessive voltage or current from damaging the LEDs.

Input Voltage (IN)

The input supply pin (IN) must be locally bypassed with a minimum of 1µF capacitance close to the pin. All the input current drawn by the device goes through this pin. The positive terminal of the bypass capacitor must be placed as close as possible to this pin and the negative terminal of the bypass capacitor must be placed as close as possible to the PGND pin.

Undervoltage Lockout (UVLO)

The device features adjustable UVLO using the enable input (UVEN). Connect UVEN to V_{IN} through a resistive divider to set the UVLO threshold. The device is enabled when V_{UVEN} exceeds the 1.24V (typ) threshold. UVEN also functions as an enable/disable input to the device. Drive UVEN low to disable the output and high to enable the output.

V_{CC} Regulator

The V_{CC} supply is the low-voltage analog supply for the device and derives power from the input voltage from IN to PGND. Use a 1µF low-ESR ceramic capacitor from V_{CC} to PGND for stable operation. The V_{CC} regulator provides power to all the internal logic and control circuitry inside the device.

7V Linear Regulator (V7V)

The device features a 7V low-side linear regulator (V7V). V7V powers up the switching MOSFET driver with sourcing capability of up to 50mA. Use a 1µF (min) low-ESR ceramic capacitor from V7V to PGND for stable operation. The V7V regulator goes below 7V if the input voltage falls below 7V. The dropout voltage for this regulator at 50mA is 0.2V. This means that for an input voltage of 5V, the V7V voltage is 4.8V. The short-circuit current on the V7V regulator is 100mA (typ). It is also possible to apply an external voltage on the V7V regulator output and save its power dissipation. The maximum externally applied voltage on V7V should not exceed its absolute maximum rating.

BST Capacitor Node (BST)

Use the BST pin to provide a drive voltage to the low-side switching MOSFET that is higher than V_{CC}. An internal diode is connected from BST to V_{CC}. Connect a 0.01µF (min) ceramic capacitor from this pin to the NDRV pin. Place the capacitor as close as possible to this pin.

Dimming MOSFET Driver ($\overline{DIMOUT}$)

The device requires an external p-channel MOSFET for PWM dimming. For normal operation, connect the gate of the MOSFET to the output of the dimming driver ($\overline{DIMOUT}$). The dimming driver can sink up to 35mA or source up to 77mA of peak current for fast charging and discharging of the pMOS gate. When the PWMDIM signal is high, this driver pulls the pMOS gate to 7.4V below the ISENSE+ pin to completely turn on the p-channel dimming MOSFET. The $\overline{DIMOUT}$ pin inverts and level shifts the signal on PWMDIM to drive the gate of the external pMOS. In some applications, the pMOS dimming MOSFET is not used. In these cases, the $\overline{DIMOUT}$ pin can be left open.

LED Current-Sense Inputs (ISENSE+/ISENSE-)

The differential voltage from ISENSE+ to ISENSE- is fed to an internal current-sense amplifier. This amplified signal is then connected to the negative input of the transconductance error amplifier. The voltage-gain factor of this amplifier is 5. The resistor is connected between ISENSE+ and ISENSE- to program the maximum LED current. The full-scale signal is 200mV. The ISENSE+ pin should be connected to the positive terminal of the current-sense resistor and the ISENSE- pin should be connected to the negative terminal of the current-sense resistor (LED string anode side).

Internal Oscillator (RT)

The internal oscillators of the MAX20090 are programmable from 200kHz to 2.2MHz using a single resistor at RT. Use the equation below to calculate the switching frequency:

$$f_{OSC}\ (kHz) = 34{,}200/R_{RT}\ (k\Omega)$$

where R_{RT} is the resistor from RT to SGND.

The frequency calculated from the above formula may not be totally accurate, and some final trimming might be needed. The resistor values for a frequency of 200kHz is 188kΩ, 1MHz is 34.2kΩ, and 2.2MHz is 14.7kΩ.

The switching-frequency oscillator in the device is synchronized to the leading edge of the PWM dimming pulse on input PWMDIM. The device has built-in frequency dithering of ±6% of the programmed frequency to alleviate EMI problems.

Spread-Spectrum Option

The device has an internal spread-spectrum option to optimize EMI performance. This is factory set and the S-version of the device should be ordered. For spread-spectrum-enabled devices, the operating frequency is varied ±6%, centered on the oscillator frequency (f_{OSC}). The modulation signal is a triangular wave with a period of 190µs at 2.2MHz. Therefore, f_{OSC} ramps down 6% and back to 2.2MHz in 190µs and also ramps up 6% and back to 2.2MHz in 190µs. The cycle then repeats.

For operations at f_{OSC} values other than 2.2MHz, the modulation signal scales proportionally (e.g., at 400kHz, the 100µs modulation period increases to 190µs x 2.2MHz/400kHz = 1045µs).

n-Channel Switching-MOSFET Driver (NDRV)

The device drives an external n-channel switching MOSFET (NDRV). NDRV swings between V7V and PGND. NDRV can sink/source 2A of peak current, allowing the ICs to switch MOSFETs in high-power applications. The average current demanded from the supply to drive the external MOSFET depends on the total gate charge (Q_g) and the operating frequency of the converter (f_{SW}). Use the following equation to calculate the driver supply current (I_{NDRV}) required for the switching MOSFET:

$$I_{NDRV} = Q_g \times f_{SW}$$

Switching-MOSFET Current-Sense Input (CS)

CS is part of the current-mode-control loop. The switching control uses the voltage on CS, set by R_{CS_FET} and R_{SC} to terminate the on-pulse width of the switching cycle, thus achieving peak current-mode control. Internal leading-edge blanking of 66ns is provided to prevent premature turn-off of the switching MOSFET in each switching cycle. Resistor R_{CS_FET} is connected between the source of the n-channel switching MOSFET and PGND. During switching, a current ramp with a slope of 50µA x f_{SW} is sourced from the CS input. This current ramp, along with resistor R_{SC}, programs the amount of slope compensation.

Overvoltage Protection (OVP)

OVP sets the overvoltage-threshold limit across the LEDs. Use a resistive divider between ISENSE+ to OVP and SGND to set the overvoltage-threshold limit. An internal overvoltage-protection comparator senses the differential voltage across OVP and SGND. If the differential voltage is greater than 1.23V, NDRV goes low, $\overline{DIMOUT}$ goes high, and $\overline{FLT}$ asserts. When the differential voltage drops by 70mV, NDRV is enabled if PWMDIM is high and $\overline{DIMOUT}$ goes low. $\overline{FLT}$ deasserts only if PWMDIM is high and $V_{(ISENSE+ - ISENSE-)}$ is > 20mV.

Output Short-Circuit Protection

The MAX20090/MAX20090B feature output short-circuit protection. This feature is most useful when the LEDs are connected to the LED driver by long cables and there is the possibility of a short occurring when connectors are exposed.

For the MAX20090, a short circuit is detected when the following two conditions are met:

- ($V_{ISENSE+}$ - V_{IN}) falls below the $V_{SHORT-VOUT}$ threshold, 1.55V (typ).
- The current-sense voltage across ($V_{ISENSE+}$ - $V_{ISENSE-}$) exceeds the $V_{SHORT-HIC}$ threshold, 398mV (typ).

The $V_{SHORT-VOUT}$ threshold flag in MAX20090B is disabled for applications in which ($V_{ISENSE+}$ - V_{IN}) is expected to be less than 1.55V (typ) during normal operation. In this case, the $V_{SHORT-HIC}$ threshold is the only criteria for detecting a short circuit.

The MAX20090/MAX20090B respond to a short circuit by entering hiccup mode, which stops NDRV and pulls $\overline{DIMOUT}$ high to turn off the DIM FET, disconnecting the output of the LED driver from the shorted LEDs. The device waits 8192 clock cycles before attempting to drive the LEDs again.

The MAX20090AUPA has a 1µs deglitch filter before the hiccup mode is triggered.The MAX20090AUPB has the hiccup mode disabled.

Internal Transconductance Amplifier

The device has a built-in transconductance amplifier used to amplify the error signal inside the feedback loop. The typical transconductance is 1800µS. For proper operation of this transconductance amplifier, it is necessary to add a 500kΩ resistor from the COMP pin to ground. Without this resistor, the performance during PWM dimming is compromised.

Analog Dimming

The device offers an analog dimming-control input pin (ICTRL). The voltage at ICTRL sets the LED current level when V_{ICTRL} < 1.2V. The LED current can be linearly adjusted from zero with the voltage on ICTRL. For V_{ICTRL} > 1.4V, an internal reference sets the LED current. The maximum withstand voltage of this input is 6V. The LED current is guaranteed to be at zero when the ICTRL voltage is at or below 0.18V. The LED current can be linearly adjusted from zero to full scale for the ICTRL voltage in the range of 0.2V to 1.2V.

Pulsed-Dimming Input (PWMDIM)

PWMDIM functions with either analog or PWM control signals. Once the internal pulse detector detects three successive edges of a PWM signal with a frequency between 60Hz and 2kHz, the device synchronizes to the external signal and pulse-width modulates the LED current at the external PWMDIM input frequency, with the same duty cycle as the PWMDIM input. If an analog control signal is applied to PWMDIM, the device compares the DC input to an internally generated 200Hz

ramp to pulse-width-modulate the LED current (f_{DIM} = 200Hz). The output-current duty cycle is linearly adjustable from 0% to 100% (0.2V < V_{PWMDIM} < 3.2V).

Use the following formula to calculate the voltage (V_{PWMDIM}), necessary for a given output-current duty cycle (D):

$$V_{PWMDIM} = (D \times 3.0) + 0.2V$$

where V_{PWMDIM} is the voltage applied to PWMDIM in volts.

Power Ground (PGND)

This pin is the power ground for the LED driver circuitry. Place the negative terminal of the input bypass capacitor as close as possible to the PGND pin.

Signal Ground (SGND)

This is the analog ground pin for all the LED driver control circuitry. Connect PGND (power ground) and SGND together at the negative terminal of the input bypass capacitor.

Thermal Shutdown

Internal thermal-shutdown circuitry is provided to protect the device in the event the maximum junction temperature is exceeded. The threshold for thermal shutdown is 165°C with 10°C hysteresis (both values typ). The part returns to regulation mode once the junction temperature goes below +155°C. This results in a cycled output during continuous thermal-overload conditions.

Fault Indicator ($\overline{FLT}$)

The device features an active-low, open-drain fault indicator ($\overline{FLT}$). $\overline{FLT}$ asserts when one of the following conditions occur:

1) Overvoltage or open across the LED string
2) Short-circuit condition across the LED string
3) Overtemperature condition

For overvoltage or open across the LED string, the $\overline{FLT}$ indicator asserts only when an overvoltage occurs with the PWMDIM in the high state. Once asserted, $\overline{FLT}$ stays low and only changes state if PWMDIM is high, the overvoltage condition is removed, and the voltage across the LED current-sense resistor is above 20mV. The $\overline{FLT}$ signal never changes state when PWMDIM is low.

Exposed Pad

The MAX20090 package features an exposed thermal pad on its underside that should be used as a heat sink. This pad lowers the package's thermal resistance by providing a direct heat-conduction path from the die to the PCB. Connect the exposed pad and GND to the system ground using a large pad or ground plane, or multiple vias to the ground plane layer.

Applications Information

V_{CC} Regulator

The internal 5V regulator is used to power the internal control circuitry inside the device, except for the output gate driver. This regulator can provide a load of 10mA to external circuitry. The 5V regulator requires an external ceramic capacitor for stable operation. A 1FF ceramic capacitor is adequate for most applications. Place the ceramic capacitor close to the IC to minimize trace length to the internal V_{CC} pin and also to the IC ground. Choose a 10V rated low-ESR, X7R ceramic capacitor for optimal performance.

7V Regulator

The 7V regulator also requires a capacitor on the output for stable operation. Place the capacitor close to the IC to minimize trace length to the V7V pin and to the PGND pin. Use a 10V or higher low-ESR, X7R ceramic capacitor for best performance. A 2.2FF ceramic capacitor should be adequate in most applications. This capacitor is used to provide the peak switching currents required to drive the external MOSFET on NDRV. The maximum current that can be delivered by the 7V regulator is 50mA. The current from the 7V regulator is given by:

$$I_{7V} = Q_g \times f_{SW}$$

where Q_g is the gate charge of the external MOSFET at 7V VGS and f_{SW} is the switching frequency. This current should not exceed 50mA. The 7V regulator has UVLO at 4.33V that causes the gate drive to be disabled if the input voltage falls below the UVLO threshold.

Programming the UVLO Threshold

The UVLO threshold is set by resistors R_{UVEN1} and R_{UVEN2} (see the *Simplified Schematic*). The device turns on when the voltage across R_{UVEN2} exceeds 1.24V, the UVLO threshold. Use the following equation to set the desired UVLO threshold:

$$V_{UVEN} = 1.24 \times (R_{UVEN1} + R_{UVEN2})/R_{UVEN2}$$

The UVEN pin can also be used as a separate enable pin where an external logic signal can turn on and off the device.

Programming the LED Current

Normal sensing of the LED current should be done on the high side where the LED current-sense resistor is connected to the anode of the LED string. The LED current is programmed using resistor R_{CS_LED} (see the *Simplified Schematic*).

The LED current can also be programmed adjusting the voltage on ICTRL when $V_{ICTRL} \leq 1.2V$ (analog dimming). The current is given by:

$$I_{LED} = (V_{ICTRL} - 0.2)/(5 \times R_{CS\_LED})$$

Programming the Switching Frequency

The internal oscillator of the device is programmable from 200kHz to 2.2MHz using a single resistor at RT.

Use the following equation to calculate the value of the resistor (R_{RT}):

$$R_{RT}(k\Omega) = 34{,}200/f_{OSC}(kHz)$$

where $f_{OSC}(kHz)$ is the desired switching frequency in kHz.

The frequency calculated from the above formula may not be totally accurate, and some final trimming might be needed. The resistor values for a frequency of 200kHz is 88kΩ, 1MHz is 34.2kΩ, and 2.2MHz is 14.7kΩ.

Additional ±6% spread spectrum is added internally to the oscillator to improve EMI performance.

Setting the Overvoltage Threshold

The overvoltage threshold is set by resistors R_{OVP1} and R_{OVP2} (see the *Simplified Schematic*). The overvoltage circuit in the device is activated when the voltage on OVP with respect to GND exceeds 1.23V. Use the following equation to set the desired overvoltage threshold:

$$V_{OVP} = 1.23 \times (R_{OVP1} + R_{OVP2})/R_{OVP2}$$

Inductor Selection

Boost Configuration

In the boost converter, the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage.

For the boost converter, the average inductor current is equal to the input current. Calculate maximum duty cycle using the equation below:

$$D_{MAX} = (V_{LED} - V_D - V_{INMIN})/(V_{LED} + V_D - V_{FET})$$

where V_{LED} is the forward voltage of the LED string in volts, V_D is the forward drop of rectifier diode D1 in volts (approximately 0.6V), V_{INMIN} is the minimum input supply voltage in volts, and V_{FET} is the average drain-to source voltage of MOSFET N1 in volts when it is on. Use an approximate value of 0.2V initially to calculate D_{MAX}. A more accurate value of the maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current. Use the following equations to calculate the maximum average inductor current (IL_{AVG}), peak-to-peak inductor current ripple (ΔIL), and the peak inductor current (I_{LP}) in amperes:

$$IL_{AVG} = I_{LED}/(1 - D_{MAX})$$

Allowing the peak-to-peak inductor ripple to be ΔIL, the peak inductor current is given by:

$$I_{LP} = IL_{AVG} + 0.5 \times \Delta IL$$

The inductance value (L) of inductor L1 in henries (H) is calculated as:

$$L = (V_{INMIN} - V_{FET}) \times D_{MAX}/(f_{SW} \times \Delta IL)$$

where f_{SW} is the switching frequency in hertz, V_{INMIN} and V_{FET} are in volts, and ΔIL is in amperes. Choose an inductor that has a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than I_{LP} at the operating temperature.

Buck-Boost Configuration

In the buck-boost LED driver, the average inductor current is equal to the input current plus the LED current. Calculate the maximum duty cycle using the following equation:

$$D_{MAX} = (V_{LED} + V_D)/(V_{LED} + V_D + V_{INMIN} - V_{FET})$$

where V_{LED} is the forward voltage of the LED string in volts, V_D is the forward drop of rectifier diode D1 (~ 0.6V) in volts, V_{INMIN} is the minimum input supply voltage in volts, and V_{FET} is the average drain-to-source voltage of MOSFET N1 in volts when it is on. Use an approximate value of 0.2V initially to calculate D_{MAX}. A more accurate value of the maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current.

Use the equations below to calculate the maximum average inductor current (IL_{AVG}), peak-to-peak inductor current ripple (ΔIL), and the peak inductor current (IL_P) in amperes:

$$IL_{AVG} = I_{LED}/(1 - D_{MAX})$$

Allowing the peak-to-peak inductor ripple to be ΔIL:

$$I_{LP} = IL_{AVG} + 0.5 \times \Delta IL$$

where I_{LP} is the peak inductor current.

The inductance value (L) of inductor L1 in henries is calculated as:

$$L = (V_{INMIN} - V_{FET}) \times D_{MAX}/(f_{SW} \times \Delta IL)$$

where f_{SW} is the switching frequency in hertz, V_{INMIN} and V_{FET} are in volts, and ΔIL is in amperes. Choose an inductor that has a minimum inductance greater than the calculated value.

High-Side Buck Configuration

In the high-side buck LED driver, the average inductor current is the same as the LED current. The peak inductor current occurs at the maximum input line voltage where the duty cycle is at the minimum:

$$D_{MIN} = (V_{LED} + V_D)/(V_{INMAX} - V_{FET})$$

where V_{LED} is the forward voltage of the LED string in volts, V_D is the forward drop of rectifier diode D1 (~ 0.6V) in volts, V_{INMAX} is the maximum input supply voltage in volts, and V_{FET} is the average drain-to-source voltage of MOSFET N1 in volts when it is on. Use an approximate value of 0.2V initially to calculate D_{MIN}. The maximum peak-to-peak inductor ripple (ΔIL) occurs at the maximum input line. The peak inductor current is given by:

$$I_{LP} = I_{LED} + 0.5 \times \Delta IL$$

The inductance value (L) of inductor L1 in henries is calculated as:

$$L = (V_{INMAX} - V_{FET} - V_{LED}) \times D_{MIN}/(f_{SW} \times \Delta IL)$$

where f_{SW} is the switching frequency in hertz, V_{INMAX} and V_{FET} are in volts, and ΔIL is in amperes. Choose an inductor that has a minimum inductance greater than the calculated value.

SEPIC, Zeta, and Ćuk Configurations

In the SEPIC, zeta, and Ćuk converters, there are separate inductors for L1 and L2. Neglecting the drops in the switching MOSFET and diode, the maximum duty cycle (D_{MAX}) occurs at low line and is given by:

$$D_{MAX} = V_{LED}/(V_{INMIN} + V_{LED})$$

where V_{LED} is the LED string voltage and V_{INMIN} is the minimum input voltage. If the desired maximum input current ripple is ΔIL_{IN}, then the inductor value of L1 is given by:

$$L1 = V_{INMIN} \times D_{MAX}/(\Delta IL_{IN} \times f_{SW})$$

The peak inductor current in L1 is IL_{INP} and is given by:

$$IL_{INP} = (I_{LED} \times D_{MAX}/(1 - D_{MAX})) + 0.5 \times \Delta IL_{IN}$$

To account for current transients, the peak saturation rating of the inductor should be 1.2 times the calculated value above. The average output current in inductor L2 is the same as the LED current. The desired maximum peak-to-peak output current ripple is ΔIL_{OUT}. The value of the inductor L2 is given by:

$$L2 = V_{INMIN} \times D_{MAX}/(\Delta IL_{OUT} \times f_{SW})$$

The peak inductor current in L2 is IL_{OUTP} and is given by:

$$IL_{OUTP} = I_{LED} + 0.5 \times \Delta IL_{OUT}$$

Selecting Slope Compensation and MOSFET Current-Sense Resistor

Slope compensation should be added to converters with peak current-mode-control operating in continuous-conduction mode with more than 50% duty cycle to avoid current-loop instability and subharmonic oscillations. The minimum amount of slope compensation required for stability is:

$$\text{min slope} = 0.5 \times (\text{inductor current downslope} - \text{inductor current upslope}) \times R_{CS\_FET}$$

In the MAX20090, the slope-compensating ramp is added to the current-sense signal before it is fed to the PWM comparator. Connect a resistor (R_{SC}) from CS to the switch current-sense resistor terminal for programming the amount of slope compensation.

The device generates a current ramp with a slope of 50µA/t_{OSC} for slope compensation. The current-ramp signal is forced into an external resistor (R_{SC}) connected between CS and the source of the external MOSFET, thereby adding a programmable slope-compensating voltage (V_{SCOMP}) at the current-sense input CS. Therefore:

$$dv(V_{SCOMP})/dt = (R_{SC} \times 50\mu A)/t_{OSC} \text{ in V/s}$$

The minimum required value of the slope-compensation voltage that needs to be added to the current signal at peak of the current signal at minimum line voltage is:

For boost LED driver:

$$V_{SLOPE}\,(MIN) = (D_{MAX} \times (V_{LED} - 2V_{INMIN}) \times R_{CS\_FET})/(2 \times L_{MIN} \times f_{SW}) \text{ volts}$$

For buck-boost LED driver:

$$V_{SLOPE}\,(MIN) = (D_{MAX} \times (V_{LED} - V_{INMIN}) \times R_{CS\_FET})/(2 \times L_{MIN} \times f_{SW}) \text{ volts}$$

For high-side buck LED driver:

$$V_{SLOPE}\,(MIN) = (D_{MAX} \times (2V_{LED} - V_{INMIN}) \times R_{CS\_FET})/(2 \times L_{MIN} \times f_{SW}) \text{ volts}$$

For SEPIC LED driver:

$$V_{SLOPE}\,(MIN) = (D_{MAX} \times (V_{LED} - V_{INMIN}) \times R_{CS\_FET})/(2 \times L_{MIN} \times f_{SW}) \text{ volts}$$

where $L_{MIN} = SQRT\,(L1_{MIN} \times L2_{MIN})$

where L1 and L2 are the two inductors in the SEPIC configuration, f_{SW} is the switching frequency, D_{MAX} is the maximum duty cycle that occurs at minimum input voltage V_{INMIN}, and L_{MIN} is the minimum value of the selected inductor. For adequate margin, use a slope compensation that is 1.5 times the minimum required value of the slope compensation.

The minimum value of the peak current-limit comparator is 0.388V. The current-sense resistor value is given by:

$$R_{CS\_FET} = (0.388\text{-slope compensation voltage})/I_{LP}$$

where I_{LP} is the peak inductor current that occurs at low line in the boost, SEPIC, and buck-boost configuration.

For boost configuration:

$$R_{CS\_FET} = \frac{0.388}{\left(I_{LP} + 0.75D_{MAX}\frac{V_{LED} - 2V_{INMIN}}{L_{MIN} f_{SW}}\right)}$$

For buck-boost configuration:

$$R_{CS\_FET} = \frac{0.388}{\left(I_{LP} + 0.75D_{MAX}\frac{V_{LED} - V_{INMIN}}{L_{MIN} f_{SW}}\right)}$$

For SEPIC configuration:

$$R_{CS\_FET} = \frac{0.388}{\left(I_{LP1} + I_{LP2} + 0.75D_{MAX}\frac{V_{LED} - V_{INMIN}}{f_{SW}\sqrt{L_{1MIN} L_{2MIN}}}\right)}$$

Input Capacitor

The input-filter capacitor bypasses the ripple current drawn by the converter and reduces the amplitude of high-frequency current conducted to the input supply.

The ESR, ESL, and bulk capacitance of the input capacitor contribute to the input ripple. Use a low-ESR input capacitor that can handle the maximum input RMS ripple current from the converter. For the boost configuration, the input current is the same as the inductor current. For buck-boost configuration, the input current is the inductor current minus the LED current. However, for both configurations, the ripple current that the input filter capacitor has to supply is the same as the inductor ripple current with the condition that the output filter capacitor should be connected to ground for buck-boost configuration. Neglecting the effect of LED current ripple, the calculation of the input capacitor for boost, as well as buck-boost configurations is the same. Neglecting the effect of the ESL, ESR, and bulk capacitance at the input contributes to the input-voltage ripple. For simplicity, assume that the contribution from the ESR and the bulk capacitance is equal. This allows 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{IN} > \Delta IL/(4 \times \Delta V_{IN} \times f_{SW})$$

where ΔIL is in amperes, C_{IN} is in farads, f_{SW} is in hertz, and ΔV_{IN} is in volts. The remaining 50% of allowable ripple is for the ESR of the output capacitor.

Use X7R ceramic capacitors for optimal performance. The selected capacitor should have the minimum required capacitance at the operating voltage.

In the buck mode, the input capacitor has large pulsed currents due to the current flowing in the freewheeling diode when the switching MOSFET is off. It is very important to consider the ripple-current rating of the input capacitor in this application.

Output Capacitor Selection

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise generated by the ceramic capacitors during PWM dimming, it may be necessary to minimize the number of ceramic capacitors on the output. In these cases, an additional electrolytic or tantalum capacitor provides most of the bulk capacitance.

Boost and Buck-Boost Configurations

The calculation of the output capacitance is the same for both boost and buck-boost configurations. The output ripple is caused by the ESR and bulk capacitance of the output capacitor if the ESL effect is considered negligible. For simplicity, assume that the contributions from ESR and bulk capacitance are equal, allowing 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{OUT} \geq \frac{I_{LED} \times 2 \times D_{MAX}}{V_{OUTRIPPLE} \times f_{SW}}$$

where I_{LED} is in amperes, C_{OUT} is in farads, f_{SW} is in hertz, and $V_{OUTRIPPLE}$ is in volts. The remaining 50% of allowable ripple is for the ESR of the output capacitor. Based on this, the ESR of the output capacitor is given by:

$$ESR_{COUT} < \frac{V_{OUTRIPPLE}\ (\Omega)}{(IL_P \times 2)}$$

where I_{LP} is the peak inductor current in amperes.

Rectifier Diode Selection

Use a Schottky diode as the rectifier (D1) for fast switching and to reduce power dissipation. The selected Schottky diode must have a voltage rating 20% above the maximum converter output voltage. The maximum converter output voltage is V_{LED} in the boost configuration and V_{LED} + V_{INMAX} in the buck-boost configuration.

The current rating of the diode should be greater than I_D in the following equation:

$$I_D = IL_{AVG}\ (1 - D_{MAX})1.5$$

where IL_{AVG} is the average inductor current.

Switching MOSFET Selection

The switching MOSFET (N1) should have a voltage rating sufficient to withstand the maximum output voltage together with the diode drop of rectifier diode D1, and any possible overshoot due to ringing caused by parasitic inductances and capacitances. Use a MOSFET with a drain-to-source voltage rating higher than that calculated by the following equations:

Boost configuration:

$$V_{DS} = (V_{LED} + V_D) \times 1.2$$

Buck-boost configuration:

$$V_{DS} = (V_{LED} + V_{INMAX} + V_D) \times 1.2$$

where V_{LED} is the LED string voltage, V_{INMAX} is the maximum input voltage, and V_D is the forward drop of the rectifier diode. The factor 1.2 provides 20% safety margin.

Dimming MOSFET Selection

Select a dimming MOSFET (P1) with continuous current rating at the operating temperature higher than the LED current by 30%. The drain-to-source voltage rating of the dimming MOSFET must be higher than V_{LED} by 20%.

Dimming MOSFET Slew Rate Control

Filter capacitors placed on the drain side (LED side) of the P1 pMOS dimming FET may cause a current spike from the output capacitor when the dimming FET turns on. If the current spike is large enough, it may trigger the short-circuit protection of the MAX20090/MAX20090B. To reduce these current spike amplitudes, the turn-on slew rate of the dimming FET can be reduced. Slew-rate control of the P1 dimming MOSFET may be achieved by adding a resistor RG in series with the gate, and a capacitor CG across the gate and drain.

Choose RG = 10kΩ and CG according to the following equation:

$$CG = (C_{LED} \times R_{CS\_LED} \times (7V - V_{THDIM})/(0.25 \times V_{CS\_LIMIT} \times RG)$$

Where C_{LED} = Total capacitance (capacitance across LEDs + EMI filter capacitance) on the drain side of the dimming FET

R_{CS_LED} = LED current-sense resistor

V_{THDIM} = Threshold voltage of the DIMFET pMOS

V_{CS_LIMIT} = Current-limit threshold

The diode DR should be added across RG to enable fast turn-off of the DIMFET during LED short-fault conditions. Because the ISENSE+ sensing input is also the supply rail for the DIMOUT driver, any high-impedance component (such as a Ferrite Bead) in series with the ISENSE+ input is not recommended. For a typical application, RG = 10kΩ and CG = 1nF is sufficient. See Figure 1.

Feedback Compensation

The LED current-control loop comprising the switching converter, LED current amplifier, and the error amplifier should be compensated for stable control of the LED current. The switching converter small-signal transfer function has a right half-plane (RHP) zero for both boost and buck-boost configurations, as the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate. The easiest way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

Boost configuration:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

Buck-boost configuration:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

where f_{ZRHP} is in hertz, V_{LED} is in volts, L is the inductance value of L1 in henries (H), and I_{LED} is in amperes.

The switching converter small-signal transfer function also has an output pole for both boost and buck-boost configurations. The effective output impedance that determines the output pole frequency together with the output filter capacitance is calculated as:

Boost configuration:

$$R_{OUT} = \frac{(R_{LED} + R_{CS\_LED}) \times V_{LED}}{(R_{LED} + R_{CS\_LED}) \times I_{LED} + V_{LED}}$$

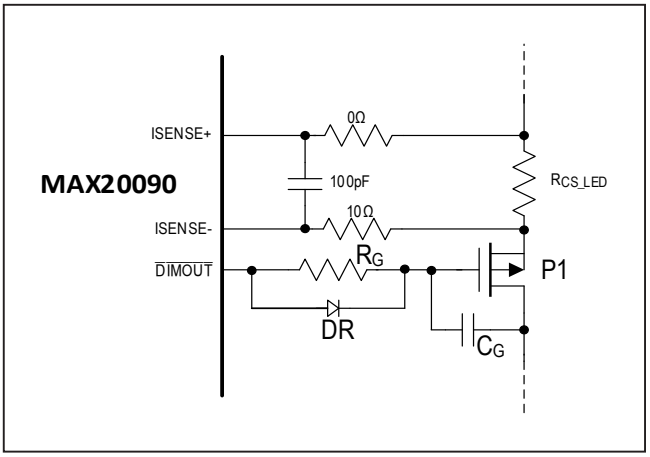


Figure 1. DIMFET Circuit

Buck-boost configuration:

$$R_{OUT} = \frac{(R_{LED} + R_{CS\_LED}) \times V_{LED}}{(R_{LED} + R_{CS\_LED}) \times I_{LED} \times D_{MAX} + V_{LED}}$$

where R_{LED} is the dynamic impedance of the LED string at the operating current in ohms, R_{CS_LED} is the LED current-sense resistor in ohms, V_{LED} is in volts, and I_{LED} is in amperes.

The output pole frequency for both boost and buck-boost configurations is calculated as follows:

$$f_P = \frac{1}{2\pi \times C_{OUT} \times R_{OUT}}$$

where f_P is in hertz, C_{OUT} is the output filter capacitance in farads, and R_{OUT} is the effective output impedance in ohms calculated above.

The feedback-loop compensation is done by connecting a resistor (R_{COMP}) and capacitor (C_{COMP}) in series from COMP to GND. R_{COMP} is chosen to set the high-frequency integrator gain for fast transient response, while C_{COMP} is chosen to set the integrator zero to maintain loop stability. For optimum performance, choose the components using the following equations:

$$f_C = 0.2 \times f_{ZRHP}$$

$$R_{COMP} = \frac{2 \times f_{ZRHP} \times R_{CS\_FET}}{f_C \times (1 - D_{MAX}) \times R_{CS\_LED} \times 5 \times G_M}$$

The value of C_{COMP} can be calculated as:

$$C_{COMP} = \frac{25}{\pi \times f_{ZRHP} \times R_{COMP}}$$

High-Side Buck Compensation

The high-side buck configuration does not have a right half-plane zero to avoid, so in most cases a single capacitor from COMP to GND will suffice to compensate the loop. Calculate C_{COMP} ccording to the following equation:

$$C_{COMP} = \frac{G_M \times A_V \times R_{CS_{LED}}}{2\pi \times f_C \times R_{CS_{FET}}}$$

Where C_{COMP} is the compensation capacitor value in nF, G_M is the G_M amplifier transconductance in µA/V, AV is the LED current-sense voltage gain, and f_C is the desired crossover frequency in kHz. Choose a crossover frequency that is lower than f_{SW}/15.

The output pole is set by the dynamic resistance of the LED string and the C_{OUT} capacitor.

$$f_{POUT} = \frac{1}{2\pi \times R_{DYN} \times C_{OUT}}$$

If the output pole is within a decade of the crossover frequency, then it can be compensated by adding a resistor, R_{COMP}, in series with C_{COMP}.

$$R_{COMP} = \frac{C_{OUT}}{C_{COMP}} \times R_{DYN}$$

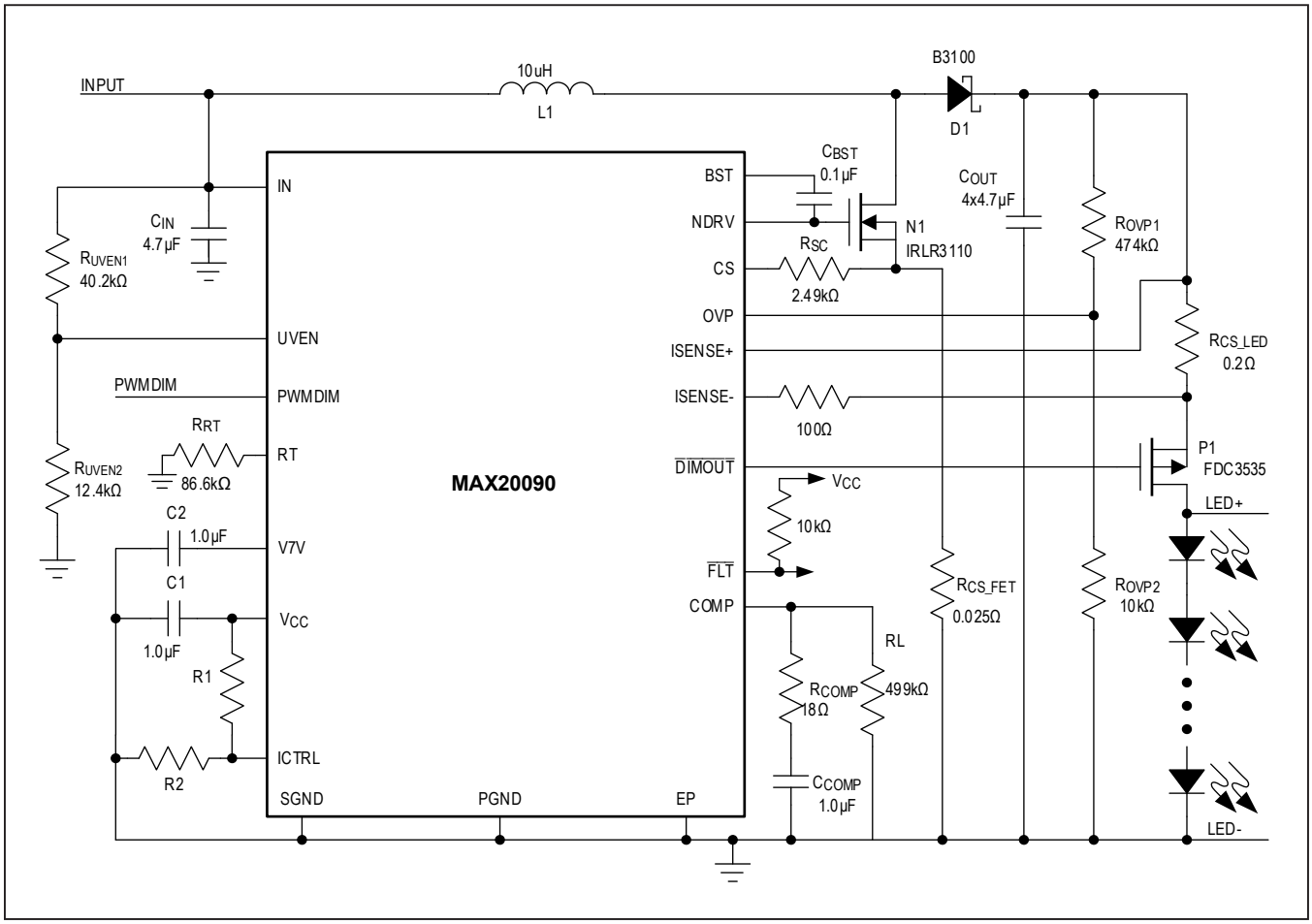
PCB Layout

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET connected to the device drain presents a dv/dt source; therefore, minimize the surface area of the heatsink as much as is compatible with the MOSFET power dissipation, or shield it. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use ground planes for best results.

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

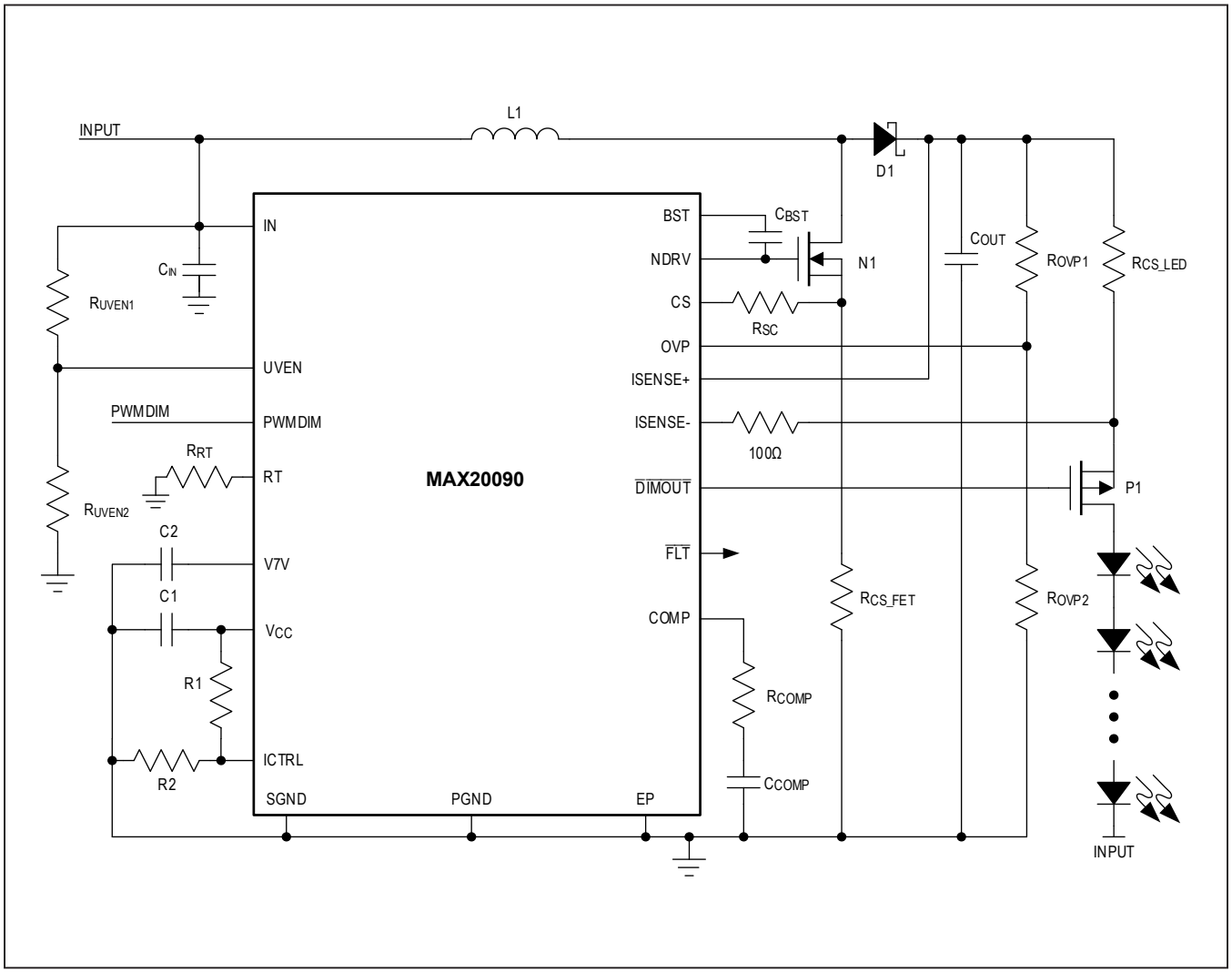
1) Use a large contiguous copper plane under the IC package. Ensure that all heat-dissipating components have adequate cooling.
2) Isolate the power components and high-current path from the sensitive analog circuitry.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Keep switching loops short:
   a) The anode of D1 must be connected very close to the drain of MOSFET N1.
   b) The cathode of D1 must be connected very close to C_{OUT}.
   c) C_{OUT} and current-sense resistor R4 must be connected directly to the ground plane.
4) Connect PGND and SGND to a star-point configuration.
5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick-copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
6) Route high-speed switching nodes away from the sensitive analog areas. Use an internal PCB layer for the PGND and SGND plane as an EMI shield to keep radiated noise away from the device, feedback dividers, and analog bypass capacitors.

Typical Operating Circuit



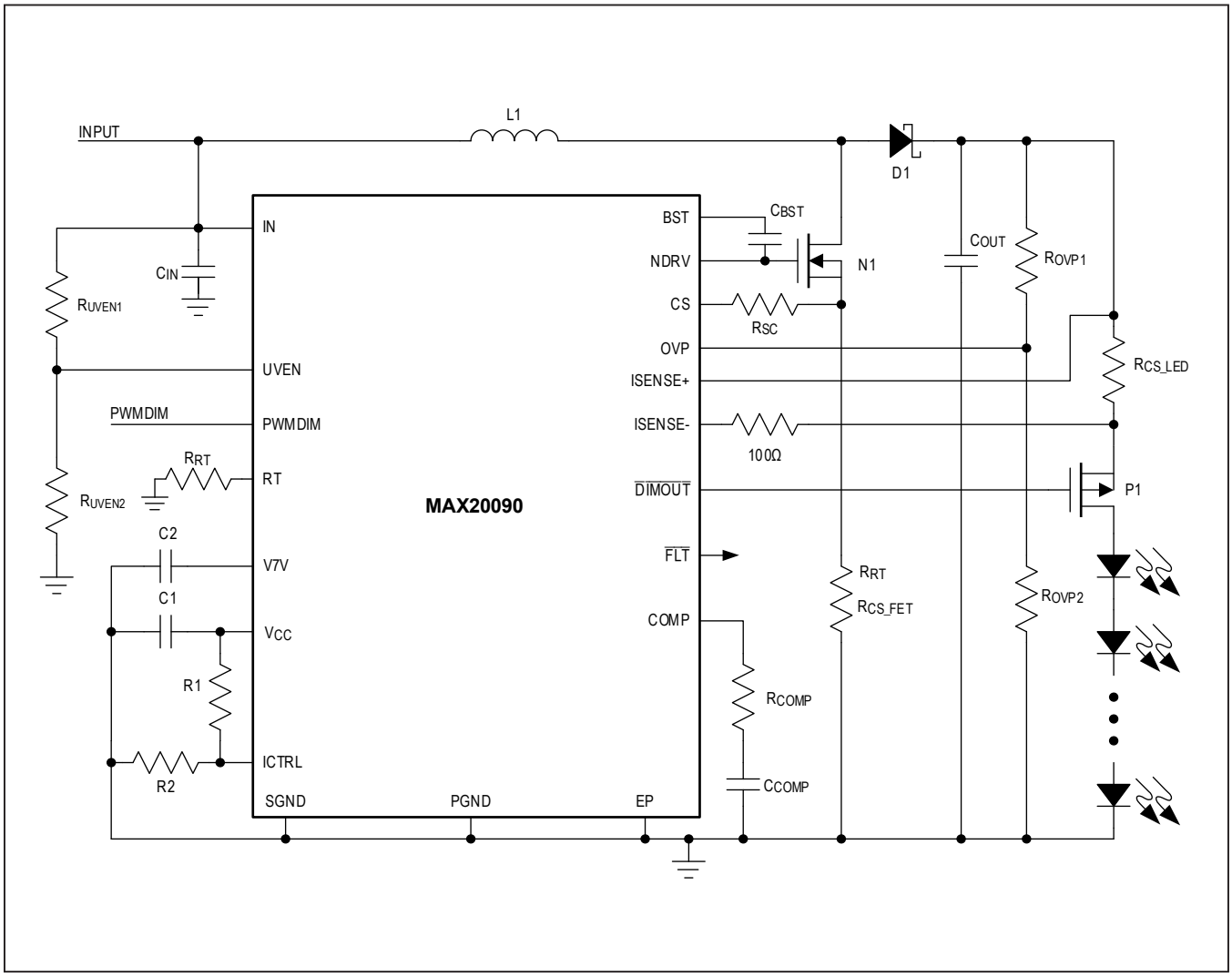
Typical Application Circuits

Buck-Boost LED Driver Using the MAX20090



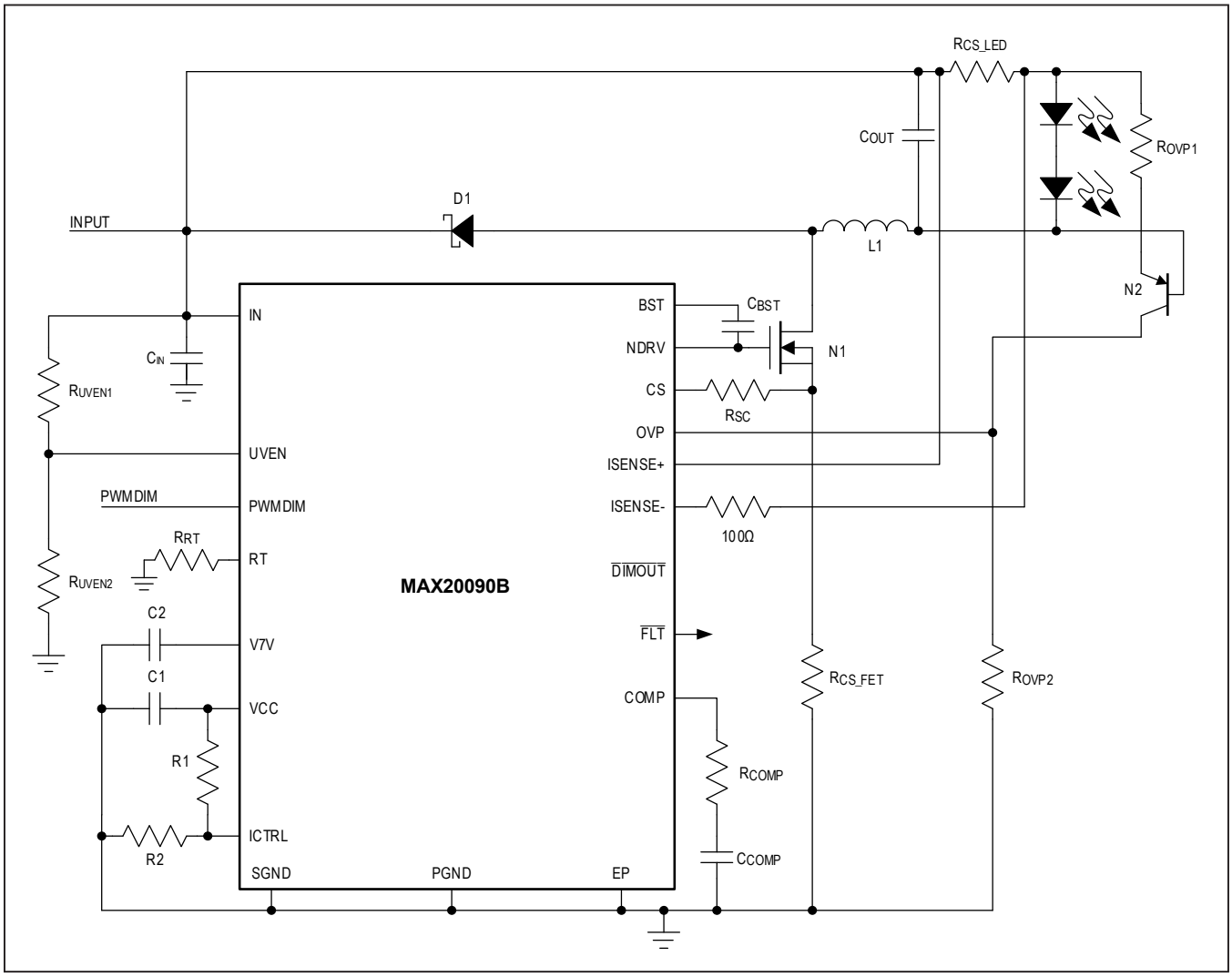
Typical Application Circuits (continued)

Boost LED Driver Using the MAX20090



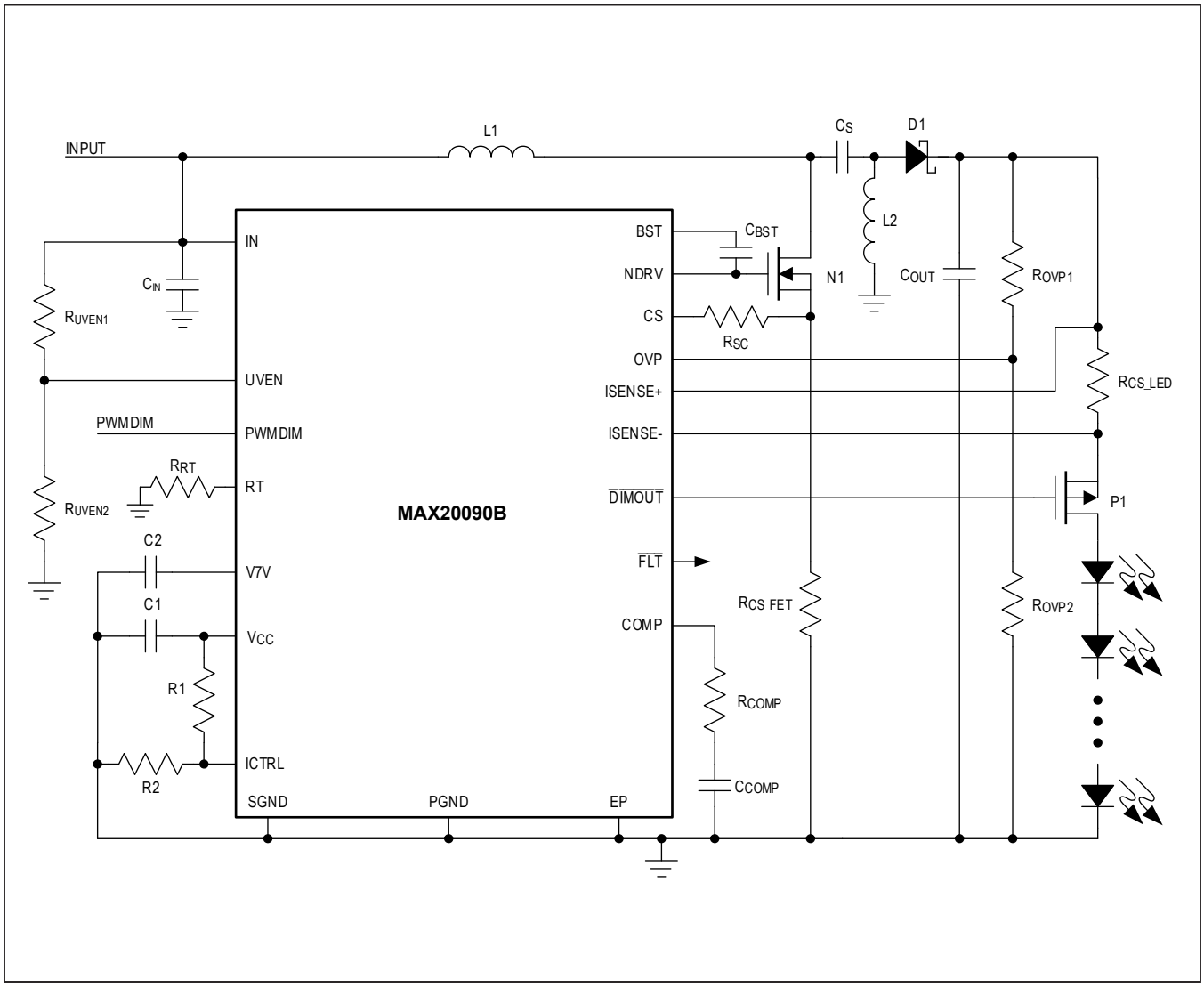
Typical Application Circuits (continued)

High-Side Buck LED Driver Using the MAX20090



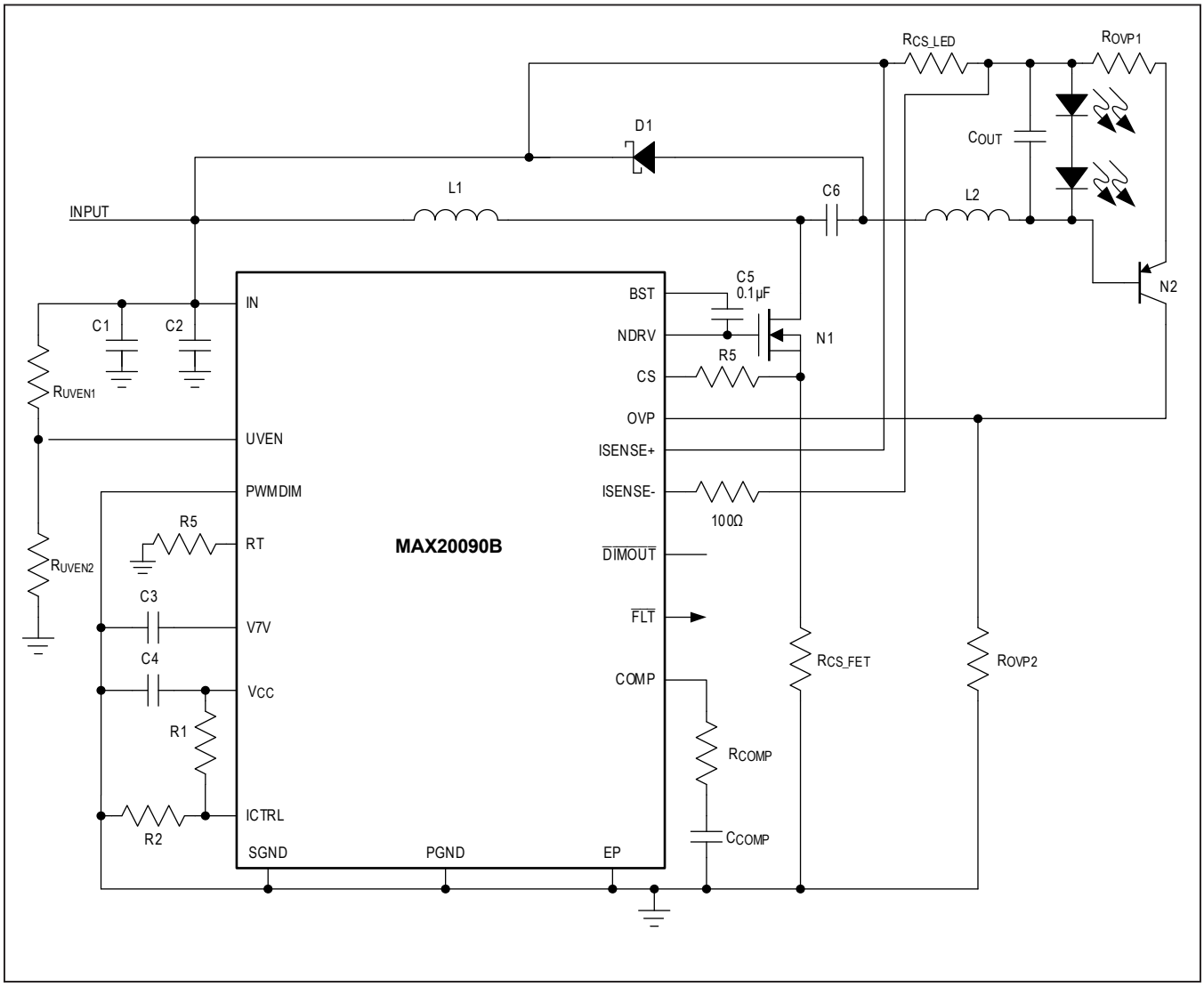
Typical Application Circuits (continued)

SEPIC LED Driver Using the MAX20090



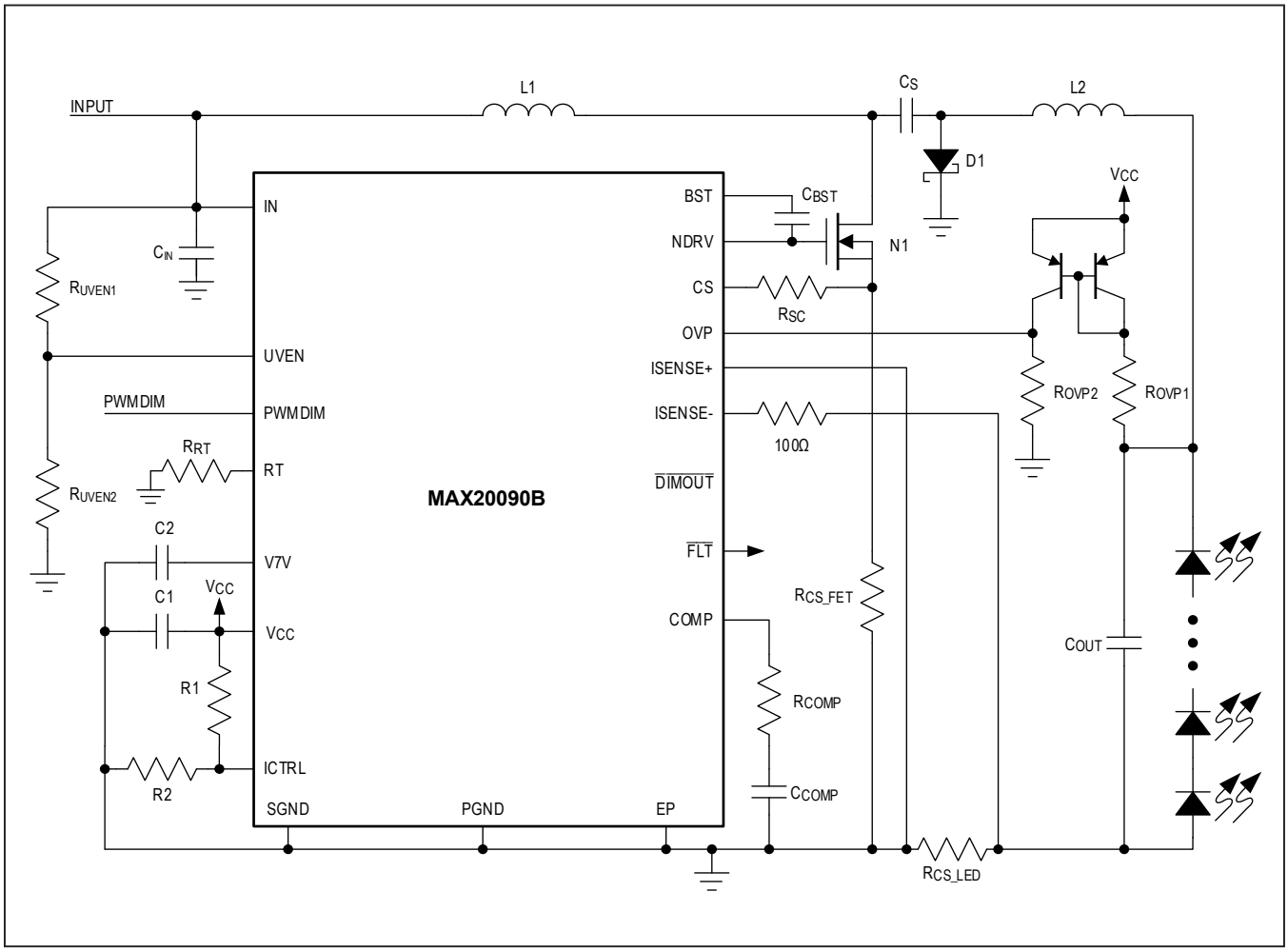
Typical Application Circuits (continued)

Zeta Converter LED Driver using the MAX20090



Typical Application Circuits (continued)

Ćuk Converter LED Driver using the MAX20090



Ordering Information

PART	DESCRIPTION	PIN-PACKAGE
MAX20090ATP/V+	No filter before hiccup mode	20 TQFN-EP*
MAX20090ATP/VY+	No filter before hiccup mode	20 TQFN-EP (SW)*
MAX20090AUP/V+	No filter before hiccup mode	20 TSSOP-EP*
MAX20090AUPA/V+	1µs filter before hiccup mode	20 TSSOP-EP*
MAX20090AUPB/V+	No hiccup mode	20 TSSOP-EP*
MAX20090BATP/V+	No filter before hiccup mode/SEPIC configuration applications	20 TQFN-EP*
MAX20090BATP/VY+	No filter before hiccup mode/SEPIC configuration applications	20 TQFN-EP (SW)*
MAX20090BAUP/V+	No filter before hiccup mode/SEPIC configuration applications	20 TSSOP-EP*

Note: *All parts operate over the -40°C to +125°C automotive temperature range.*

/V denotes an automotive-qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
(SW) = Side wettable.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2044+4C	21-100172	90-0409
20 TQFN-EP (SW)	T2044Y+4C	21-100068	90-0409
20 TSSOP-EP	U20E+3C	21-100132	90-100049

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/17	Initial release	—
1	6/17	Changed data sheet title and deleted tape-and-reel variants from *Ordering Information*	1–29
2	7/17	Removed future product designation in *Ordering Information* from the MAX20090ATP/VY+	28
3	4/18	Removed future product designation in *Ordering Information* from the MAX20090AUP/V+	28
4	1/19	Added MAX20090B to data sheet title, updated *Simplified Typical Operating Circuit, Simplified Schematic, Electrical Characteristics, Typical Operating Characteristics, Pin Configurations, Block Diagram, Detailed Description, Applications Information, Typical Operating Circuits,* and *Ordering Information*	1–29
5	5/19	Added MAX20090BATP/V+ to *Ordering Information*	28
6	4/20	Updated *Typical Operating Characteristics* and *Detailed Description*	8, 19, 20
7	6/20	Updated *Detailed Description* and *Ordering Information*	14, 27
8	1/21	Updated *Pin Configurations*	9

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