

256-Tap, μ PoT, Low-Drift, Digital Potentiometer

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND-0.3V to +6V
 DIN, SCLK, $\overline{\text{CS}}$ to GND-0.3V to +6V
 H, L, W to GND-0.3V to (V_{DD} + 0.3)
 Maximum Continuous Current into Pins H, L, and W1mA
 Continuous Power Dissipation (T_A = +70°C)
 8-Pin μ MAX (derate 4.1mW/°C above +70°C)330mW

Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_H = V_{DD}, V_L = 0, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------|---|-----------------------|-----------------------|------|--------|
| DC PERFORMANCE (Voltage-Divider Mode) | | | | | | |
| Resolution | N | | 8 | | | Bits |
| Integral Nonlinearity (Notes 1, 2) | INL | | | | ±1/2 | LSB |
| Differential Nonlinearity (Notes 1, 2) | DNL | | | | ±1 | LSB |
| End-to-End Resistor Tempco | TC _R | | | 35 | | ppm/°C |
| Ratiometric Resistor Tempco | | | | 5 | | ppm/°C |
| Full-Scale Error | | | | -6 | | LSB |
| Zero-Scale Error | | | | +6 | | LSB |
| DC PERFORMANCE (Variable-Resistor Mode) | | | | | | |
| Resolution | N | | 8 | | | Bits |
| Integral Nonlinearity (Notes 1, 3) | INL | V _{DD} = +5V | | | ±1 | LSB |
| | | V _{DD} = +3V | | | ±3 | LSB |
| Differential Nonlinearity (Notes 1, 3) | DNL | V _{DD} = +5V | | | ±1/2 | LSB |
| | | V _{DD} = +3V | | | ±1/2 | LSB |
| DC PERFORMANCE (Resistor Characteristics) | | | | | | |
| Wiper Resistance (Note 4) | R _W | V _{DD} = +5V | | 275 | | Ω |
| | | V _{DD} = +3V | | | 550 | |
| Wiper Capacitance | C _W | | | 46 | | pF |
| End-to-End Resistance | R _{HL} | | 7.5 | 10 | 12.5 | kΩ |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage | V _{IH} | | 0.7 × V _{DD} | | | V |
| Input Low Voltage | V _{IL} | | | 0.3 × V _{DD} | | V |
| Input Leakage Current | | | | ±1.0 | | μA |
| Input Capacitance | | | | 5 | | pF |
| TIMING CHARACTERISTICS (ANALOG) | | | | | | |
| Wiper-Settling Time | t _s | To 50% of final value from code 0 to code 128 | | 100 | | ns |
| TIMING CHARACTERISTICS (DIGITAL) (Note 5) (Figure 2) | | | | | | |
| SCLK Clock Period | t _{CP} | | 100 | | | ns |
| SCLK Pulse Width High | t _{CH} | | 40 | | | ns |

256-Tap, μ PoT, Low-Drift, Digital Potentiometer

MAX5402

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +5V$, $V_H = V_{DD}$, $V_L = 0$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $V_{DD} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|-----------|--|------------------|-----|-----|-----|---------|
| SCLK Pulse Width Low | t_{CL} | | | 40 | | | ns |
| \overline{CS} Fall to SCLK Rise Setup Time | t_{CSS} | | | 40 | | | ns |
| SCLK Rise to \overline{CS} Rise Hold Time | t_{CSH} | | | 0 | | | ns |
| DIN Setup Time | t_{DS} | | | 40 | | | ns |
| DIN Hold Time | t_{DH} | | | 0 | | | ns |
| SCLK Rise to \overline{CS} Fall Delay | t_{CS0} | | | 10 | | | ns |
| \overline{CS} Rise to SCLK Rise Hold | t_{CS1} | | | 40 | | | ns |
| \overline{CS} Pulse Width High | t_{CSW} | | | 100 | | | ns |
| POWER SUPPLIES | | | | | | | |
| Supply Voltage | V_{DD} | | | 2.7 | | 5.5 | V |
| Supply Current | I_{DD} | $\overline{CS} = SCLK =$ DIN = V_{DD} | $V_{DD} = +5V$ | | 0.8 | 5 | μA |
| | | | $V_{DD} = +2.7V$ | | 0.1 | | μA |

Note 1: Linearity is defined in terms of the H-to-L code-dependent resistance.

Note 2: The DNL and INL are measured with the potentiometer configured as a voltage-divider with $H = V_{DD}$ and $L = 0$. The wiper terminal is unloaded and measured with an ideal voltmeter.

Note 3: The DNL and INL are measured with the potentiometer configured as a variable resistor. H is unconnected and $L = 0$. The wiper terminal is driven with a source current of $200\mu A$ at $V_{DD} = +3V$ and $400\mu A$ at $V_{DD} = +5V$.

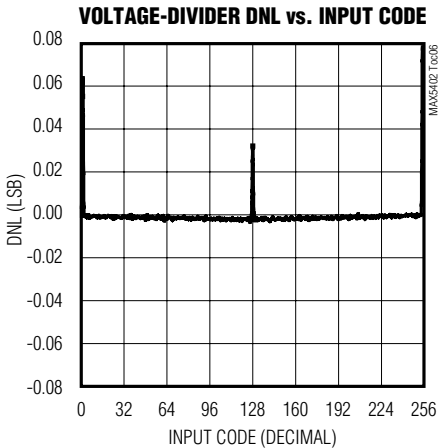
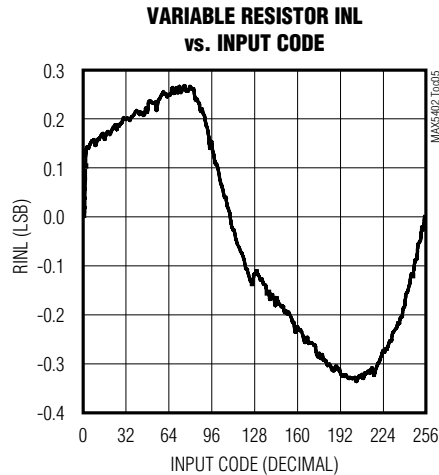
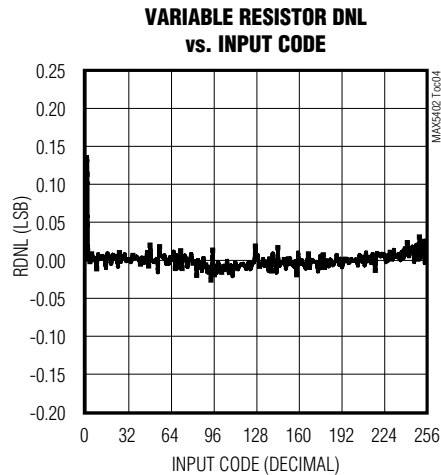
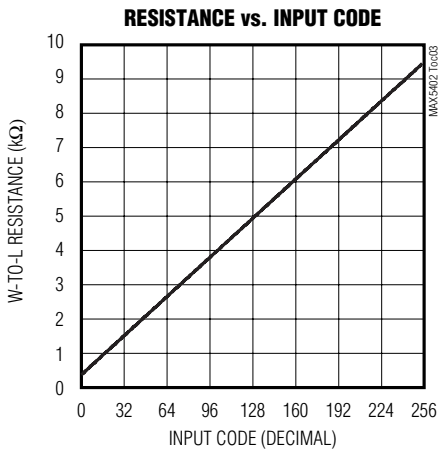
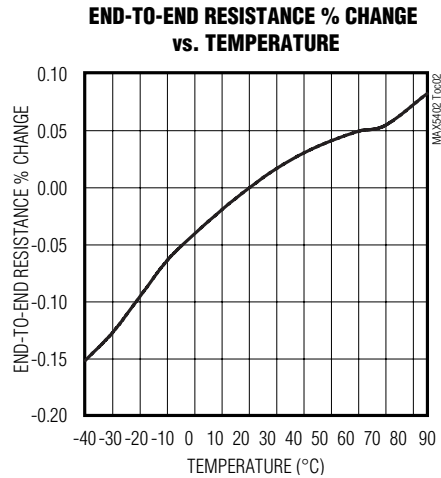
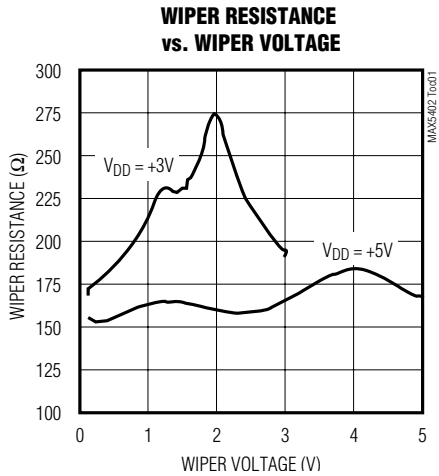
Note 4: The wiper resistance is the worst value measured, injecting a current, $I_W = V_{DD}/R_{HL}$ into terminal W.

Note 5: Digital timing is guaranteed by design.

256-Tap, μ PoT, Low-Drift, Digital Potentiometer

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

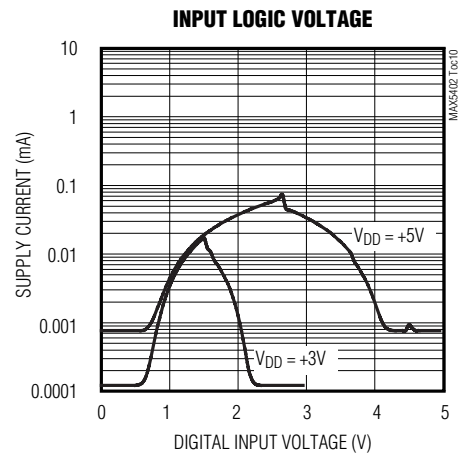
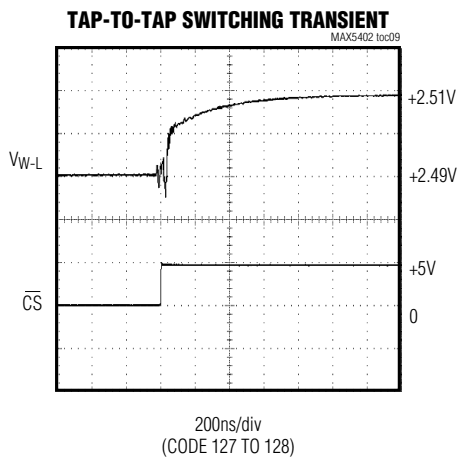
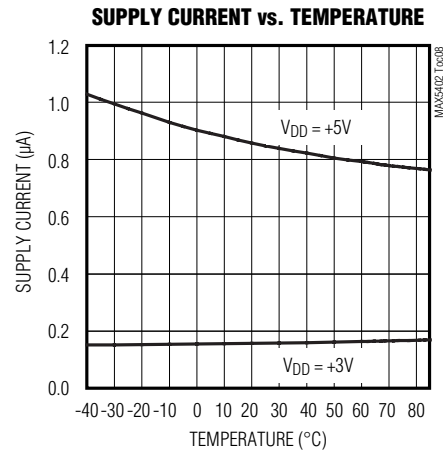
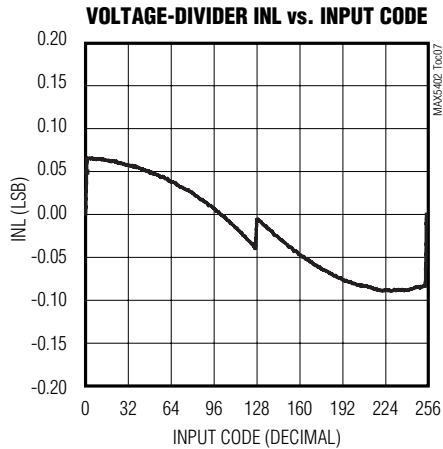


256-Tap, μ PoT, Low-Drift, Digital Potentiometer

MAX5402

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

| PIN | NAME | FUNCTION |
|-----|------------------------|---|
| 1 | L | Low Terminal of Resistor |
| 2 | GND | Ground |
| 3 | $\overline{\text{CS}}$ | Chip Select Input |
| 4 | DIN | Serial Data Input |
| 5 | SCLK | Serial Clock Input |
| 6 | V_{DD} | Power Supply. Bypass with a 0.1 μF capacitor to GND. |
| 7 | W | Wiper Terminal |
| 8 | H | High Terminal of Resistor |

256-Tap, μ PoT, Low-Drift, Digital Potentiometer

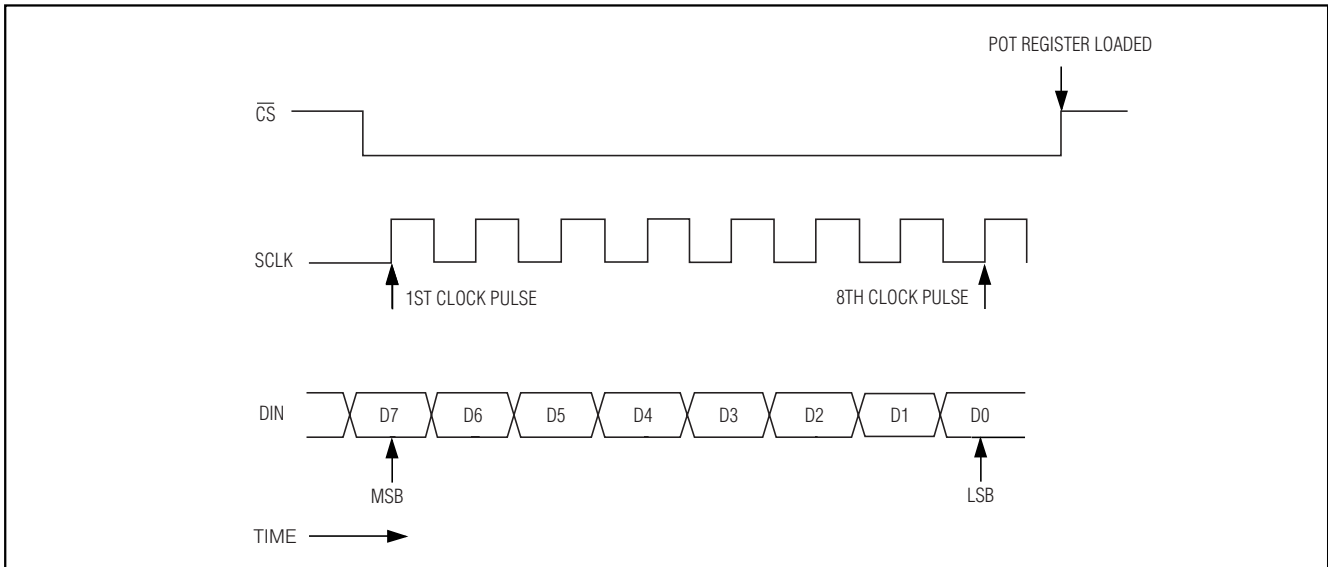


Figure 1. Serial Interface Timing Diagram

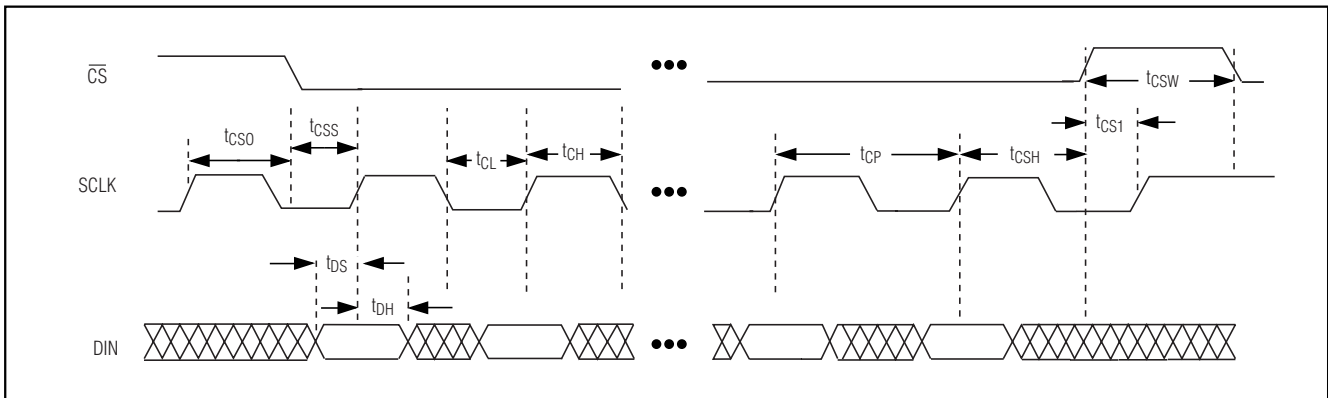


Figure 2. Detailed Serial Interface Timing Diagram

Detailed Description

The MAX5402 consists of 255 fixed resistors in series between pins H and L. The potentiometer wiper (pin W) can be programmed to access any one of the 256 different tap points on the resistor string. The MAX5402 has an SPI-compatible 3-wire serial data interface to control the wiper tap position. This write-only interface contains three inputs: Chip Select (\overline{CS}), Data In (DIN), and Data Clock (SCLK). When \overline{CS} is taken low, data from the DIN pin is synchronously loaded into the 8-bit serial shift register on the rising edge of each SCLK pulse (Figure 1). The MSB is shifted in first, as shown in Figure 3. Note that if \overline{CS} is not kept low during the entire data stream, the data will be corrupted and the device

will need to be reloaded. After all 8 data bits have been loaded into the shift register, they are latched into the decoder once \overline{CS} is taken high. The decoder switches the potentiometer wiper to the tap position that corresponds to the 8-bit input data. Each resistor cell is $10k\Omega/255$ or 39.2Ω for the MAX5402.

The MAX5402 features POR circuitry. This sets the wiper to the midscale position at power-up by loading a binary value of 128 into the 8-bit latch. The MAX5402 can be used as a variable resistor by connecting pin W to either pin H or L.

256-Tap, μ PoT, Low-Drift, Digital Potentiometer

MAX5402

| Data Word | B0 (D7) | B1 (D6) | B2 (D5) | B3 (D4) | B4 (D3) | B5 (D2) | B6 (D1) | B7 (D0) |
|-----------------------|---------|---------|---------|---------|---------|---------|---------|----------------------|
| (MSB) First Bit In | | | | | | | | (LSB) Last Bit In |

Figure 3. Serial Data Format

Applications Information

The MAX5402 is intended for a variety of circuits where accurate, fine-tuned adjustable resistance is required, such as in adjustable voltage or adjustable gain circuit configurations. The MAX5402 is used in either a potentiometer divider or a variable resistor configuration.

Adjustable Current to Voltage Converter

Figure 4 shows the MAX5402 used with a MAX4250 low-noise op amp to precisely tune a current-to-voltage converter. Pins H and W of the MAX5402 are connected to the node between R3 and R2, and pin L is connected to ground.

Adjustable Gain Amplifier

The MAX5402 is used again with the MAX4250 to make a digitally adjustable gain circuit as shown in Figure 5. The normal feedback resistor is replaced with the MAX5402 in a variable resistor configuration, so that the gain of the circuit can be digitally controlled.

Adjustable Voltage Reference

In Figure 6, the MAX5402 is shown with the MAX6160 to make an adjustable voltage reference. In this circuit, the H pin of the MAX5402 is connected to the OUT pin of the MAX6160, the L pin of the MAX5402 is connected to GND, and the W pin of the MAX5402 is connected to the ADJ pin of the MAX6160. The MAX5402 allows precise tuning of the voltage reference output. A low 5ppm/ $^{\circ}$ C ratiometric tempco allows a very stable adjustable voltage overtemperature.

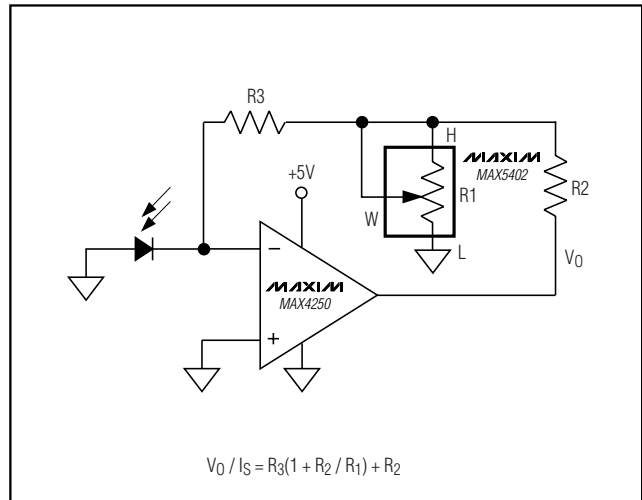


Figure 4. I to V Converter

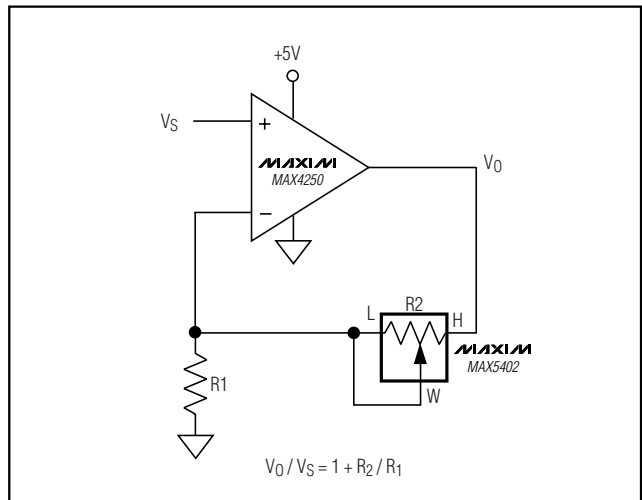


Figure 5. Noninverting Amplifier

256-Tap, μ PoT, Low-Drift, Digital Potentiometer

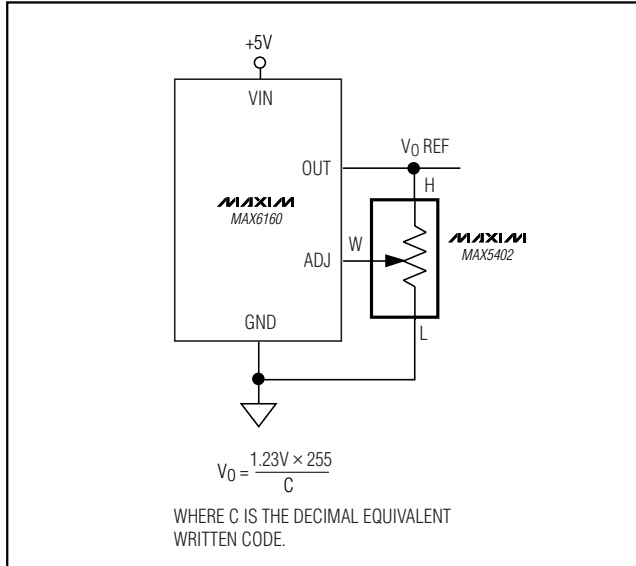


Figure 6. Adjustable Voltage Reference

Chip Information

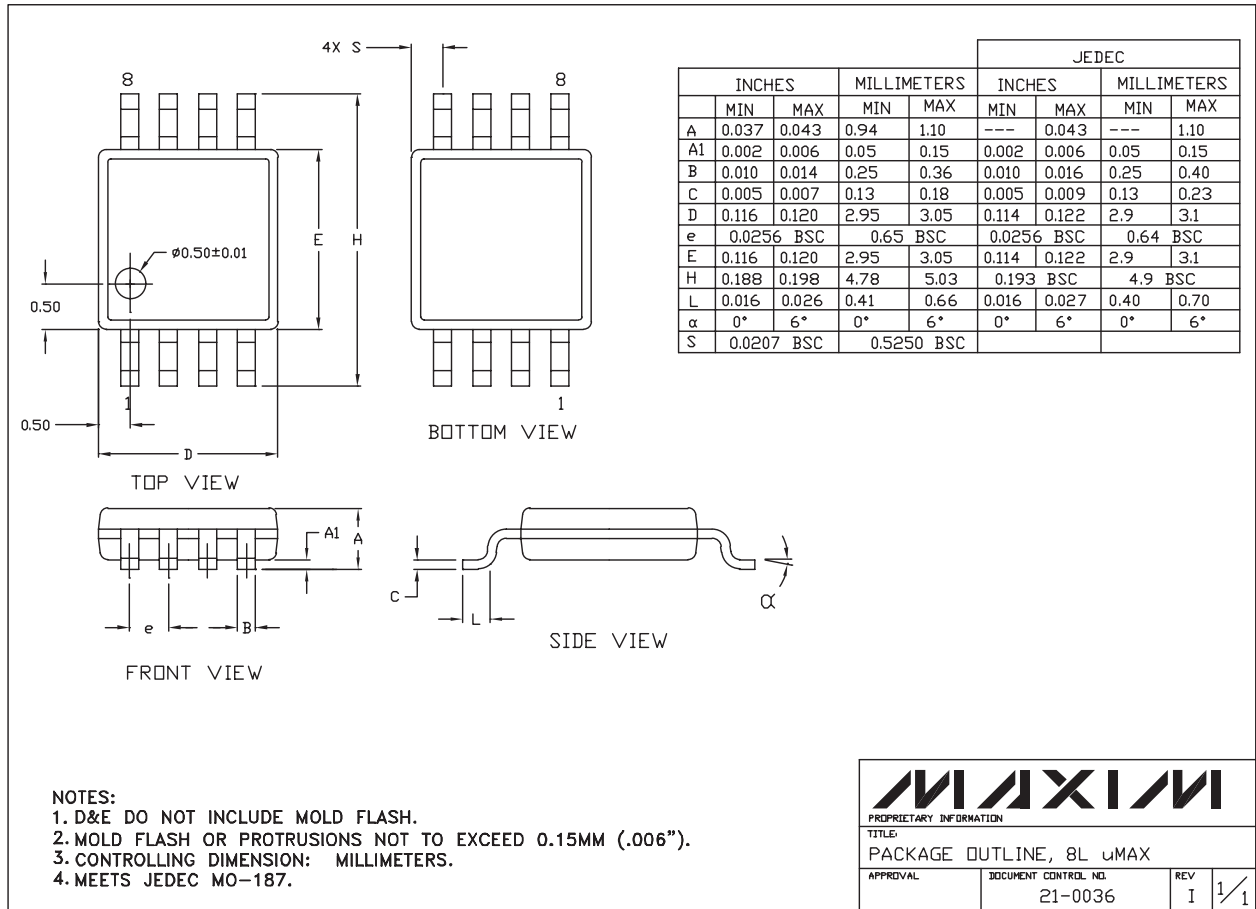
TRANSISTOR COUNT: 3475

PROCESS: BiCMOS

256-Tap, μ PoT, Low-Drift, Digital Potentiometer

Package Information

MAX5402



8LUMAXD:EPS

MAXIM
 PROPRIETARY INFORMATION
 TITLE:
 PACKAGE OUTLINE, 8L μ MAX
 APPROVAL: _____ DOCUMENT CONTROL NO: 21-0036 REV: I 1/1

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