

Absolute Maximum Ratings

V _{CC} to GND	-0.3V to +6.0V	Continuous Power Dissipation (T _A = +70°C)
RESET Open-Drain Output	-0.3V to +6.0V	3-Pin SC70 (derate 2.9mW/°C above +70°C).....
RESET, RESET (push-pull output)	-0.3V to (V _{CC} + 0.3V)	4-Pin SC70 (derate 3.1mW/°C above +70°C).....
MR, RESET IN	-0.3V to (V _{CC} + 0.3V)	6-Pin μDFN (derate 2.1mW/°C above +70°C)
Input Current (V _{CC}).....	20mA	Operating Temperature Range.....
Output Current (all pins).....	20mA	Storage Temperature Range.....
		Lead Temperature (soldering, 10s)
		Soldering Temperature (reflow).....

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

3 SC70

Package Code	X3+2
Outline Number	21-0075
Land Pattern Number	90-0208
THERMAL RESISTANCE, MULTILAYER BOARD	
Junction to Ambient (θ _{JA})	340.4°C/W
Junction to Case (θ _{JC})	120°C/W

4 SC70

Package Code	X4+1
Outline Number	21-0098
Land Pattern Number	90-0187
THERMAL RESISTANCE, MULTILAYER BOARD	
Junction to Ambient (θ _{JA})	322.6°C/W
Junction to Case (θ _{JC})	115°C/W

6 FDFN

Package Code	L611+1
Outline Number	21-0147
Land Pattern Number	90-0080
THERMAL RESISTANCE, MULTILAYER BOARD	
Junction to Ambient (θ _{JA})	477°C/W
Junction to Case (θ _{JC})	122°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{CC} = full range, T_A = -40°C to $+125^{\circ}\text{C}$, unless otherwise specified. Typical values are at T_A = $+25^{\circ}\text{C}$.) (Note 1)

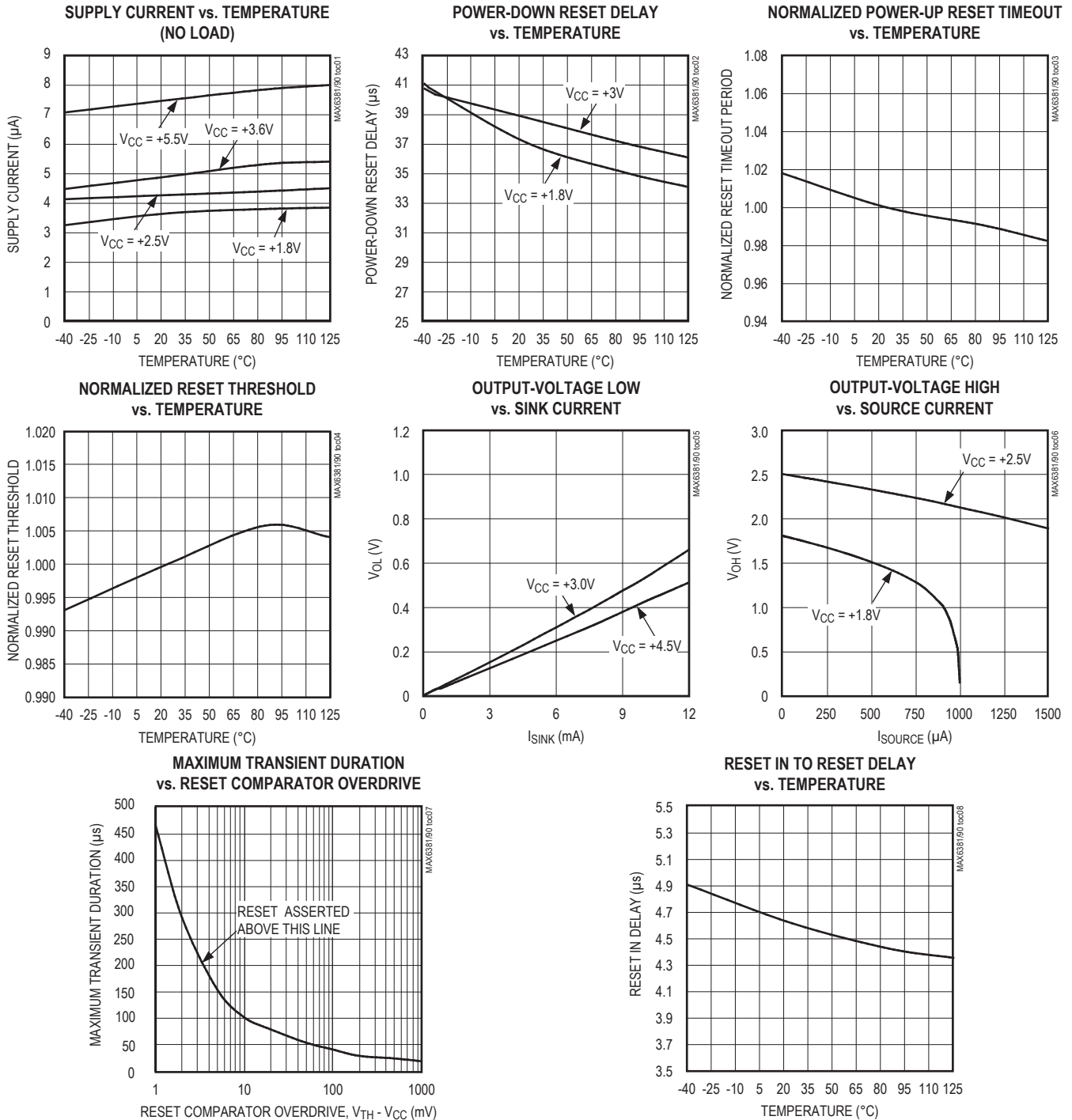
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Voltage Range	V_{CC}		1.0		5.5	V	
V_{CC} Supply Current	I_{CC}	V_{CC} = 5.5V, no load		7	13	μA	
		V_{CC} = 3.6V, no load		6	11		
		V_{CC} = 2.5V, no load		4	7		
		V_{CC} = 1.8V, no load		3	6		
V_{CC} Reset Threshold (See Reset Thresholds table)	V_{TH}	T_A = $+25^{\circ}\text{C}$	$V_{TH} - 1.5\%$	V_{TH}	$V_{TH} + 1.5\%$	V	
		T_A = -40°C to $+125^{\circ}\text{C}$	$V_{TH} - 2.5\%$	V_{TH}	$V_{TH} + 2.5\%$		
Reset Threshold Tempco	$\Delta V_{TH}/^{\circ}\text{C}$			60		ppm/ $^{\circ}\text{C}$	
V_{CC} to Reset Delay		V_{CC} falling at 10mV/ μs from $V_{TH} + 100\text{mV}$ to $V_{TH} - 100\text{mV}$		35		μs	
Reset Timeout Period MAX6381–MAX6389 (See Reset Timeout table)	t_{RP}	D1		1	2	ms	
		D2		20	40		
		D3		140	280		
		D5		280	560		
		D6		560	1120		
		D4		1120	2240		
		D7		1200	2400		
Reset Timeout Period MAX6390	t_{RP}	$\overline{\text{MR}}$ timeout period	D4		140	280	ms
			D7		150	300	
		V_{CC} timeout period	D4		1120	2240	
			D7		1200	2400	
$\overline{\text{MR}}$ Input Voltage	V_{IL}	$V_{TH} < 4\text{V}$			$0.3 \times V_{CC}$	V	
	V_{IH}			$0.7 \times V_{CC}$			
	V_{IL}	$V_{TH} > 4\text{V}$			0.8		
	V_{IH}			2.4			

Electrical Characteristics (continued)(V_{CC} = full range, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{MR}}$ Minimum Input Pulse Width			1			μs
$\overline{\text{MR}}$ Glitch Rejection				100		ns
$\overline{\text{MR}}$ to Reset Delay				200		ns
$\overline{\text{MR}}$ Internal Pullup Resistance		MAX6381–MAX6389	32	63	100	k Ω
		MAX6390	500	1560	3000	Ω
RESET IN Input Threshold	V _{THRST}	T _A = +25°C	1.245	1.27	1.295	V
		T _A = 0°C to +85°C	1.232		1.308	
		T _A = -40°C to +125°C	1.219		1.321	
RESET IN to RESET Delay		V _{RESETIN} falling at 4mV/ μs from V _{THRST} + 40mV to V _{THRST} - 40mV		4.5		μs
RESET IN Input Leakage Current	I _{RESET IN}		-50	± 1	+50	nA
Open-Drain $\overline{\text{RESET}}$ Output Voltage	V _{OL}	V _{CC} \geq 4.5V, I _{SINK} = 3.2mA, reset asserted			0.4	V
		V _{CC} \geq 2.5V, I _{SINK} = 1.2mA, reset asserted			0.3	
		V _{CC} \geq 1.0V, I _{SINK} = 80 μ A, reset asserted			0.3	
Open-Drain $\overline{\text{RESET}}$ Output Leakage Current	I _{LKG}	V _{CC} > V _{TH} , $\overline{\text{RESET}}$ not asserted			1.0	μA
Push-Pull $\overline{\text{RESET}}$ Output Voltage	V _{OL}	V _{CC} \geq 4.5V, I _{SINK} = 3.2mA, reset asserted			0.4	V
		V _{CC} \geq 2.5V, I _{SINK} = 1.2mA, reset asserted			0.3	
		V _{CC} \geq 1.0V, I _{SINK} = 80 μ A, reset asserted			0.3	
	V _{OH}	V _{CC} \geq 4.5V, I _{SOURCE} = 800 μ A, reset not asserted	0.8 x	V _{CC}		
		V _{CC} \geq 2.5V, I _{SOURCE} = 500 μ A, reset not asserted	0.8 x	V _{CC}		
Push-Pull RESET Output Voltage	V _{OH}	V _{CC} \geq 4.5V, I _{SOURCE} = 800 μ A, reset asserted	0.8 x	V _{CC}		
		V _{CC} \geq 2.5V, I _{SOURCE} = 500 μ A, reset asserted	0.8 x	V _{CC}		
		V _{CC} \geq 1.8V, I _{SOURCE} = 150 μ A, reset asserted	0.8 x	V _{CC}		
		V _{CC} \geq 1.0V, I _{SOURCE} = 1 μ A, reset asserted	0.8 x	V _{CC}		
	V _{OL}	V _{CC} \geq 4.5V, I _{SINK} = 3.2mA, reset not asserted			0.4	
V _{CC} \geq 2.5V, I _{SINK} = 1.2mA, reset not asserted				0.3		

Note 1: Specifications over temperature are guaranteed by design, not production tested.

Typical Operating Characteristics



Pin Description

μ DFN	PIN						NAME	FUNCTION
	3-PIN SC70		4-PIN SC70					
	MAX6381/ MAX6383	MAX6382	MAX6384/ MAX6386/ MAX6390	MAX6385	MAX6387/ MAX689	MAX6388		
1 (MAX6382/ MAX6385/ MAX6388)		2	—	2	—	2	RESET	Active-High Push-Pull Reset Output. RESET changes from low to high when any monitored voltage (V_{CC} or $V_{RESETIN}$) drops below the reset threshold or \overline{MR} is pulled low. RESET remains high for the reset timeout period after monitored voltages exceed the reset thresholds or \overline{MR} is released.
1 (MAX6381/ MAX6383/ MAX6384/ MAX6386/ MAX6387/ MAX6390)	2	—	2	—	2	—	\overline{RESET}	Active-Low Open-Drain/Push-Pull Reset Output. \overline{RESET} changes from high to low when any monitored voltage (V_{CC} or $V_{RESETIN}$) drops below the reset threshold or \overline{MR} is pulled low. \overline{RESET} remains low for the reset timeout period after the monitored voltages exceed the reset thresholds or \overline{MR} is released. Open-drain requires an external pullup resistor.
2, 3, 5 (MAX6381/ MAX6382/ MAX6383)	—	—	—	—	—	—	N.C.	No Connection. Not Internally connected.
2, 5 (MAX6384– MAX6390)								
3 (MAX6384/ MAX6385/ MAX6386/ MAX6390)	—	—	3	3	—	—	\overline{MR}	Active-Low Manual Reset Input. Drive low to force a reset. Reset remains active as long as \overline{MR} is low and for the reset timeout period after \overline{MR} is released. Leave unconnected or connect to V_{CC} if unused. \overline{MR} has an internal 63k Ω (1.56k Ω for MAX6390) pullup resistor to V_{CC} .
3 (MAX6387/ MAX6388/ MAX6389)	—	—	—	—	3	3	RESET IN	Auxiliary Reset Input. High-impedance input to the auxiliary reset comparator. Connect RESET IN to the center point of an external resistor voltage-divider network to set the reset threshold voltage. Reset asserts when either V_{CC} or RESET IN falls below its threshold voltage.
4 (MAX6381– MAX6390)	3	3	4	4	4	4	V_{CC}	Supply Voltage for the device and input for fixed V_{CC} reset threshold monitor.
6 (MAX6381– MAX6390)	1	1	1	1	1	1	GND	Ground

Detailed Description

RESET Output

A μ P reset input starts the μ P in a known state. These μ P supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

Reset asserts when V_{CC} is below the reset threshold; once V_{CC} exceeds the reset threshold, an internal timer keeps the reset output asserted for the reset timeout period. After this interval, reset output deasserts. Reset output is guaranteed to be in the correct logic state for $V_{CC} \geq 1V$.

Manual Reset Input (MAX6384/ MAX6385/MAX6386/MAX6390)

Many μ P-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on \overline{MR} asserts reset. Reset remains asserted while \overline{MR} is low, and for the reset active timeout period (t_{RP}) after \overline{MR} returns high. This input has an internal 63k Ω pullup resistor (1.56k Ω for MAX6390), so it can be left unconnected if it is not used. \overline{MR} can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from \overline{MR} to GND to create a manual-reset function; external debounce circuitry is not required. If \overline{MR} is driven from long cables or if the device is used in a noisy environment, connecting a 0.1 μ F capacitor from \overline{MR} to GND provides additional noise immunity.

RESET IN Comparator (MAX6387/MAX6388/MAX6389)

RESET IN is compared to an internal +1.27V reference. If the voltage at RESET IN is less than 1.27V, reset asserts. Use the RESET IN comparator as a user-adjustable reset detector or as a secondary power-supply monitor by implementing a resistor-divider at RESET IN (shown in Figure 1). Reset asserts when either V_{CC} or RESET IN falls below its respective threshold voltage. Use the following equation to set the threshold:

$$V_{INTH} = V_{THRST} (R1/R2 + 1)$$

where $V_{THRST} = +1.27V$. To simplify the resistor selection, choose a value of $R2$ and calculate $R1$:

$$R1 = R2 [(V_{INTH}/V_{THRST}) - 1]$$

Since the input current at RESET IN is 50nA (max), large values can be used for $R2$ with no significant loss in accuracy.

Reset Thresholds (-40°C to +125°C)

SUFFIX	V_{TH} (min)	V_{TH} (nom)	V_{TH} (max)
46	4.51	4.63	4.74
45	4.39	4.50	4.61
44	4.27	4.38	4.48
43	4.19	4.30	4.41
42	4.10	4.20	4.31
41	4.00	4.10	4.20
40	3.90	4.00	4.10
39	3.80	3.90	4.00
38	3.71	3.80	3.90
37	3.61	3.70	3.79
36	3.51	3.60	3.69
35	3.41	3.50	3.59
34	3.32	3.40	3.49
33	3.22	3.30	3.38
32	3.12	3.20	3.28
31	3.00	3.08	3.15
30	2.93	3.00	3.08
29	2.85	2.93	3.00
28	2.73	2.80	2.87
27	2.63	2.70	2.77
26	2.56	2.63	2.69
25	2.44	2.50	2.56
24	2.34	2.40	2.46
23	2.26	2.31	2.37
22	2.13	2.19	2.24
21	2.05	2.10	2.15
20	1.95	2.00	2.05
19	1.85	1.90	1.95
18	1.76	1.80	1.85
17	1.62	1.67	1.71
16	1.54	1.58	1.61

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the μ P during power-up, power-down, and brownout conditions, the MAX6381–MAX6390 are relatively immune to short duration negative-going V_{CC} transients (glitches).

The *Typical Operating Characteristics* section shows the Maximum Transient Durations vs. Reset Comparator Overdrive, for which the MAX6381–MAX6390 do not generate a reset pulse. This graph was generated using

MAX6381–MAX6390

SC70/ μ DFN, Single/Dual Low-Voltage, Low-Power μ P Reset Circuits

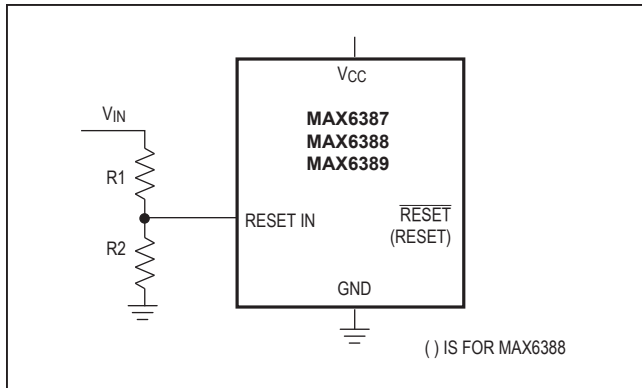


Figure 1. RESET IN Configuration

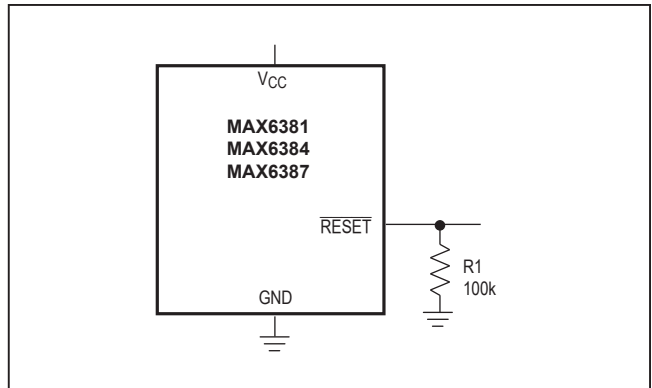


Figure 2. RESET Valid to V_{CC} = Ground Circuit

Reset Timeout Delay

SUFFIX	MIN
D1	1ms
D2	20ms
D3	140ms
D5	280ms
D6	560ms
D4	1120ms
D7	1200ms
MAX6390__D4	1120/140ms*
MAX6390__D7	1200/150ms*

*The MAX6390 has a 1120ms or 1200ms \overline{RESET} timeout and a 140ms or 150ms manual reset timeout.

a negative-going pulse applied to V_{CC} , starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going V_{CC} transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1 μ F capacitor mounted as close as possible to V_{CC} provides additional transient immunity.

Ensuring a Valid RESET Output Down to V_{CC} = 0V

The MAX6381–MAX6390 are guaranteed to operate properly down to V_{CC} = 1V. In applications that require valid reset levels down to V_{CC} = 0V, a pull-down resistor to active-low outputs (push/pull only, Figure 2) and a pullup resistor to active-high outputs (push/pull only) will

ensure that the reset line is valid while the reset output can no longer sink or source current. This scheme does not work with the open-drain outputs of the MAX6383/MAX6386/MAX6389/MAX6390. The resistor value used is not critical, but it must be small enough not to load the reset output when V_{CC} is above the reset threshold. For most applications, 100k Ω is adequate.

Standard Versions

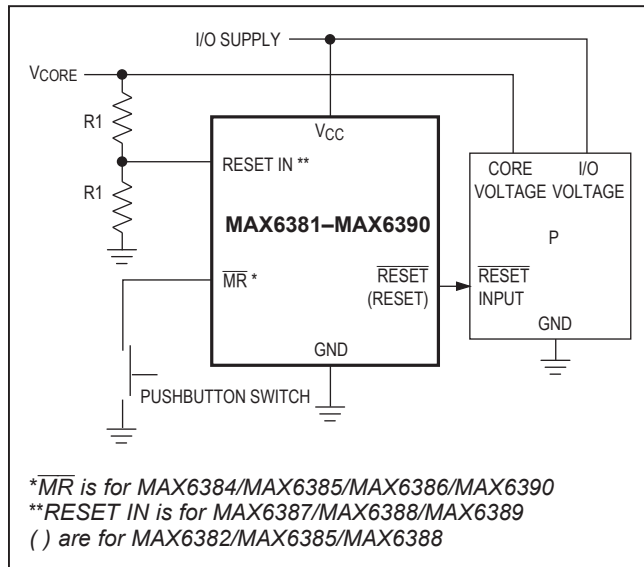
PART	RESET THRESHOLD	RESET TIMEOUT
MAX638_	46	D3
	44	
	31	
	29	
	26	
	23	
	22	
	17	
	16	
MAX6390	46	D4
	44	
	31	
	29	
	26	
	23	
	22	
	17	
	16	

Selector Guide

PART NUMBER	PUSH-PULL ACTIVE-LOW	PUSH-PULL ACTIVE-HIGH	OPEN-DRAIN ACTIVE-LOW	MANUAL RESET INPUT MR	RESET IN
MAX6381	X				
MAX6382		X			
MAX6383			X		
MAX6384	X			X	
MAX6385		X		X	
MAX6386			X	X	
MAX6390*			X	X	
MAX6387	X				X
MAX6388		X			X
MAX6389			X		X

*The MAX6390 offers a V_{CC} reset timeout of 1120ms or 1200ms (min) and a manual reset timeout of 140ms or 150ms (min).

Typical Operating Circuit



Ordering Information (continued)

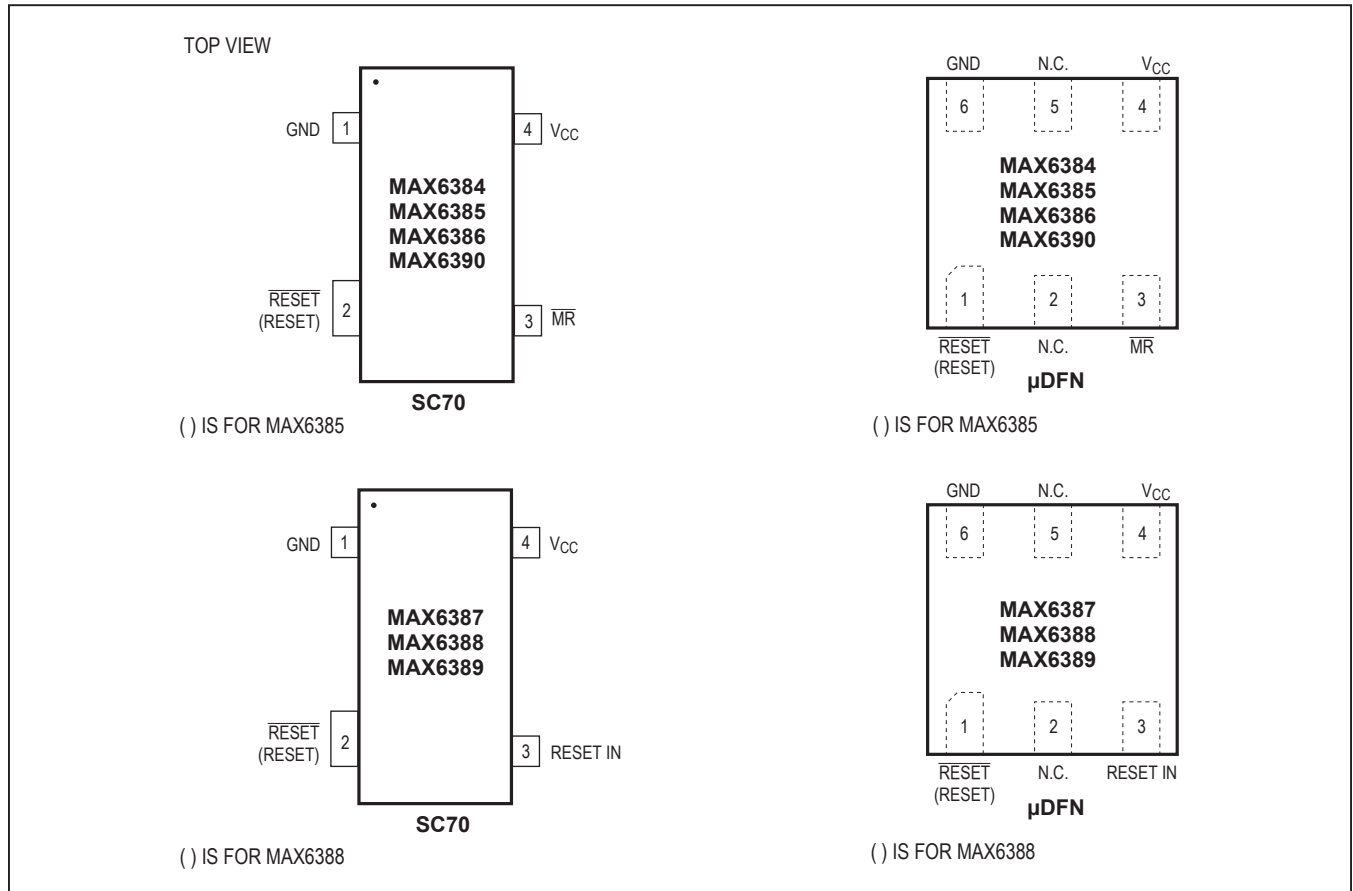
PART	TEMP RANGE	PIN-PACKAGE
MAX6382LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6382XR__D_+T	-40°C to +125°C	3 SC70
MAX6383LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6383XR__D_+T	-40°C to +125°C	3 SC70
MAX6384LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6384XS__D_+T	-40°C to +125°C	4 SC70
MAX6385LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6385XS__D_+T	-40°C to +125°C	4 SC70
MAX6386LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6386XS__D_+T	-40°C to +125°C	4 SC70
MAX6387LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6387XS__D_+T	-40°C to +125°C	4 SC70
MAX6388LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6388XS__D_+T	-40°C to +125°C	4 SC70
MAX6389LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6389XS__D_+T	-40°C to +125°C	4 SC70
MAX6389XS30D2/V+T	-40°C to +125°C	4 SC70
MAX6389XS31D1/V+T	-40°C to +125°C	4 SC70
MAX6389XS32D1/V+T	-40°C to +125°C	4 SC70
MAX6390LT__D_+T	-40°C to +125°C	6 μ DFN
MAX6390XS__D_+T*	-40°C to +125°C	4 SC70

Note: Insert reset threshold suffix (see Reset Threshold table) after “XR”, “XS”, or “LT.” Insert reset timeout delay (see Reset Timeout Delay table) after “D” to complete the part number. Sample stock is generally held on standard versions only (see Standard Versions table). Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability of nonstandard versions.

*MAX6390 is available with D4 or D7 timing only.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configurations (continued)



Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/00	Initial release	—
3	12/05	Added lead-free notation to <i>Ordering Information</i> .	1, 8
4	4/07	Added μ DFN package to data sheet.	1, 2, 5, 7–13
5	7/12	Added automotive package to <i>Ordering Information</i> .	1
6	3/18	Updated <i>Ordering Information</i> table	1, 8
7	8/20	Added <i>Package Information</i> table with thermal characteristics and removed <i>Package Information</i> table	2, 10

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[MAX6383LT27D6+T](#) [MAX6389XS25D3+T](#) [MAX6384XS43D7+T](#) [MAX6385LT32D2+T](#) [MAX6382XR26D7+T](#)
[MAX6388XS44D6+T](#) [MAX6387LT16D3+T](#) [MAX6384XS33D7+T](#) [MAX6382XR37D7+T](#) [MAX6382LT28D7+T](#)
[MAX6385LT35D1+T](#) [MAX6386XS27D5+T](#) [MAX6386XS29D6+T](#) [MAX6387XS34D5+T](#) [MAX6388LT36D1+T](#)
[MAX6386LT37D2+T](#) [MAX6389LT32D3+T](#) [MAX6383XR16D5+T](#) [MAX6387LT36D3+T](#) [MAX6383LT16D4+T](#)
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[MAX6381LT16D4+T](#) [MAX6381LT16D5+T](#) [MAX6381LT16D6+T](#) [MAX6381LT16D7+T](#) [MAX6381LT17D2+T](#)
[MAX6381LT17D3+T](#) [MAX6381LT17D4+T](#) [MAX6381LT17D5+T](#) [MAX6381LT17D6+T](#) [MAX6381LT17D7+T](#)
[MAX6381LT18D1+T](#) [MAX6381LT18D2+T](#) [MAX6381LT18D3+T](#) [MAX6381LT18D4+T](#) [MAX6381LT18D5+T](#)
[MAX6381LT18D6+T](#) [MAX6381LT18D7+T](#) [MAX6381LT19D1+T](#) [MAX6381LT19D2+T](#) [MAX6381LT19D3+T](#)
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[MAX6381LT20D7+T](#) [MAX6381LT21D1+T](#) [MAX6381LT21D2+T](#) [MAX6381LT21D3+T](#) [MAX6381LT21D4+T](#)
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