

# µP Supervisory Circuits in 4-Bump (2 × 2) Chip-Scale Package

## ABSOLUTE MAXIMUM RATINGS

All voltages measured with respect to GND, unless otherwise noted.

V <sub>CC</sub> .....	-0.3V to +6V
RESET, RESET (push-pull) .....	-0.3V to (V <sub>CC</sub> + 0.3V)
RESET (open-drain) .....	-0.3V to +6V
MR .....	-0.3V to (V <sub>CC</sub> + 0.3V)
Input/Output into Any Pin .....	20mA

Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
4-Bump UCSP (derate 3.8mW/°C above +70°C).....	303mW
Operating Temperature Range .....	-40°C to +85°C
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Bump Reflow Temperature .....	+235°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 1.0V to 5.5V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = 3.0V and T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Voltage Range	V <sub>CC</sub>	T <sub>A</sub> = 0°C to +70°C	1.0		5.5	V	
		T <sub>A</sub> = -40°C to +85°C	1.2		5.5		
Supply Current	I <sub>CC</sub>	MAX6400/MAX6401/MAX6402 V <sub>CC</sub> = 3.0V for V <sub>TH</sub> ≤ 2.93V, V <sub>CC</sub> = 3.2V for V <sub>TH</sub> ≥ 2.93V, no load		0.5	1.0	µA	
		V <sub>CC</sub> = 5.5V, no load		1.0	1.75		
Reset Threshold	V <sub>TH</sub>	Table 1	T <sub>A</sub> = +25°C	V <sub>TH</sub> - 1.5%	V <sub>TH</sub>	V <sub>TH</sub> + 1.5%	V
			T <sub>A</sub> = -40°C to +85°C	V <sub>TH</sub> - 2.5%	V <sub>TH</sub>	V <sub>TH</sub> + 2.5%	
Reset Threshold Hysteresis		MAX6400/MAX6401/MAX6402		6.3		mV	
		MAX6403/MAX6404/MAX6405		9.5			
Reset Threshold Tempco	ΔV <sub>TH</sub> /°C			40		ppm/°C	
V <sub>CC</sub> to Reset Delay	t <sub>RD</sub>	V <sub>CC</sub> = (V <sub>TH</sub> + 100mV) to (V <sub>TH</sub> - 100mV)		20		µs	
Reset Active Timeout Period	t <sub>RP</sub>		100	185	280	ms	
MR Input	V <sub>IL</sub>	V <sub>TH</sub> > 4.0V			0.8	V	
	V <sub>IH</sub>		2.0				
	V <sub>IL</sub>	V <sub>TH</sub> ≤ 4.0V			0.2 × V <sub>CC</sub>		
	V <sub>IH</sub>		0.7 × V <sub>CC</sub>				
MR Minimum Input Pulse Width	t <sub>MD</sub>		1			µs	
MR Glitch Rejection				100		ns	
MR to Reset Delay Time				200		ns	
MR Pullup Resistance			25	50	75	kΩ	

# μP Supervisory Circuits in 4-Bump (2 × 2) Chip-Scale Package

**MAX6400-MAX6405**

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = 1.0V to 5.5V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = 3.0V and T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET Output Voltage Low (MAX6400/MAX6402/MAX6403/ MAX6405)	V <sub>OL</sub>	I <sub>SINK</sub> = 1.6mA, V <sub>CC</sub> ≥ 2.1V, reset asserted			0.3	V
		I <sub>SINK</sub> = 100μA, V <sub>CC</sub> ≥ 1.2V, reset asserted			0.4	
RESET Output Voltage High (MAX6400/MAX6403)	V <sub>OH</sub>	I <sub>SOURCE</sub> = 500μA, V <sub>CC</sub> = 3.2V, MAX6400, only, reset not asserted	0.8 × V <sub>CC</sub>			V
		I <sub>SOURCE</sub> = 800μA, V <sub>CC</sub> = 4.5V, V <sub>TH</sub> ≤ 4.38V, reset not asserted	0.8 × V <sub>CC</sub>			
		I <sub>SOURCE</sub> = 800μA, V <sub>CC</sub> = V <sub>TH</sub> (max), V <sub>TH</sub> ≥ 4.5V, reset not asserted	0.8 × V <sub>CC</sub>			
RESET Output Voltage (MAX6401/MAX6404)	V <sub>OH</sub>	I <sub>SOURCE</sub> = 500μA, V <sub>CC</sub> ≥ 2.1V, reset asserted	0.8 × V <sub>CC</sub>			V
		I <sub>SOURCE</sub> = 50μA, V <sub>CC</sub> ≥ 1.2V, reset asserted	0.8 × V <sub>CC</sub>			
	V <sub>OL</sub>	I <sub>SINK</sub> = 1.2mA, V <sub>CC</sub> ≥ 3.2V, reset not asserted, MAX6401 only			0.3	
		I <sub>SINK</sub> = 3.2mA, V <sub>CC</sub> ≥ 4.5V, reset not asserted, V <sub>TH</sub> ≤ 4.38V			0.4	
		I <sub>SINK</sub> = 3.2mA, V <sub>CC</sub> = V <sub>TH</sub> (max), V <sub>TH</sub> ≥ 4.5V, reset not asserted			0.4	
Open-Drain RESET Output Leakage Current (Note 2)		RESET not asserted			0.1	μA

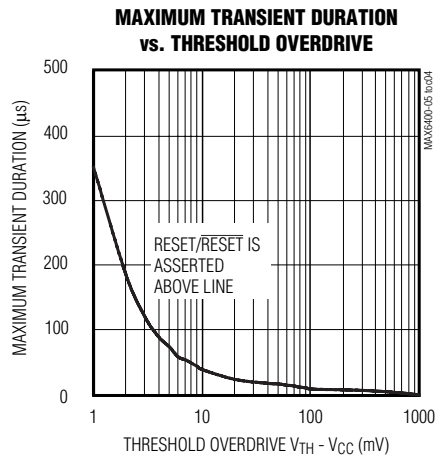
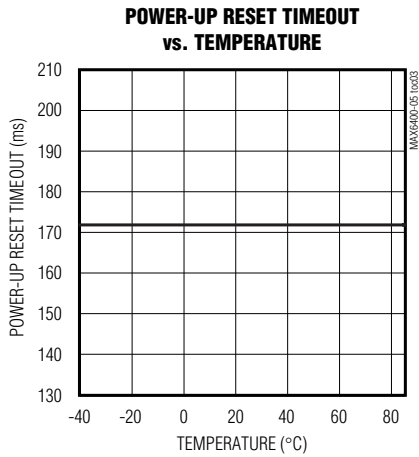
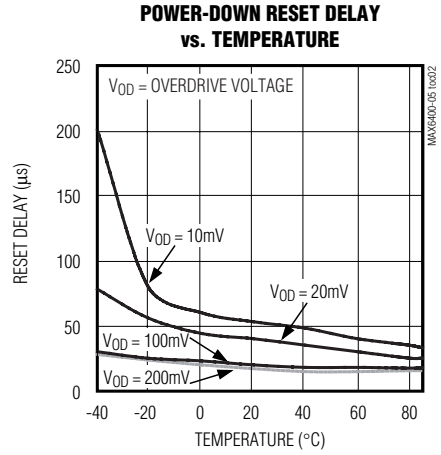
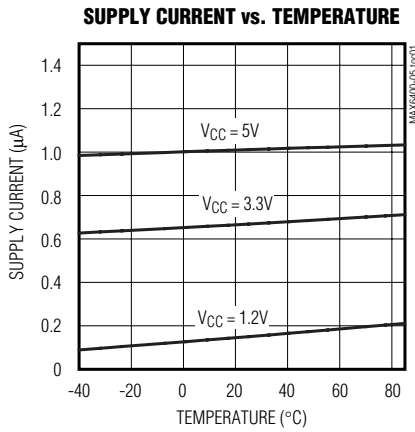
**Note 1:** Production testing done at +25°C only. Overtemperature limits are guaranteed by design and not production tested.

**Note 2:** Guaranteed by design.

# μP Supervisory Circuits in 4-Bump (2 × 2) Chip-Scale Package

## Typical Operating Characteristics

(T<sub>A</sub> = +25°C, unless otherwise noted.)



# μP Supervisory Circuits in 4-Bump (2 × 2) Chip-Scale Package

MAX6400-MAX6405

## Pin Description

PIN		NAME	FUNCTION
MAX6400/MAX6402 MAX6403/MAX6405	MAX6401/MAX6404		
A1	A1	GND	Ground
B1	—	$\overline{\text{RESET}}$	Active-Low Reset Output, (Open-Drain or Push-Pull). $\overline{\text{RESET}}$ is asserted low when the $V_{CC}$ input is below the selected reset threshold. $\overline{\text{RESET}}$ remains low for the reset timeout period after $V_{CC}$ exceeds the device reset threshold. Open-drain outputs require an external pullup resistor.
—	B1	RESET	Active-High Reset Output. RESET remains high while $V_{CC}$ is below the reset threshold and for at least 100ms after $V_{CC}$ rises above the reset threshold.
B2	B2	$\overline{\text{MR}}$	Active-Low Manual Reset. Internal 50kΩ pullup to $V_{CC}$ . Pull low to assert a reset. Reset remains asserted as long as $\overline{\text{MR}}$ is low and for the reset timeout period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to $V_{CC}$ if unused.
A2	A2	$V_{CC}$	Supply Voltage and Input for the Reset Threshold Monitor

## Detailed Description

### Reset Output

A microprocessor's (μP's) reset input starts the μP in a known state. These μP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

$\overline{\text{RESET}}$  is guaranteed to be a logic low for  $V_{CC}$  down to 1V. Once  $V_{CC}$  exceeds the reset threshold, an internal timer keeps  $\overline{\text{RESET}}$  low for the reset timeout period; after this interval,  $\overline{\text{RESET}}$  goes high.

If a brownout condition occurs ( $V_{CC}$  dips below the reset threshold),  $\overline{\text{RESET}}$  goes low. Any time  $V_{CC}$  goes below the reset threshold, the internal timer resets to zero, and  $\overline{\text{RESET}}$  goes low. The internal timer starts after  $V_{CC}$  returns above the reset threshold, and  $\overline{\text{RESET}}$  remains low for the reset timeout period.

The manual reset input ( $\overline{\text{MR}}$ ) can also initiate a reset, see the *Manual Reset Input* section. The MAX6401/MAX6404 have active-high RESET outputs that are the inverse of the MAX6400/MAX6402/MAX6403/MAX6405 outputs (Figure 1).

### Manual Reset Input

Many μP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuit to initiate a reset. A logic low on  $\overline{\text{MR}}$  asserts reset. Reset remains asserted while  $\overline{\text{MR}}$  is low, and for

the reset active timeout period ( $t_{RP}$ ) after  $\overline{\text{MR}}$  returns high. This input has an internal 50kΩ pullup resistor, so it can be left open if it is not used.  $\overline{\text{MR}}$  can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{\text{MR}}$  to GND to create a manual reset function; external debouncing circuitry is not required. If  $\overline{\text{MR}}$  is driven from long cables or if the device is used in a noisy environment, connect a 0.1μF capacitor from  $\overline{\text{MR}}$  to ground to provide additional noise immunity (see Figure 1).

## Applications Information

### Interfacing to μP with Bidirectional Reset Pins

Since the  $\overline{\text{RESET}}$  output on the MAX6402/MAX6405 is open-drain, these devices interface easily with (μPs) that have bidirectional reset pins. Connecting the μP supervisor's  $\overline{\text{RESET}}$  output directly to the microcontroller's (μC's)  $\overline{\text{RESET}}$  pin with a single pullup resistor allows either device to assert reset (Figure 2).

### Negative-Going VCC Transients

These devices are relatively immune to short-duration, negative-going  $V_{CC}$  transients (glitches).

The *Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Threshold Overdrive graph, for which reset pulses are not gener-

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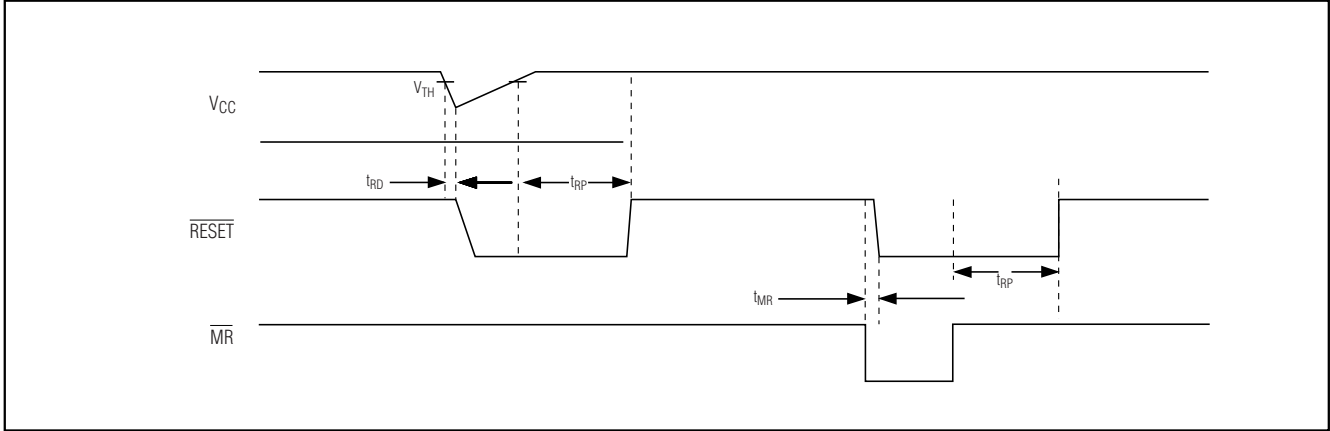


Figure 1. Reset Timing Diagram

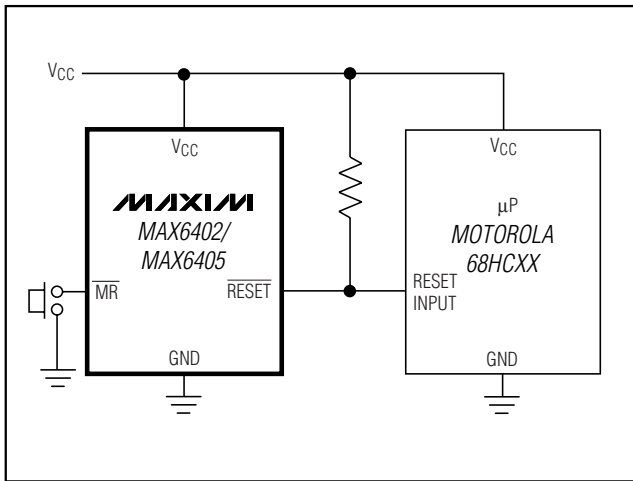


Figure 2. Interfacing to μPs with Bidirectional Reset Pins

ated. The graph shows the maximum pulse width that a negative going VCC transient may typically have when issuing a reset signal. As the amplitude of the transient increases, the maximum allowable pulse width decreases.

### Chip Information

TRANSISTOR COUNT: 512

PROCESS: BiCMOS

# μP Supervisory Circuits in 4-Bump (2 × 2) Chip-Scale Package

**MAX6400-MAX6405**

**Table 1. Factory Trimmed Reset Thresholds\***

PARTS	SUFFIX	Reset Threshold Voltage, V <sub>TH</sub> (V)				
		T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C	
		MIN	TYP	MAX	MIN	MAX
MAX6400BS MAX6401BS MAX6402BS	22*	2.167	2.200	2.233	2.145	2.250
	23*	2.285	2.320	2.355	2.262	2.375
	24	2.364	2.400	2.436	2.340	2.460
	25	2.462	2.500	2.537	2.437	2.562
	26*	2.591	2.630	2.669	2.564	2.692
	27	2.660	2.700	2.741	2.633	2.768
	28	2.758	2.800	2.842	2.730	2.870
	29*	2.886	2.930	2.974	2.857	3.000
	30	2.955	3.000	3.045	2.925	3.075
	31*	3.034	3.080	3.126	3.003	3.150
MAX6403BS MAX6404BS MAX6405BS	33	3.250	3.300	3.350	3.217	3.383
	34	3.349	3.400	3.451	3.315	3.485
	35	3.447	3.500	3.552	3.412	3.587
	36	3.546	3.600	3.654	3.510	3.690
	37	3.644	3.700	3.755	3.607	3.792
	38	3.743	3.800	3.857	3.705	3.895
	39	3.841	3.900	3.958	3.802	3.997
	40	3.940	4.000	4.060	3.900	4.100
	41	4.038	4.100	4.161	3.997	4.202
	42	4.137	4.200	4.263	4.095	4.305
	43	4.235	4.300	4.364	4.192	4.407
	44*	4.314	4.380	4.446	4.270	4.489
	45	4.432	4.500	4.567	4.387	4.612
	46*	4.560	4.630	4.699	4.514	4.746

Factory-trimmed voltage thresholds are available in approximately 100mV increments with a 1.5% room-temperature variance.

\*Note: Parts marked with an asterisk (\*) are standard versions.

## $\mu$ P Supervisory Circuits in 4-Bump (2 × 2) Chip-Scale Package

Table 2. Device Marking Codes

PARTS	TOP MARK	PARTS	TOP MARK	PARTS	TOP MARK
<b>MAX6400</b> BS31-T	AAJ	<b>MAX6401</b> BS31-T	ABV	<b>MAX6402</b> BS31-T	ACF
MAX6400BS30-T	AAI	MAX6401BS30-T	ABU	MAX6402BS30-T	ACE
MAX6400BS29-T	AAH	MAX6401BS29-T	ABT	MAX6402BS29-T	ACD
MAX6400BS28-T	AAG	MAX6401BS28-T	ABS	MAX6402BS28-T	ACC
MAX6400BS27-T	AAF	MAX6401BS27-T	ABR	MAX6402BS27-T	ACB
MAX6400BS26-T	AAE	MAX6401BS26-T	ABQ	MAX6402BS26-T	ACA
MAX6400BS25-T	AAD	MAX6401BS25-T	ABP	MAX6402BS25-T	ABZ
MAX6400BS24-T	AAC	MAX6401BS24-T	ABO	MAX6402BS24-T	ABY
MAX6400BS23-T	AAB	MAX6401BS23-T	ABN	MAX6402BS23-T	ABX
MAX6400BS22-T	AAA	MAX6401BS22-T	ABM	MAX6402BS22-T	ABW

PARTS	TOP MARK	PARTS	TOP MARK	PARTS	TOP MARK
<b>MAX6403</b> BS46-T	ACT	<b>MAX6404</b> BS46-T	ADH	<b>MAX6405</b> BS46-T	ADV
MAX6403BS45-T	ACS	MAX6404BS45-T	ADG	MAX6405BS45-T	ADU
MAX6403BS44-T	ACR	MAX6404BS44-T	ADF	MAX6405BS44-T	ADT
MAX6403BS43-T	ACQ	MAX6404BS43-T	ADE	MAX6405BS43-T	ADS
MAX6403BS42-T	ACP	MAX6404BS42-T	ADD	MAX6405BS42-T	ADR
MAX6403BS41-T	ACO	MAX6404BS41-T	ADC	MAX6405BS41-T	ADQ
MAX6403BS40-T	ACN	MAX6404BS40-T	ADB	MAX6405BS40-T	ADP
MAX6403BS39-T	ACM	MAX6404BS39-T	ADA	MAX6405BS39-T	ADO
MAX6403BS38-T	ACL	MAX6404BS38-T	ACZ	MAX6405BS38-T	ADN
MAX6403BS37-T	ACK	MAX6404BS37-T	ACY	MAX6405BS37-T	ADM
MAX6403BS36-T	ACJ	MAX6404BS36-T	ACX	MAX6405BS36-T	ADL
MAX6403BS35-T	ACI	MAX6404BS35-T	ACW	MAX6405BS35-T	ADK
MAX6403BS34-T	ACH	MAX6404BS34-T	ACV	MAX6405BS34-T	ADJ
MAX6403BS33-T	ACG	MAX6404BS33-T	ACU	MAX6405BS33-T	ADI

### UCSP Reliability

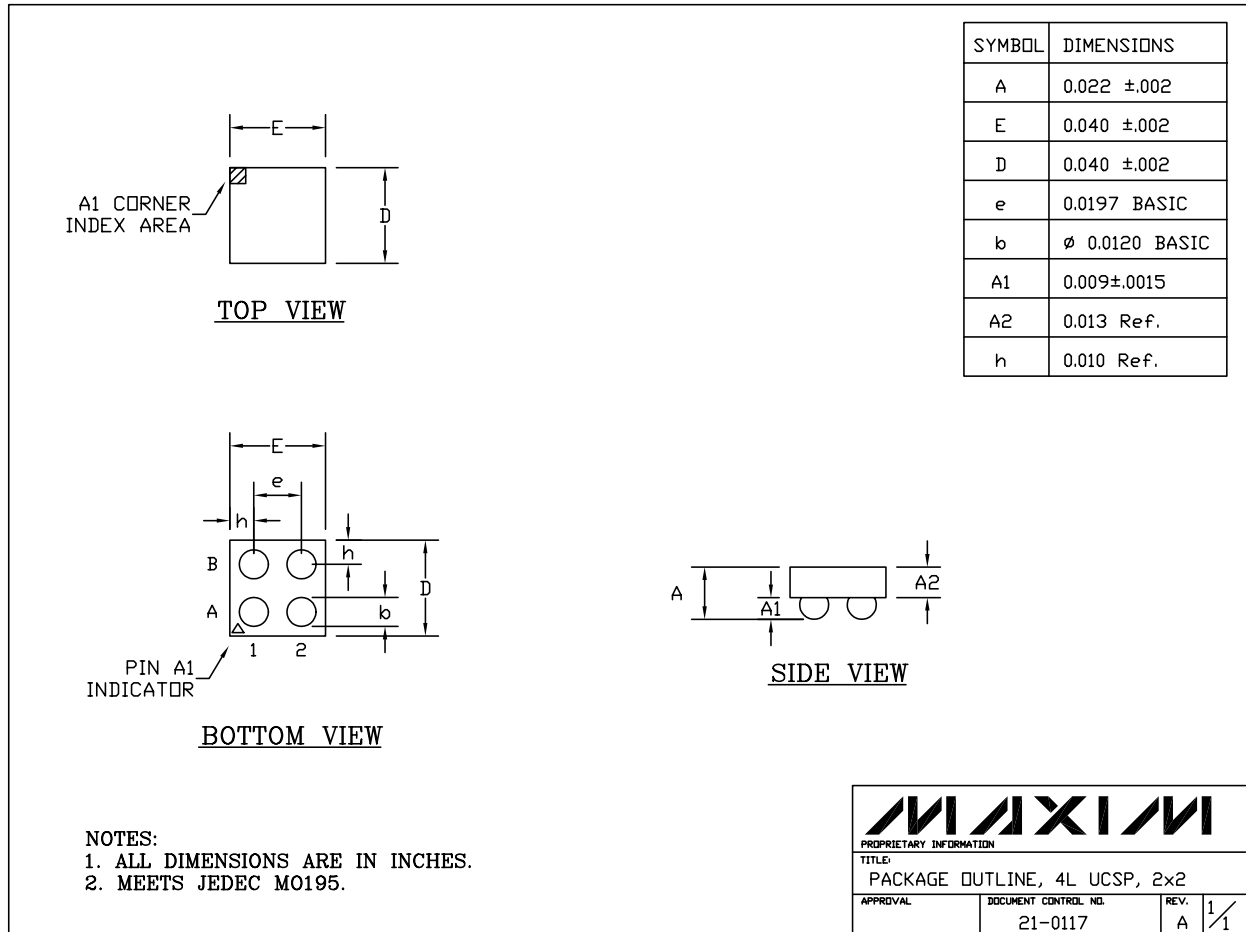
The chip-scale package (UCSP) represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. CSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a CSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a CSP package. CSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Information on Maxim's qualification plan, test data, and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

# μP Supervisory Circuits in 4-Bump (2 × 2) Chip-Scale Package

## Package Information

**MAX6400-MAX6405**



4L UCSP 2x2.EPS

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