

MC14099B

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$)

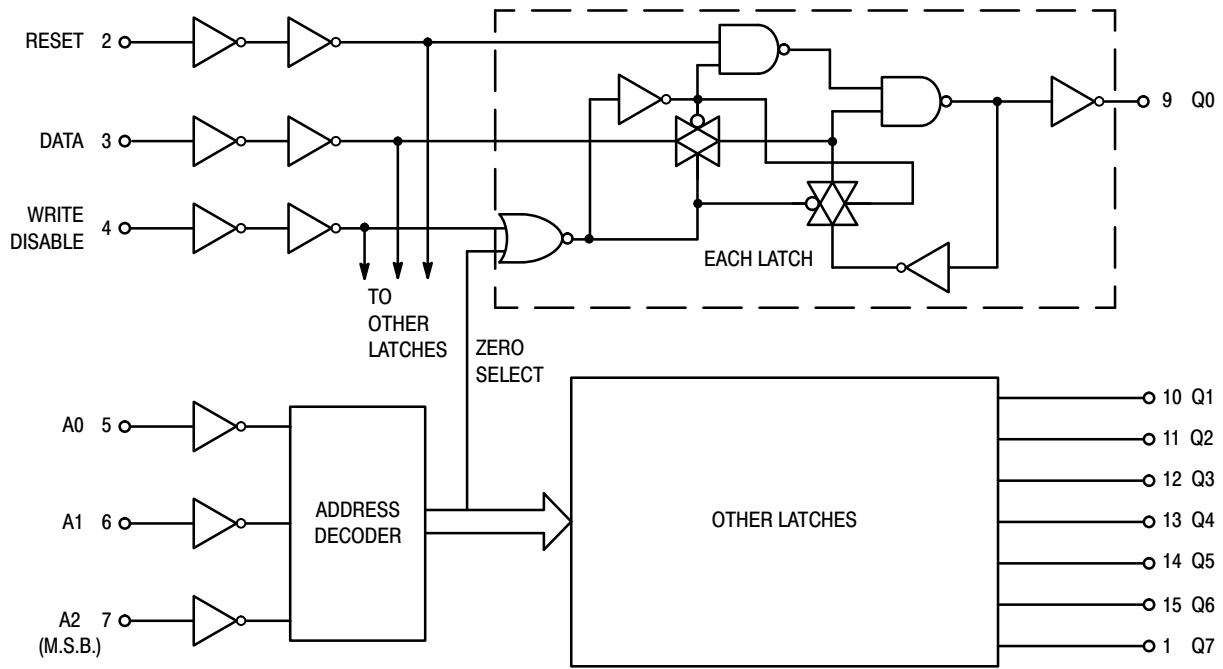
Characteristic	Symbol	V _{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH},$ t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time Data to Output Q	$t_{PHL},$ t_{PLH}	5.0 10 15	– – –	200 75 50	400 150 100	ns
Write Disable to Output Q		5.0 10 15	– – –	200 80 60	400 160 120	ns
Reset to Output Q		5.0 10 15	– – –	175 80 65	350 160 130	ns
CE to Output Q (MC14599B only)		5.0 10 15	– – –	225 100 75	450 200 150	ns
Propagation Delay Time, MC14599B only Chip Enable, Write/Read to Data	$t_{PHL},$ t_{PLH}	5.0 10 15	– – –	200 80 65	400 160 130	ns
Address to Data		5.0 10 15	– – –	200 90 75	400 180 150	ns
Pulse Widths Reset	$t_{w(H)}$ $t_{w(L)}$	5.0 10 15	150 75 50	75 40 25	– – –	ns
Write Disable		5.0 10 15	320 160 120	160 80 60	– – –	ns
Set Up Time Data to Write Disable	t_{su}	5.0 10 15	100 50 35	50 25 20	– – –	ns
Hold Time Write Disable to Data	t_h	5.0 10 15	150 75 50	75 40 25	– – –	ns
Set Up Time Address to Write Disable	t_{su}	5.0 10 15	100 80 40	45 30 10	– – –	ns
Removal Time Write Disable to Address	t_{rem}	5.0 10 15	0 0 0	– 80 – 40 – 40	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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FUNCTION DIAGRAM



TRUTH TABLE

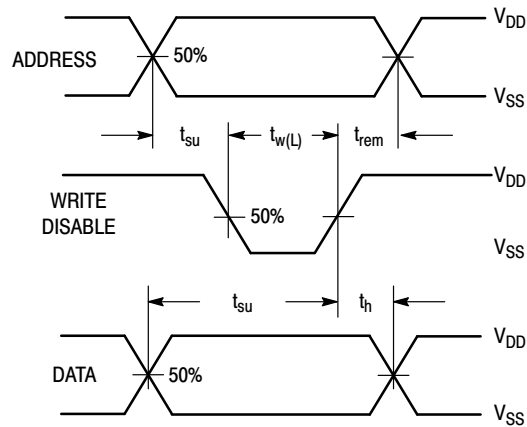
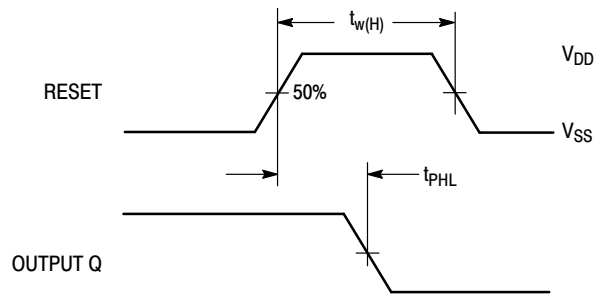
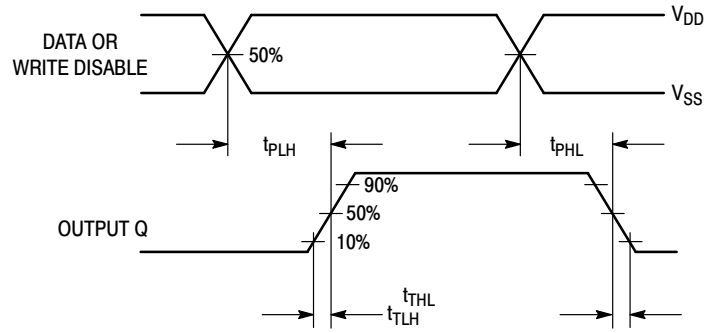
Write Disable	Reset	Addressed Latch	Unaddressed Latches
0	0	Data	Q_n^*
0	1	Data	Reset †
1	0	Q_n^*	Q_n^*
1	1	Reset	Reset

* Q_n is previous state of latch.
 †Reset to zero state.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

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SWITCHING WAVEFORMS



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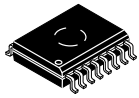
ORDERING INFORMATION

Device	Package	Shipping†
MC14099BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail
MC14099BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel
NLV14099BDWR2G*	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

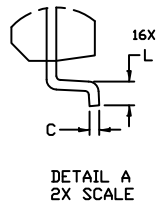
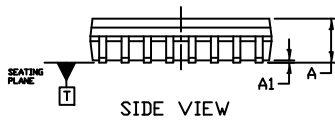
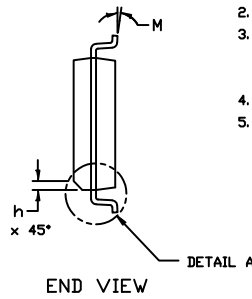
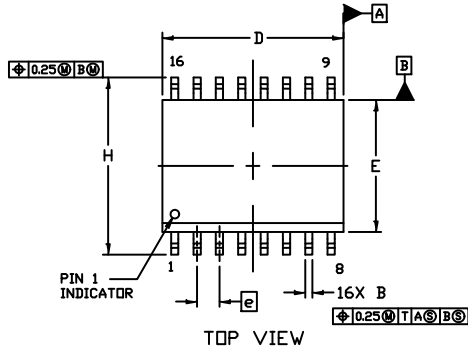
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1
SCALE 1:1

SOIC-16 WB
CASE 751G
ISSUE E

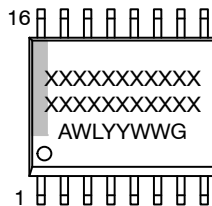
DATE 08 OCT 2021



- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 - CONTROLLING DIMENSION: MILLIMETERS
 - DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF *B* DIMENSION AT MAXIMUM MATERIAL CONDITION.
 - DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD PROTRUSIONS.
 - MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

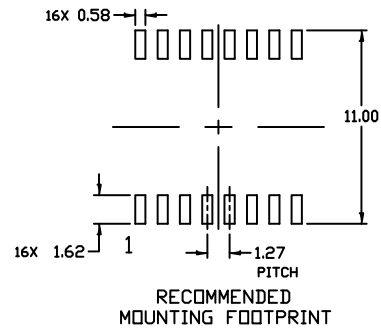
DIM	MILLIMETERS	
	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	SOIC-16 WB	PAGE 1 OF 1

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