

Freescale Semiconductor, Inc.

- **Analog-to-Digital Converters**
 - One or two 8-channel modules with 10-bit resolution depending on the package option
 - External conversion trigger capability
- **Up to five 1M bit per second, CAN 2.0 A, B software compatible modules**
 - Five receive and three transmit buffers
 - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
 - Four separate interrupt channels for Receive, Transmit, Error and Wake-up
 - Low-pass filter wake-up function in STOP mode
 - Loop-back for self test operation
- **Enhanced Capture Timer (ECT)**
 - 16-bit main counter with 7-bit prescaler
 - 8 programmable input capture or output compare channels; 4 of the 8 input captures with buffer
 - Input capture filters and buffers, three successive captures on four channels, or two captures on four channels with a capture/compare selectable on the remaining four
 - Four 8-bit or two 16-bit pulse accumulators
 - 16-bit modulus down-counter with 4-bit prescaler
 - Four user-selectable delay counters for signal filtering
- **8 PWM channels with programmable period and duty cycle (7 channels on 80 Pin Packages)**
 - 8-bit, 8-channel or 16-bit, 4-channel
 - Separate control for each pulse width and duty cycle
 - Center- or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies
- **Serial interfaces**
 - Two asynchronous serial communications interfaces (SCI)
 - Up to three synchronous serial peripheral interfaces (SPI)
 - IIC
- **SAE J1850 Compatible Module (BDLC)**
 - 10.4 kbps Variable Pulse Width format
 - Byte level receive and transmit
 - 4x receive mode supported
- **SIM (System Integration Module)**
 - CRG (windowed COP watchdog, real time interrupt, clock monitor, clock generation and reset)
 - MEBI (multiplexed external bus interface)
 - INT (interrupt control)
- **Clock generation**
 - Phase-locked loop clock frequency multiplier
 - Limp home mode in absence of external clock
 - Clock Monitor
 - Low power 0.5 to 16 MHz crystal oscillator reference clock
- **Operating frequency for ambient temperatures $T_A -40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$**
 - 50MHz equivalent to 25MHz Bus Speed for single chip
 - 40MHz equivalent to 20MHz Bus Speed in expanded bus modes.
- **Internal 5V to 2.5V Regulator**
- **112-Pin LQFP or 80-Pin QFP package**
 - I/O lines with 5V input and drive capability
 - 5V A/D converter inputs and 5V I/O
 - 2.5V logic supply
- **Development support**
 - Single-wire background debug™ mode (BDM)
 - On-chip hardware breakpoints

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Table 1 List of MC9S12D-Family members

Flash	RAM	EEPROM	Package	Device	CAN	J1850	SCI	SPI	IIC	A/D	PWM	I/O
512K	14K	4K	112LQFP	DP512	5	1	2	3	1	2/16	8	91
				DT512	3	0	2	3	1	2/16	8	91
				DJ512	2	1	2	3	1	2/16	8	91
256K	12K	4K	112LQFP	DT256	3	0	2	3	1	2/16	8	91
				DJ256	2	1	2	3	1	2/16	8	91
				DG256	2	0	2	3	1	2/16	8	91
			80QFP	DJ256	2	1	2	3	1	1/8	7	59
				DG256	2	0	2	3	1	1/8	7	59
128K	8K	2K	112LQFP	DT128	3	0	2	2	1	2/16	8	91
				DJ128	2	1	2	2	1	2/16	8	91
				DG128	2	0	2	2	1	2/16	8	91
			80QFP	DJ128	2	1	2	2	1	1/8	7	59
				DG128	2	0	2	2	1	1/8	7	59
64K	4K	1K	112LQFP	DJ64	1	1	2	1	1	2/16	8	91
				D64	1	0	2	1	1	2/16	8	91
			80QFP	DJ64	1	1	2	1	1	1/8	7	59
				D64	1	0	2	1	1	1/8	7	59
32K	2K	1K	80QFP	D32	1	0	2	1	0	1/8	7	59

• Pin out explanations:

- A/D is the number of modules/total number of A/D channels.
- I/O is the sum of ports capable to act as digital input or output.
- 112 Pin Packages:
 - Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 7, M = 8, P = 8, S = 8, T = 8, PAD = 16 input only.
 - 22 inputs provide Interrupt capability (H =8, P= 8, J = 4, IRQ, XIRQ)
- 80 Pin Packages:
 - Port A = 8, B = 8, E = 6 + 2 input only, J = 2, M = 6, P = 7, S = 4, T = 8, PAD = 8 input only.
 - 11 inputs provide Interrupt capability (P= 7, J = 2, IRQ, XIRQ)
- CAN0 pins are shared between J1850 pins.
- CAN0 can be routed under software control from PM1:0 to pins PM3:2 or PM5:4 or PJ7:6.
- CAN4 pins are shared between IIC pins.
- CAN4 can be routed under software control from PJ7:6 to pins PM5:4 or PM7:6.
- Versions with 4 CAN modules will have CAN0, CAN1, CAN2 and CAN4.
- Versions with 3 CANs modules will have CAN0, CAN1 and CAN4.
- Versions with 2 CAN modules will have CAN0 and CAN4.
- Versions with one CAN module will have CAN0.
- Versions with 2 SPI modules will have SPI0 and SPI1.
- Versions with 1 SPI will have SPI0.
- SPI0 can be routed to either Ports PS7:4 or PM5:2.
- SPI2 pins are shared with PWM7:4; In 112 pin versions SPI2 can be routed under software control to PH7:4. In 80 pin packages \overline{SS} -signal of SPI2 is not bonded out!

NOTE

CAN and SPI routing features are not available on the 1st PC9S12DP256 mask set 0K36N!

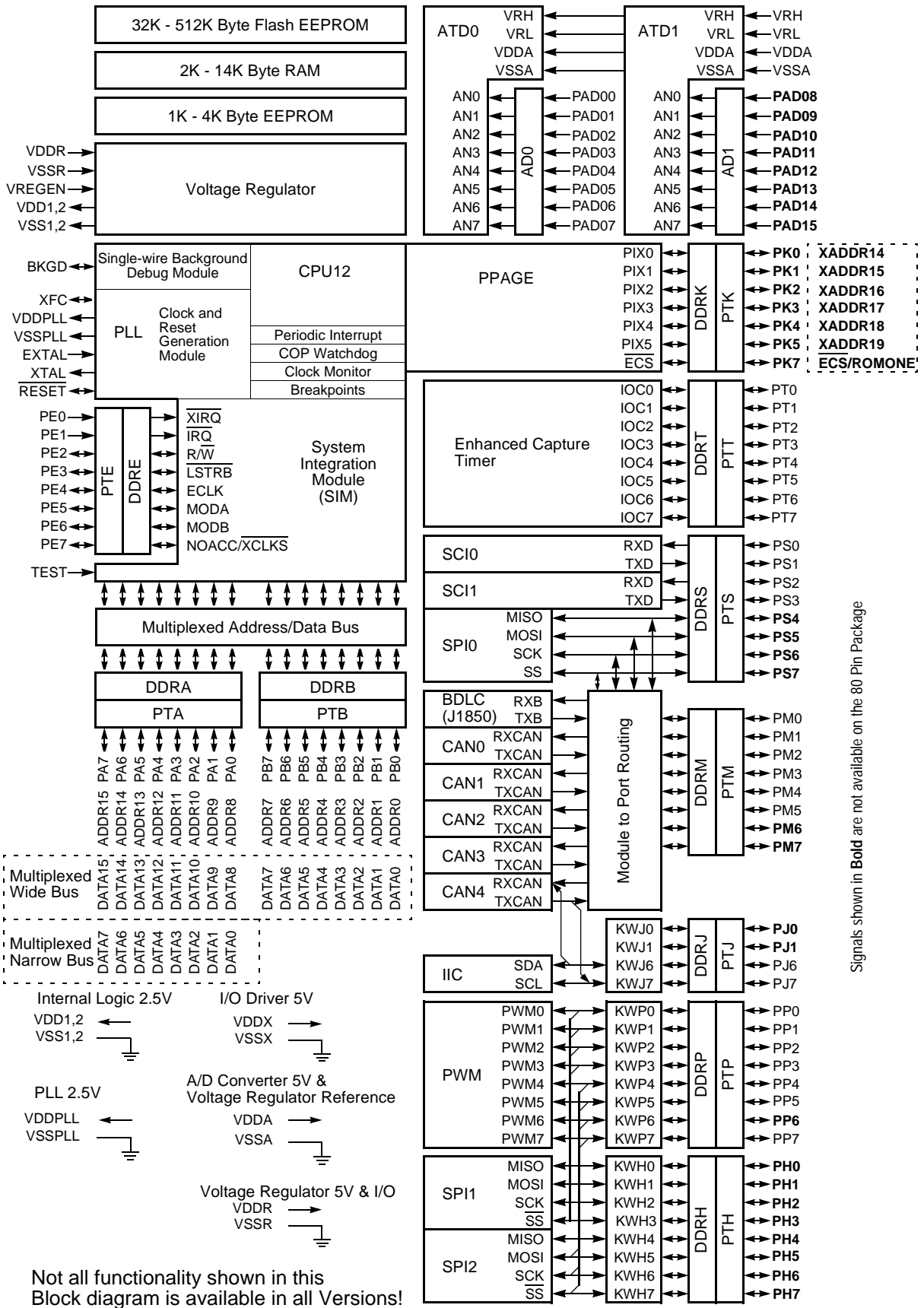
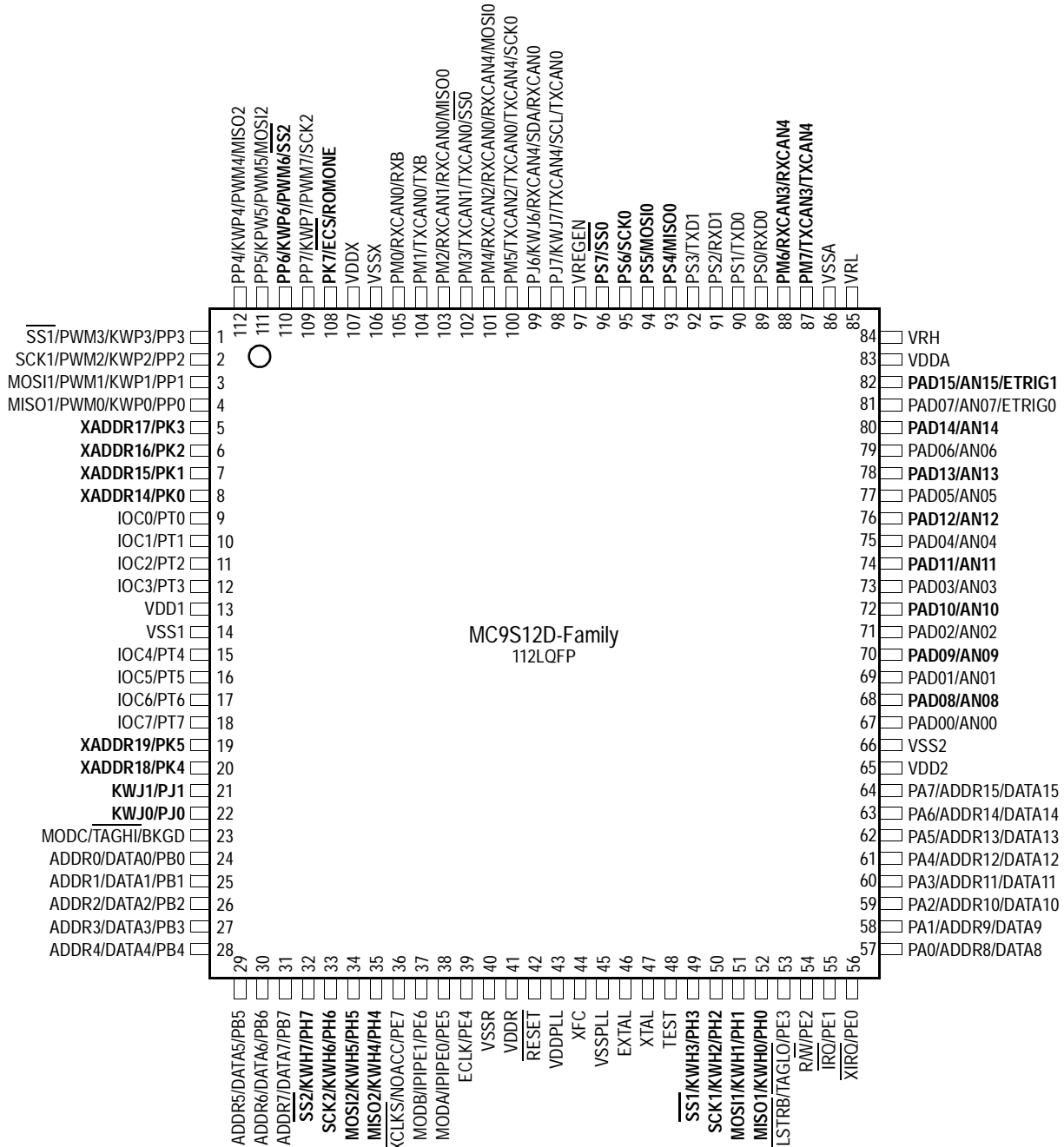


Figure 1 Pin assignments 112 LQFP for MC9S12D-Family



Signals shown in **Bold** are not available on the 80 Pin Package

Figure 2 Pin Assignments in 80 QFP for MC9S12D-Family

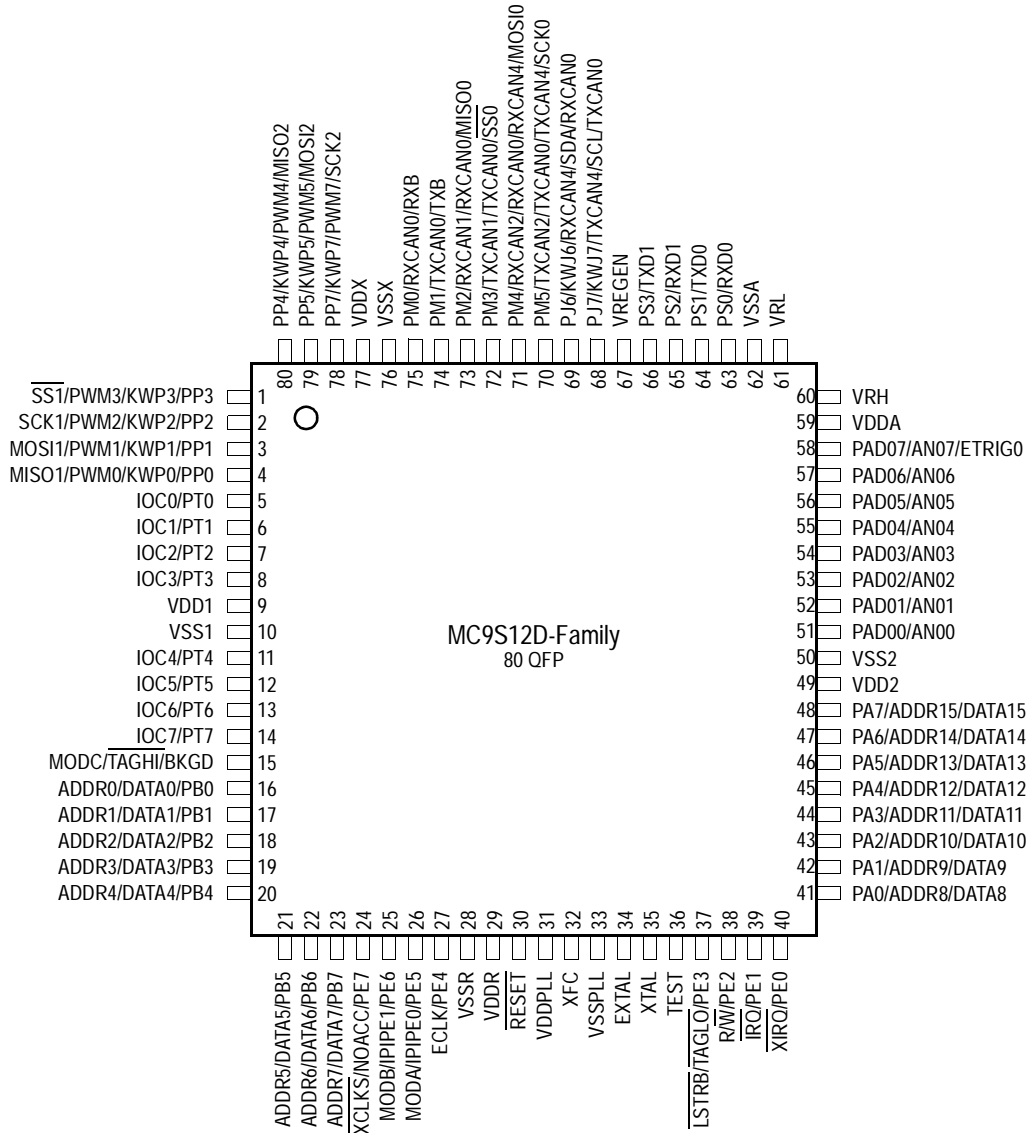
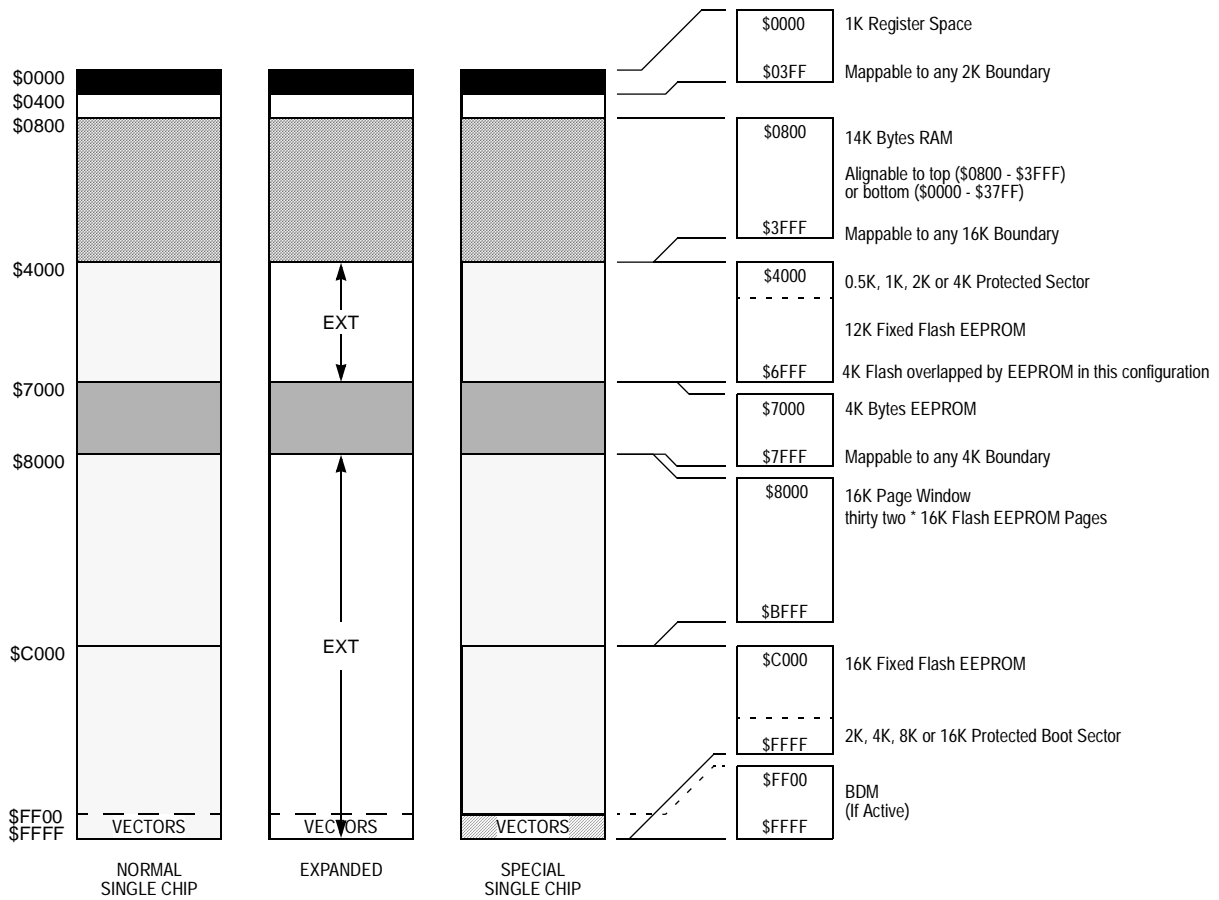


Figure 3 MC9S12Dx512 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

- \$0000 - \$03FF: Register Space
- \$0800 - \$3FFF: 14K RAM
- \$0000 - \$0FFF: 4K EEPROM (1k \$0400 - \$07FF visible, \$0000 - \$03FF and \$0800 - \$0FFF are not visible)
- Various possibilities to make more of the EEPROM fully visible are available, one of them is shown above

Figure 4 MC9S12Dx256 User Configurable Memory Map

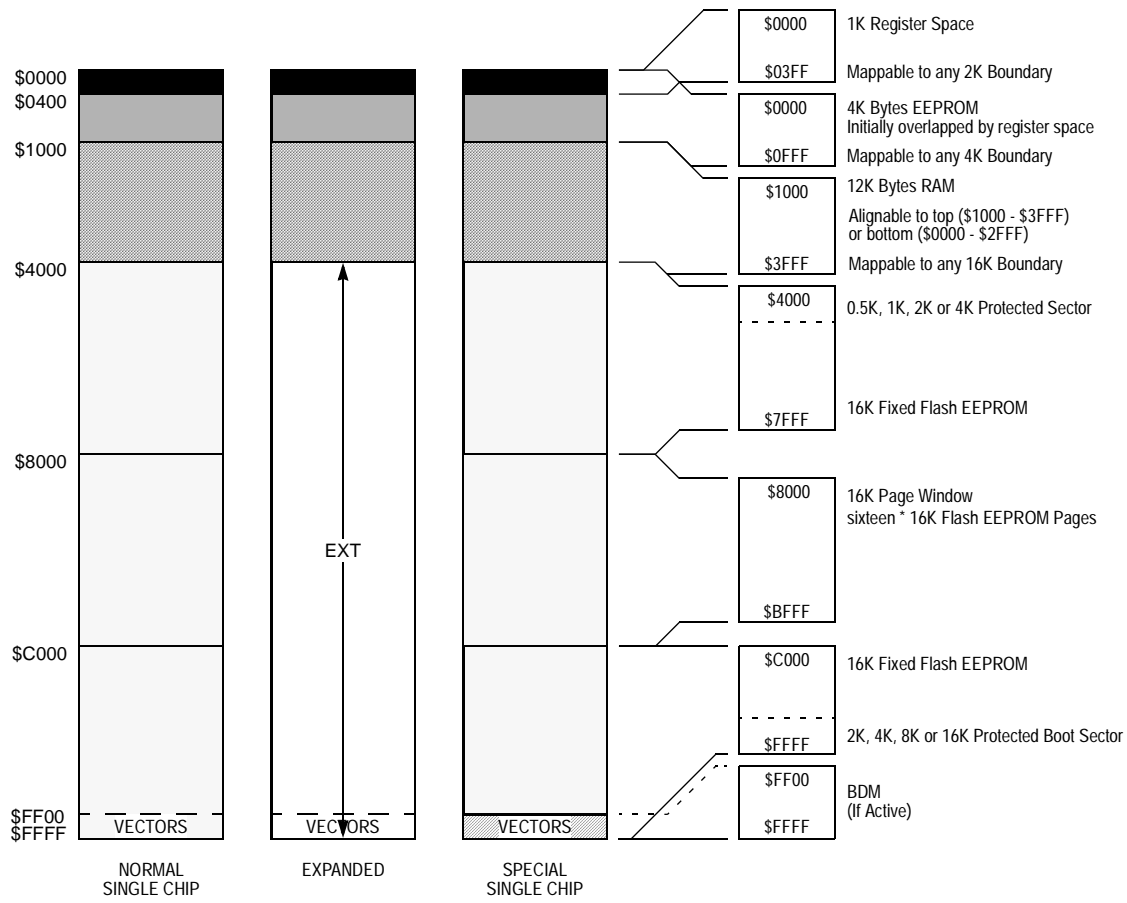
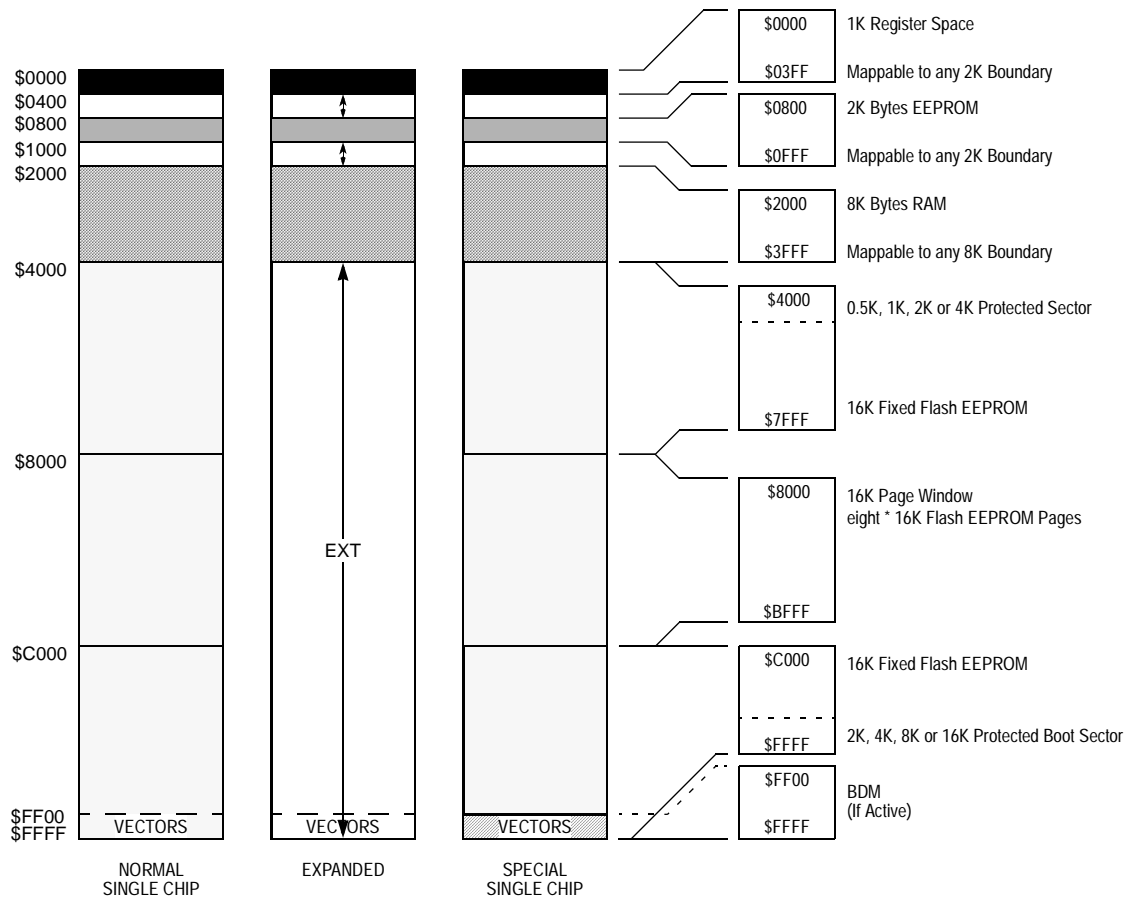


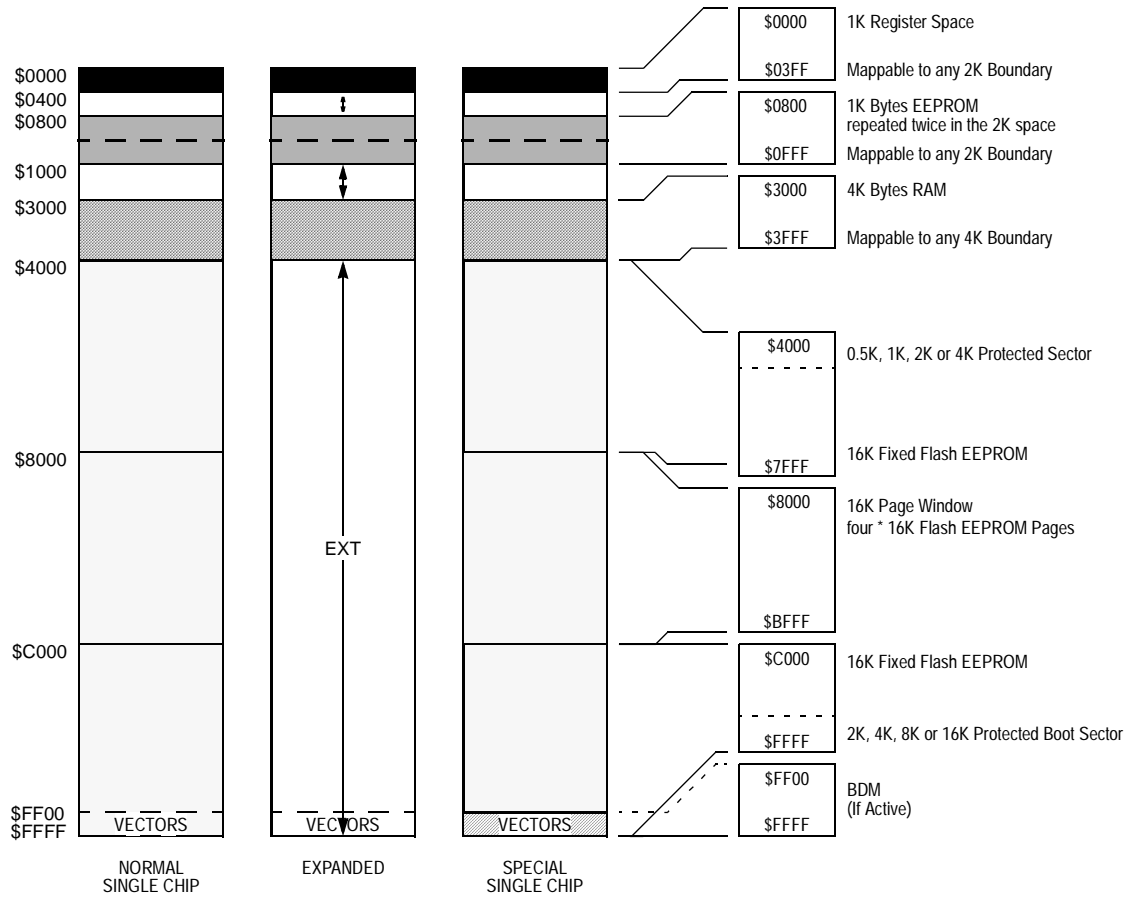
Figure 5 MC9S12Dx128 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

- \$0000 - \$03FF: Register Space
- \$0000 - \$1FFF: 8K RAM
- \$0000 - \$07FF: 1K EEPROM (not visible)

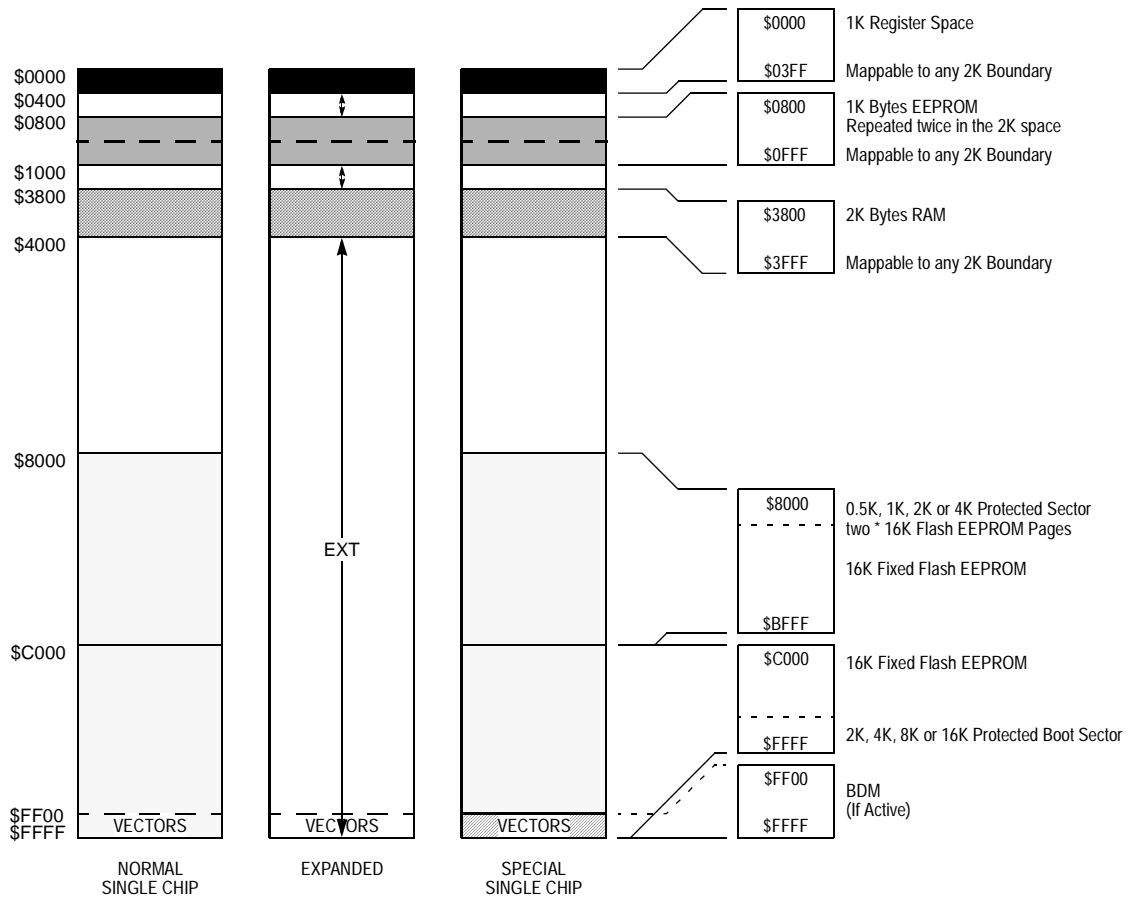
Figure 6 MC9S12Dx64 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

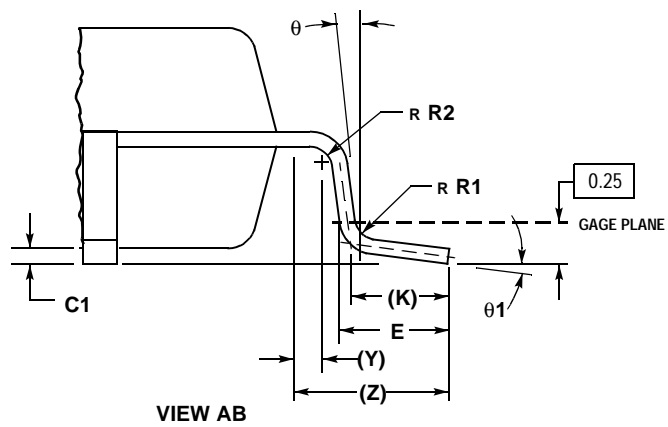
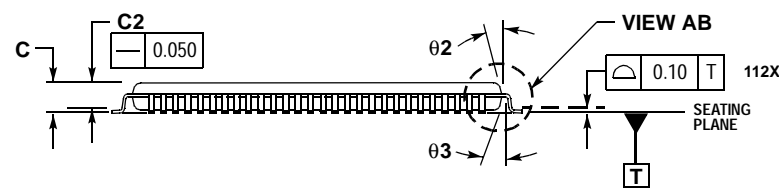
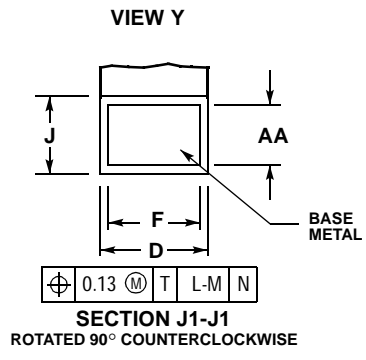
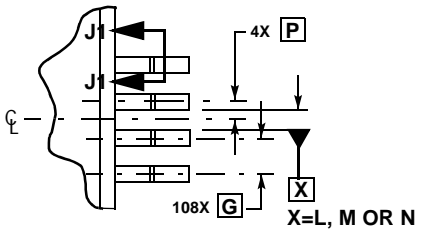
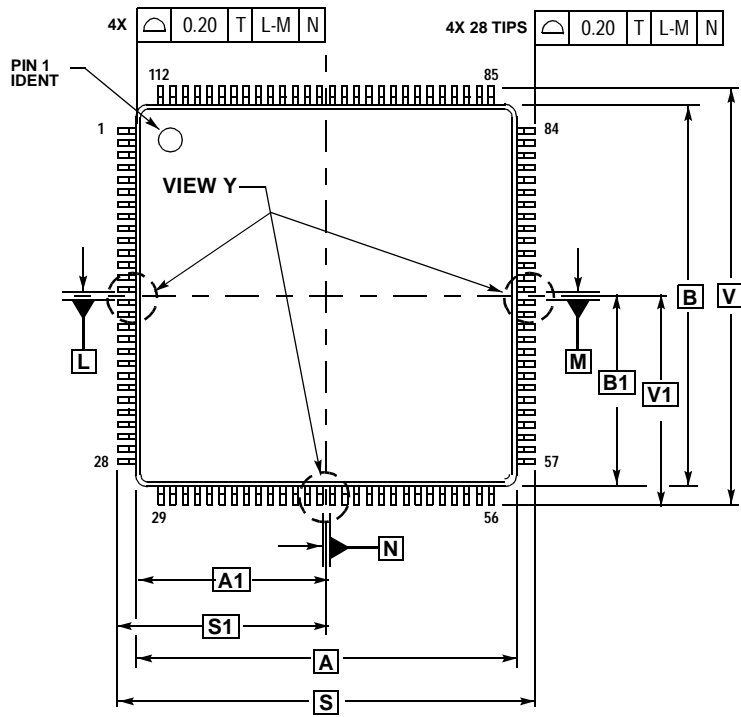
- \$0000 - \$03FF: Register Space
- \$0000 - \$0FFF: 4K RAM
- \$0000 - \$07FF: 1K EEPROM (not visible)

Figure 7 MC9S12Dx32 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

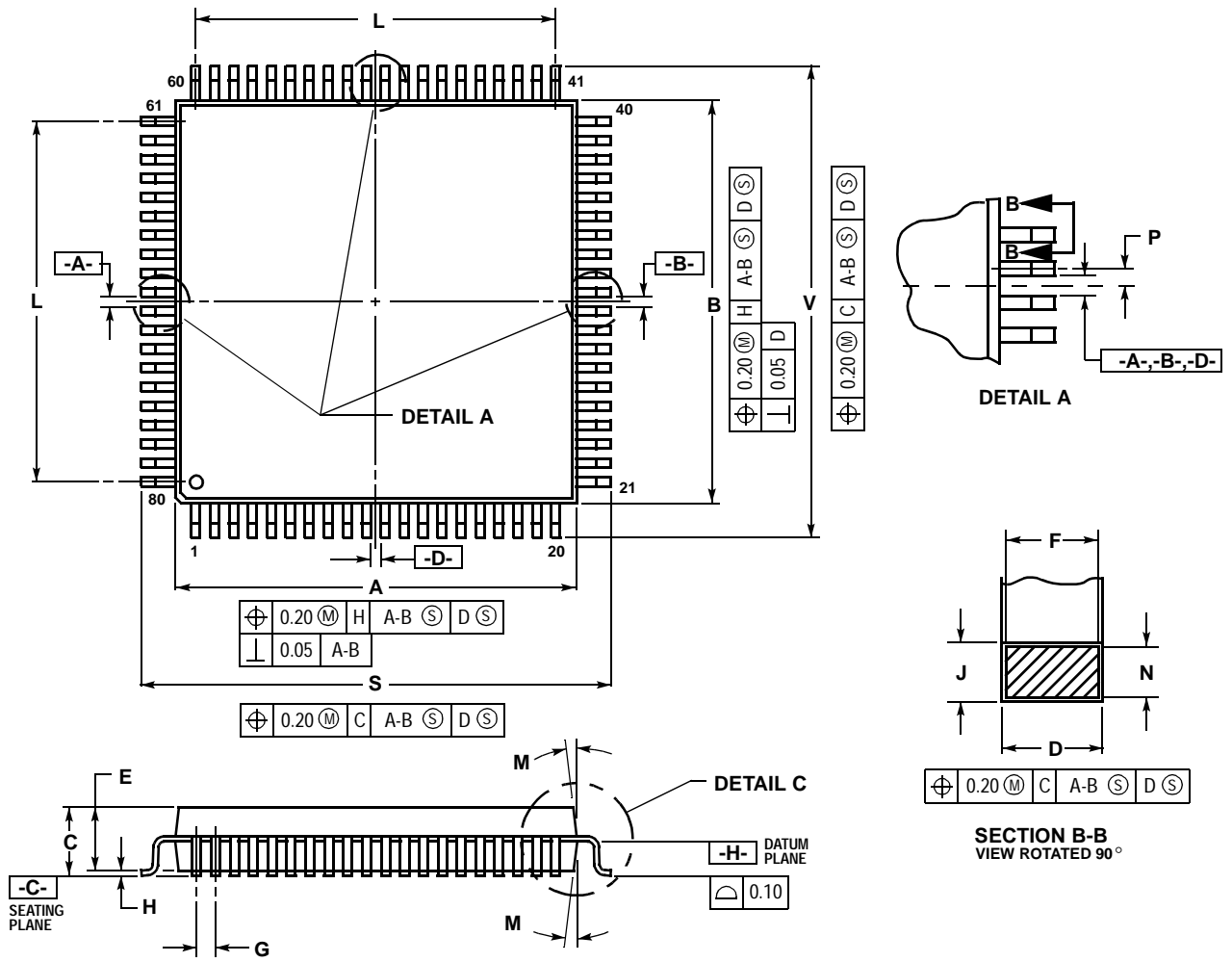
- \$0000 - \$03FF: Register Space
- \$0800 - \$0FFF: 2K RAM
- \$0000 - \$07FF: 1K EEPROM (not visible)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS IN MILLIMETERS.
 3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
 4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
 5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
 6. DIMENSION D DOES NOT INCLUDE DAMBAR

DIM	MILLIMETERS	
	MIN	MAX
A	20.000	BSC
A1	10.000	BSC
B	20.000	BSC
B1	10.000	BSC
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650	BSC
J	0.090	0.170
K	0.500	REF
P	0.325	BSC
R1	0.100	0.200
R2	0.100	0.200
S	22.000	BSC
S1	11.000	BSC
V	22.000	BSC
V1	11.000	BSC
Y	0.250	REF
Z	1.000	REF
AA	0.090	0.160
theta	0°	8°
theta 1	3°	7°
theta 2	11°	13°
theta 3	11°	13°

Figure 8 112-pin LQFP Mechanical Dimensions (case no. 987)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
 4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
 5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
 6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
 7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

DIM	MILLIMETERS	
	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure 9 80-pin QFP Mechanical Dimensions (case no. 841B)

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