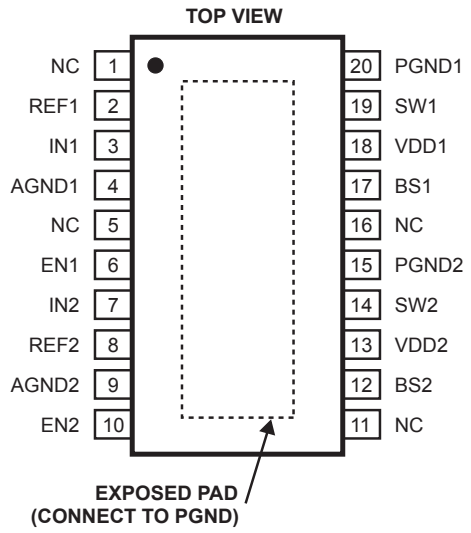
PACKAGE REFERENCE



Part Number*	Package	Temperature
MP7722DF	TSSOP20F	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP7722DF–Z)
For Lead Free, add suffix –LF (eg. MP7722DF–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{DD} 26V
BS Voltage..... V_{SW} – 0.3V to V_{SW} + 6.5V
Enable Voltage V_{EN} ..... –0.3V to +6V
V_{SW}, V_{PIN}, V_{NIN} ..... –1V to V_{DD} + 1V
AGND to PGND ..... –0.3V to +0.3V
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (2)

Supply Voltage V_{DD} ..... 9.5V to 24V
Operating Temperature T_A ..... –40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
TSSOP20F	40	6....	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{DD} = 24V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Standby Current		V_{EN} = 0V		2	10	µA
Quiescent Current				3	6	mA
Output Drivers						
SW On Resistance		Sourcing and Sinking		0.18		Ω
Short Circuit Current		Sourcing and Sinking		5.0		A
Inputs						
REF1/2, IN1/2 Input Common Mode Voltage Range			0	$\frac{V_{DD}}{2}$	V_{DD} – 1.5	V
REF1/2, IN1/2 Input Current		V_{PIN} = V_{NIN} = 12V		1	5	µA
EN Enable Threshold Voltage		V_{EN} Rising		1.4	2.0	V
		V_{EN} Falling	0.4	1.2		V
EN Enable Input Current		V_{EN} = 5V		1		µA
Thermal Shutdown						
Thermal Shutdown Trip Point		T_J Rising		150		°C
Thermal Shutdown Hysteresis				30		°C
Standby Current		V_{EN} = 0V		260		µA
Quiescent Current				23		mA

OPERATING SPECIFICATIONS

Circuit of Figure 1, V_{DD} = 24V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Output		f = 1KHz, THD+N = 10%, 4Ω Load		20		W
		f = 1KHz, THD+N = 10%, 8Ω Load		10		W
THD+ Noise		P_{OUT} = 1W, f = 1KHz, 4Ω Load		0.16		%
		P_{OUT} = 1W, f = 1KHz, 8Ω Load		0.06		%
Efficiency		f = 1KHz, P_{OUT} = 1W, 4Ω Load		90		%
		f = 1KHz, P_{OUT} = 1W, 8Ω Load		95		%
Maximum Power Bandwidth				20		KHz
Dynamic Range				93		dB
Noise Floor		A-Weighted		190		μV
Power Supply Rejection		f = 1KHz		60		dB

PIN FUNCTIONS

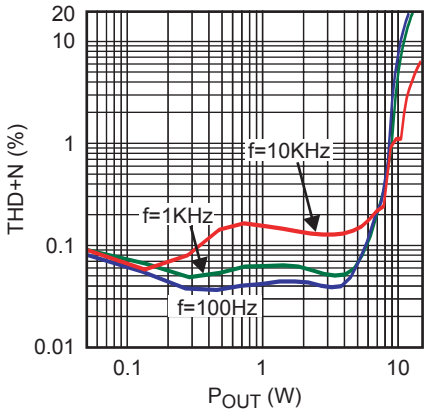
Pin #	Name	Description
1, 5, 11, 16	NC	No Connect. Not internally connected
2	REF1	Amplifier 1 Reference. REF1 is the reference point for amplifier 1. Use a resistive voltage divider to set the voltage at REF1 to V_{DD}/2.
3	IN1	Amplifier 1 Input. IN1 is the inverting input for amplifier 1.
4	AGND1	Analog Ground 1. Connect AGND1 to AGND2.
6	EN1	Enable Input 1. EN1 must be connected to EN2. Drive EN1 high to enable MP7722; low to disable it.
7	IN2	Amplifier 2 Input. IN2 is the inverting input for amplifier 2.
8	REF2	Amplifier 2 Reference. REF2 is the reference point for amplifier 2. Use a resistive voltage divider to set the voltage at REF1 to V_{DD}/2.
9	AGND2	Analog Ground 2. Connect AGND2 to AGND1.
10	EN2	Enable Input 2. EN2 must be connected to EN1. Drive high to enable MP7722, drive low to disable.
12	BS2	High-Side MOSFET Bootstrap Input for Amplifier 2. A capacitor from BS2 to SW2 supplies the gate drive current to the internal high-side MOSFET. Connect a 1μF capacitor from SW2 to BS2.
13	VDD2	Power Supply Input. Bypass VDD2 to PGND2 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the IC PIN13 and PIN15.
14	SW2	Switched Power Output. SW2 is the output of Amplifier 2. Connect the LC filter to this pin.
15	PGND2	Power Ground for Amplifier 2. Connect PGND2 to PGND1.

PIN FUNCTIONS *(continued)*

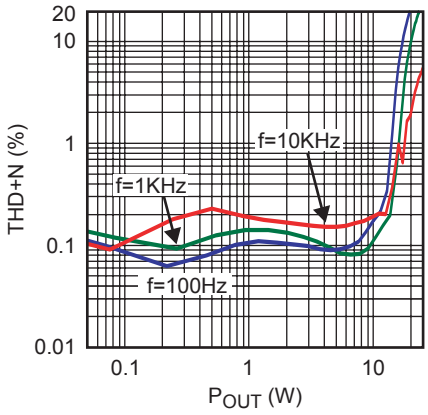
Pin #	Name	Description
17	BS1	High-Side MOSFET Bootstrap Input for Amplifier 1. A capacitor from BS1 to SW1 supplies the gate drive current to the internal high-side MOSFET. Connect a 1µF capacitor from SW1 to BS1. See Figure 1.
18	VDD1	Power Supply Input. Bypass VDD1 to PGND1 with a 1µF X7R capacitor (in addition to the main bulk capacitor), placed close to the IC PIN18 and PIN20.
19	SW1	Switched Power Output. SW1 is the output of Amplifier 1. Connect the LC filter to this pin. See Figure 1.
20	PGND1	Power Ground for Amplifier 1. Connect PGND1 to PGND2. See Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS

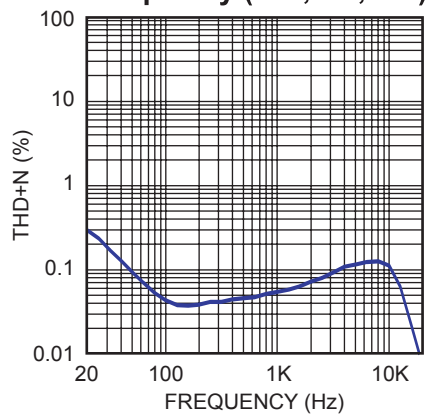
THD+N vs P_{OUT} (24V, 8Ω)



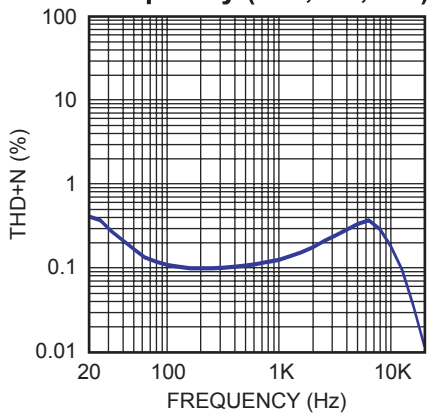
THD+N vs P_{OUT} (24V, 4Ω)



THD+N vs Frequency (24V, 8Ω, 4W)

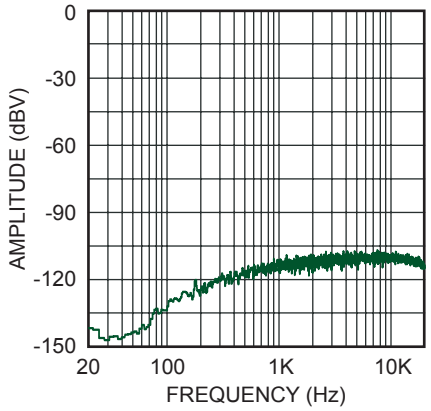


THD+N vs Frequency (24V, 4Ω, 4W)

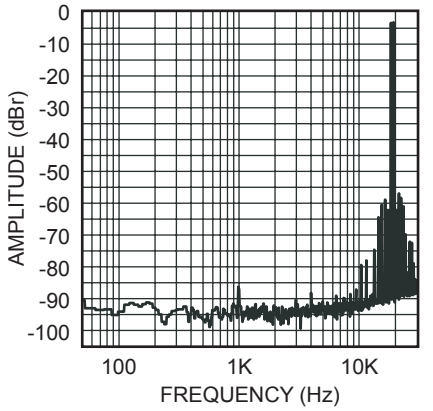


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

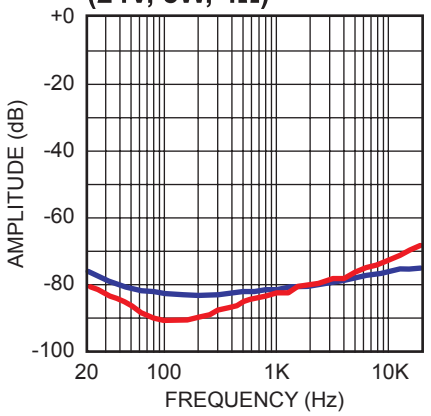
FFT Noise Floor
(A-wtd, 4Ω, A_V=12)



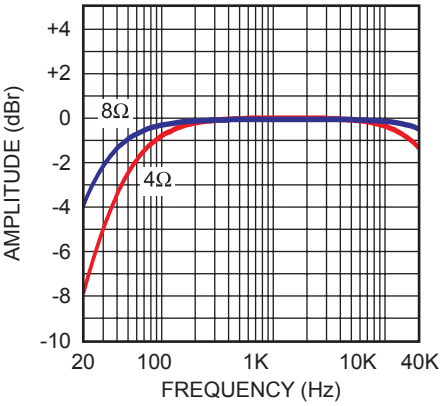
IHF-IMD
(1W, 4Ω, 24V, BW=80KHz)



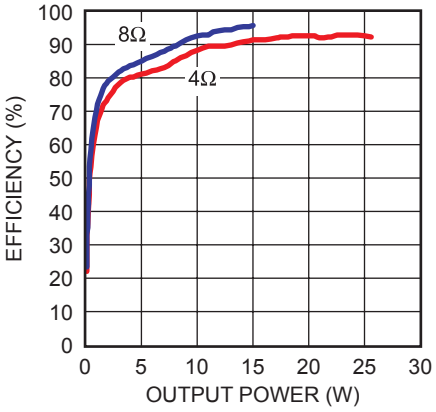
Crosstalk/Separation
vs. Frequency
(24V, 5W, 4Ω)



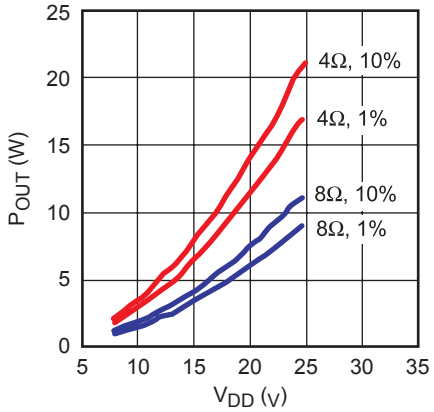
Frequency Response
0dBref = 4W, C_{IN} = 2.2µF,
R_{IN} = 10kΩ, C_{OUT} = 1000µF



Efficiency vs
P_{OUT}



P_{OUT} vs
V_{DD}



OPERATION

The MP7722 uses Monolithic Power Systems' patented Analog Adaptive Modulation™ to convert the audio input signal into pulses of power that, when filtered through an external inductor-capacitor filter, reproduce the amplified signal across the load. Because of the switching Class D output stage, power dissipation in the amplifier is drastically reduced when compared to Class A, B or A/B amplifiers while providing high fidelity and low distortion. The voltage gain is set by the combination of the input resistor R_{IN} and the feedback resistor R_{FB} and is calculated by the equation:

$$A_V = \frac{-R_{FB}}{R_{IN}}$$

Where for Channel 1: $R_{FB}=R_{FB1}$ and $R_{IN}=R_{IN1}$ and for Channel 2: $R_{FB}=R_{FB2}$ and $R_{IN}=R_{IN2}$.

The MP7722 includes four high-power MOSFETS wherein for each channel the output driver stage uses two 180mΩ N-Channel MOSFETs to deliver the pulses to the LC output filter that in turn drives the load. To fully enhance the high-side MOSFET, the gate is driven to a voltage higher than V_{DD} by the bootstrap capacitor between SW and BS. While the output is driven low, the bootstrap capacitor is charged from V_{DD}. The gate of the high-side MOSFET is driven high from the voltage at BS, forcing the MOSFET gate to a voltage higher than V_{DD} and allowing the MOSFET to fully turn on, reducing power loss in the amplifier.

Pop Elimination

The capacitors C_{OUT1} and C_{OUT2} block the DC signal and pass only the AC signals to the load. To insure that the amplifier passes low frequency signals, the capacitor values need to be chosen such that the time constant of C_{OUT} x R_{LOAD} is long. During startup, these capacitors need to be charged up to the DC operating point, which is typically at ½ of V_{DD}. The MP7722 includes special integrated circuitry that carefully controls the pre-charging of these capacitors, eliminating the turn-on and turn-off pop normally associated with the charging of the AC coupling capacitors.

Short Circuit/Overload Protection

The MP7722 has internal overload and short circuit protection. The currents in both the high-side and low-side MOSFETs are measured and if the current exceeds the 5.0A short circuit current limit, both MOSFETs are turned off. The MP7722 then restarts with the same power up sequence that is used for normal starting to prevent a pop from occurring after a short circuit condition is removed.

Mute/Enable Function

The MP7722 EN inputs are active high enable controls. To enable the MP7722, drive EN with a 2.0V or higher voltage. To disable the amplifier, drive EN below 0.4V. While the MP7722 is disabled, the V_{DD} operating current is less than 10μA and the output driver MOSFETs are turned off. The MP7722 requires approximately 500ms from the time that EN is asserted (driven high) to when the amplifier begins normal operation.

APPLICATION INFORMATION

COMPONENT SELECTION

The MP7722 uses a minimum number of external components to complete a stereo Class D audio amplifier. The circuit of Figure 1 is optimized for a 24V power supply and a 1.5V RMS maximum input signal. This circuit should be suitable for most applications. However, if this circuit is not suitable, use the following sections to determine how to customize the amplifier for a particular application.

Setting the Voltage Gain

The maximum output voltage swing is limited by the power supply. To achieve the maximum power out of the MP7722 amplifier, the gain resistors should be set such that the maximum input signal results in an output voltage swing that reaches the supply limit (clipping). The maximum output voltage swing at clipping is approximately $\pm V_{DD}/2$. To achieve clipping for a given input signal voltage, where $V_{IN(pk)}$ is the peak input voltage, the voltage gain is:

$$A_V(MAX) = \frac{V_{DD}}{2 \times V_{IN}(pk)}$$

The voltage gain setting results in the peak output voltage approaching its maximum for the maximum input signal. There are applications where it is desirable to allow the amplifier to overdrive slightly, allowing the THD to increase at higher power levels (as the output signal continues to go further into clipping), and so a higher gain than $A_{V\,(max)}$ is required.

Setting the Switching Frequency

The idle switching frequency (the switching frequency when no audio input is present) is a function of several variables: the supply voltage V_{DD}, the timing capacitor C_{INT} and the feedback resistor R_{FB}. For the MP7722, the idle switching frequencies for CH1 and CH2 are independent of each other and are a function of their own associated components. The proper setting of the "idle frequency" is important for obtaining optimum performance. If the frequency is set too high, the result will be more power loss and high distortion, while setting the idle switching frequency too low results in more inductor ripple, causing more output voltage ripple with increased the output noise.

The optimum quiescent switching frequency is approximately 700KHz to 800KHz. Refer to Table 1 for recommended values.

Table 1—Switching Frequency vs. V_{DD}, Timing Capacitor and Feedback Resistor (see Figure 1)

Gain (V/V)	Gain (dB)	R_{FB} (kΩ)	R_{IN} (kΩ)	C_{INT}	F_{SW}	V_{DD} (V)
3.9	11.8	39	10	6.8nF	660KHz	12
8.2	18.3	82	10	3.3nF	660KHz	12
8.3	18.4	39	4.7	6.8nF	660KHz	12
17.4	24.8	82	4.7	3.3nF	660KHz	12
5.6	15.0	56	10	8.2nF	670KHz	24
8.2	18.3	82	10	5.6nF	720KHz	24
11.9	21.5	56	4.7	8.2nF	670KHz	24
17.4	24.8	82	4.7	5.6nF	720KHz	24
33.0	30.4	330	10	1.8nF	700KHz	24

Choosing the LC Filter

The Inductor-Capacitor (LC) filter converts the pulse train at SW to the output voltage that drives the speaker. Typical values for the LC filter are a 10μH inductor and a 0.47μF capacitor.

The characteristic frequency of the LC filter needs to be high enough to allow high frequency audio to the output, yet needs to be low enough to filter out high frequency products of the pulses from SW. The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The voltage ripple at the output is approximated by the equation:

$$V_{RIPPLE} \cong V_{DD} \times \left(\frac{f_0}{f_{SW}}\right)$$

The quality factor (Q) of the LC filter is important. If this is too low output noise will increase, and if this is too high then peaking may occur at high signal frequencies reducing the passband flatness. The circuit Q is set by the load resistance (speaker resistance, typically 4Ω or 8Ω) and is calculated as:

$$Q = \omega_0 \times \frac{L}{R} = 2\pi \times f_0 \times \frac{L}{R}$$

Where ω_0 is the characteristic frequency in radians per second and f_0 is in Hz. Use a LC filter with Q between 0.7 and 2.

The actual output ripple and noise is greatly affected by the type of inductor and capacitor used in the LC filter. Use a film capacitor and an inductor with sufficient power handling capability to supply the output current to the load. The inductor should exhibit soft saturation characteristics. If the inductor exhibits hard saturation, it should operate well below the saturation current. Gapped ferrite, MPP, Powdered Iron or similar type toroidal cores are recommended. If open or shielded bobbin ferrite cores are used for multi-channel designs, make sure that the start windings of each inductor line up (all starts going toward SW pin or all starts going toward the output) to prevent crosstalk or other channel-to-channel interference.

Output Coupling Capacitors

The output AC coupling capacitors C_{OUT1} and C_{OUT2} serve to block DC voltages and thus pass only the amplified AC signal from the LC filter to the load. The combination of the coupling capacitor and the load resistance results in a first-order high-pass filter. The values of C_{OUT1} and C_{OUT2} should be selected such that the required minimum frequency is still allowed to pass. The output corner frequency (-3dB point), f_{OUT}, can be calculated as:

$$f_{OUT} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}}$$

Set the output corner frequency at or below the minimum required frequency.

The output coupling capacitor carries the full load current, so the capacitor should be chosen such that its ripple current rating is greater than the maximum load current. Low ESR aluminum electrolytic capacitors are recommended.

Input Coupling Capacitors

The input coupling capacitors C_{IN1} and C_{IN2} are used to pass only the AC signal at the input. In a typical system application, the source input signal is typically centered around the circuit ground, while the MP7722 input is at half the power supply voltage (V_{DD}/2). The input coupling capacitors transmit the AC signal from the source to the MP7722 while blocking the DC voltage. Choose the input coupling capacitors such that the corner frequency (f_{IN}) is less than the passband frequency. The corner frequency is calculated as:

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}}$$

Power Source

For maximum output power, the amplifier circuit requires a regulated external power source to supply the power to the amplifier. A higher power supply voltage allows more power to be delivered to a given load resistance. However if the power source voltage exceeds the maximum operating voltage of 24V, the MP7722 may sustain permanent damage. It is very important to bypass the power supply pins with 1μF X7R ceramic capacitors.

Power Supply Pumping

It is also very important to bypass the power supply with a large aluminum electrolytic capacitor. It is recommended to use a value of *at least* 2200μF. This is necessary to prevent the supply voltage from getting pumped up to a level that exceeds the absolute maximum rating. Supply pumping occurs in single-ended Class D amplifiers, and is caused by rapid switch transitions where current is pumped back up into the supply line. The large capacitor is necessary to absorb this current and prevent V_{DD} from rising too high.

PCB Layout

The circuit layout is critical for optimum performance and low output distortion and noise. Place the following components as close to the MP7722 as possible:

Power Supply Bypass, C_{BYP}

C_{BYP1} and C_{BYP2} carry the transient current for the switching power stage. To prevent overstressing of the MP7722 and excessive noise at the output, place C_{BYP1} as close to pins 18 (VDD1) and 20 (PGND1) as possible and also place C_{BYP2} as close to pins 13 (VDD2) and 15 (PGND2) as possible.

Output Catch Diodes

D_{SH1}, D_{SL1}, D_{SH2} and D_{SL2} carry the current over the dead-time while the MOSFET switches are off. Place the diodes as close to the MP7722 as possible.

Timing Capacitors

C_{INT1} and C_{INT2} are used to set the amplifier switching frequencies and are typically on the order of a few nF. Place C_{INT1} as close to pins 2 and 3 as possible to reduce distortion and noise. Likewise, place C_{INT2} as close to pins 7 and 8 as possible.

Reference Bypass Capacitors

C_{R1} and C_{R2} filter the ½ V_{DD} reference voltages. Place C_{R1} and C_{R2} as close to the IC as possible to improve power supply rejection and reduce distortion and noise at the output.

When laying out the PCB, use two separate ground planes, analog ground (AGND) and power ground (PGND), and connect the two grounds together at a single point to prevent noise injection into the amplifier input to reduce distortion.

Make sure that any traces carrying the switch node (SW) voltages are separated far from any input signal traces. If it is required to run the SW trace near the input, shield the input with a ground plane between the traces. For multiple channel applications, make sure that each channel is physically separated to prevent crosstalk. Make sure that all inductors used on a single circuit board have the same orientation. Also, make sure that the power supply is routed from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.

High V_{DD} Operation

When operating at higher supply voltages, special care must be taken to ensure that the V_{DD} level does not exceed the absolute maximum supply rating of the IC. Power supply pumping is of significant concern when operating near the maximum supply voltage. Supply pumping is an effect where the V_{DD} voltage is "pumped up" to a higher potential when charge from the output DC blocking capacitor is transferred to the power supply rail during switch transitions. The simplest way to handle excess pumping is to increase the size of the V_{DD} main bulk capacitance such that the extra charge will be absorbed by the increased capacitance, with minimal supply increase. One way to eliminate supply pumping altogether is to use a different output configuration circuit. Figure 2 shows such an alternate configuration for connecting the speaker load. With this configuration, one side of the speaker load is connected directly to the output of the LC filter, while the other side is connected to the mid-point of a series capacitor-divider (C26, C28). Both the LC filter point and the mid point of the capacitor divider will be at a DC bias level of ½ V_{DD}, so the net DC across the speaker is $0V_{DC}$. With the speaker connected in this fashion, there is no series capacitor to cause supply pumping, and supply pumping is virtually eliminated. If the output is connected in this way, however, additional circuitry may be required to protect the speaker from damage in the event of a short circuit. Because both sides of the speaker will be typically biased at ½ V_{DD}, a short-circuit to GND on the negative side of the speaker load will result in a large DC current through the load. For example, if V_{DD}=24V and R_L=4Ω, there will be 12/4=3A of DC current through the load. This current will be sustained by the output FET stage of the IC as it will not trigger the internal over-current protection sense circuitry. A simple external sense circuit will be required for those applications which may experience an externally applied short circuit under normal use. An example of such a circuit is also shown in Figure 2.

Electro-Magnetic Interference (EMI) Considerations

Due to the switching nature of the Class D amplifier, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, with proper component selection and careful attention to circuit layout, the effects of the EMI due to the amplifier switching can be minimized.

The power inductors are a potential source of radiated emissions. For the best EMI performance use toroidal inductors, since the magnetic field is well contained inside the core. However toroidal inductors can be expensive to wind. For a more economical solution, use shielded gapped ferrite or shielded ferrite bobbin core inductors. These inductors typically do not contain the field as well as toroidal inductors, but usually can achieve a better balance of good EMI performance with low cost.

The size of high-current loops that carry rapidly changing currents needs to be minimized. To do this, make sure that the V_{DD} bypass capacitors and the Schottky Catch diodes are as close to the MP7722 as possible.

Nodes that carry rapidly changing voltages, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

TYPICAL APPLICATION CIRCUITS

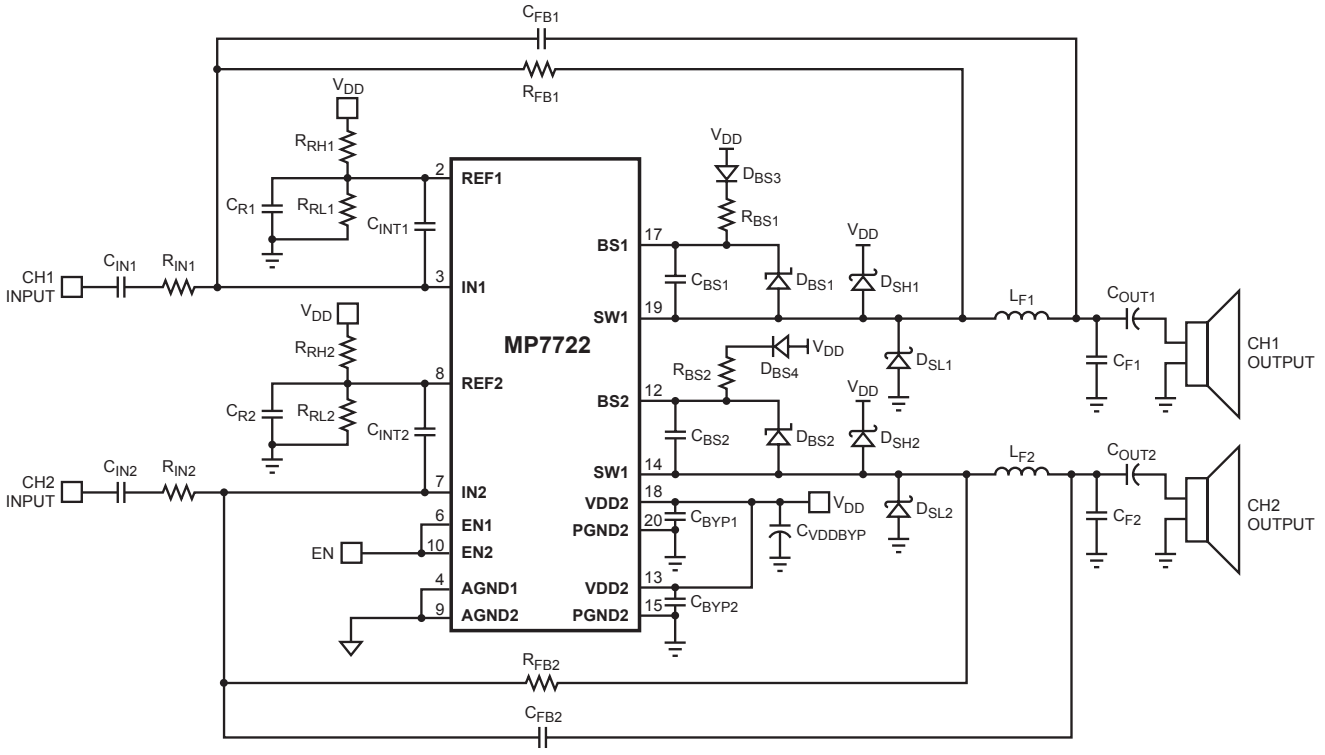


Figure 1—2 x 20W Stereo Typical Application Circuit

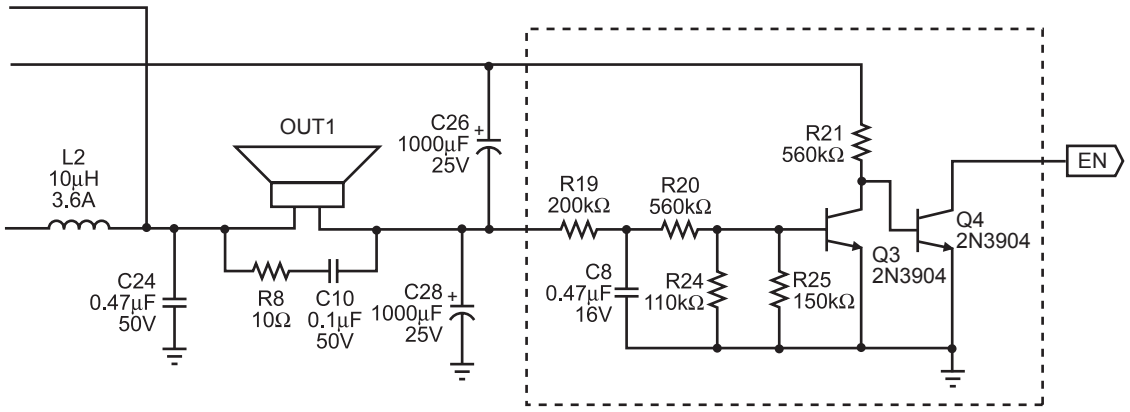
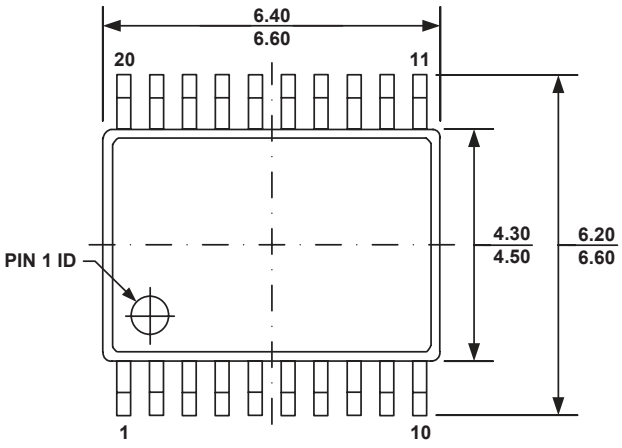


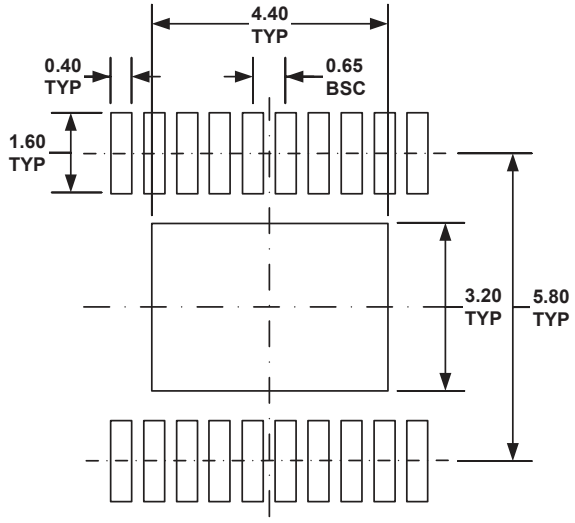
Figure 2—Alternate Configuration for High V_{DD} Applications

PACKAGE INFORMATION

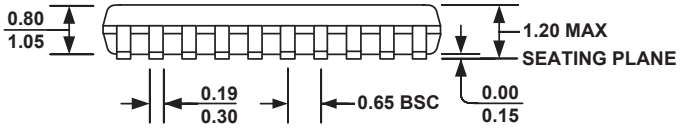
TSSOP20F
(EXPOSED PAD)



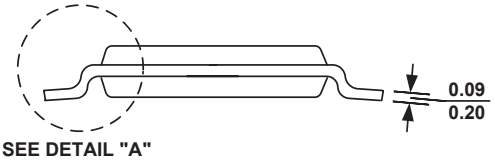
TOP VIEW



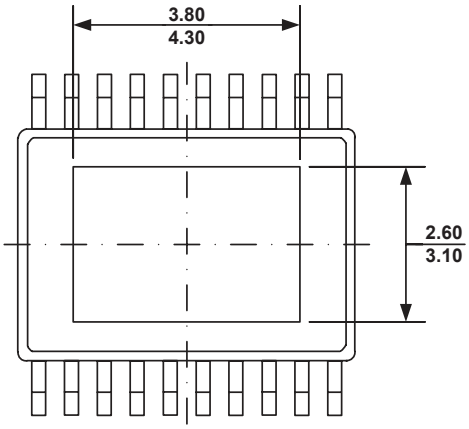
RECOMMENDED LAND PATTERN



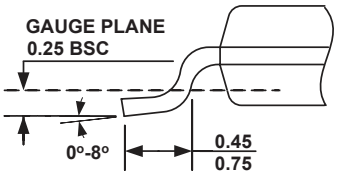
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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