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**REVISION HISTORY**

**2/09—Rev. D to Rev. E**

Deleted 14-Lead CERDIP.....	Throughout
Changes to Features Section and General Description Section.....	1
Delete Military Processed Devices Text, SMD Part Number, ADI Part Number Table, and Dice Characteristics Figure .....	3
Changes to Table 1.....	3
Changes to Absolute Maximum Ratings Section .....	4
Changes to Figure 12.....	6
Changes to Figure 18 and Figure 19.....	7
Changes to Figure 26 and Figure 28.....	8
Deleted OP497 Spice Macro-Model Section.....	10
Changes to Applications Information Section.....	10
Moved Figure 33 .....	10
Deleted Table I. OP497 SPICE Net-List.....	11
Changes to Open-Loop Gain Linearity Section and Figure 35 .....	11
Changes to Figure 40.....	13
Updated Outline Dimensions .....	14
Changes to Ordering Guide .....	15

**11/01—Rev. C to Rev. D**

Edits to Pin Connection Headings.....	1
Deleted Wafer Test Limits .....	3
Edits to Absolute Maximum Ratings .....	5
Edits to Outline Dimensions.....	16
Edits to Ordering Guide .....	17

# SPECIFICATIONS

T<sub>A</sub> = 25°C, V<sub>S</sub> = ±15 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	F Grade			G Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	V <sub>OS</sub>		40	75		80	150		μV
		-40°C ≤ +85°C	70	150		120	250		μV
Average Input Offset Voltage Drift	TCV <sub>OS</sub>	T <sub>MIN</sub> - T <sub>MAX</sub>	0.4	1.0		0.6	1.5		μV/°C
Long-Term Input Offset Voltage Stability			0.1			0.1			μV/Month
Input Bias Current	I <sub>B</sub>	V <sub>CM</sub> = 0 V	40	150		60	200		pA
		-40° ≤ T <sub>A</sub> ≤ +85°C	60	200		80	300		pA
Average Input Bias Current Drift	TC <sub>IB</sub>	-40° ≤ T <sub>A</sub> ≤ +85°C	0.3			0.3			pA/°C
Input Offset Current	I <sub>OS</sub>	V <sub>CM</sub> = 0 V	30	150		50	200		pA
		-40° ≤ T <sub>A</sub> ≤ +85°C	50	200		80	300		pA
Average Input Offset Current Drift	T <sub>CIOS</sub>		0.3			0.4			pA/°C
Input Voltage Range <sup>1</sup>	IVR		±13	±14		±13	±14		V
		T <sub>MIN</sub> - T <sub>MAX</sub>	±13	±13.5		±13	±13.5		V
Common-Mode Rejection	CMR	V <sub>CM</sub> = ±13 V	114	135		114	135		dB
		T <sub>MIN</sub> - T <sub>MAX</sub>	108	120		108	120		dB
Large Signal Voltage Gain	A <sub>VO</sub>	V <sub>O</sub> = ±10 V, R <sub>L</sub> = 2 kΩ	1500	4000		1200	4000		V/mV
		-40° ≤ T <sub>A</sub> ≤ +85°C	800	2000		800	2000		V/mV
Input Resistance Differential Mode	R <sub>IN</sub>		30			30			MΩ
Input Resistance Common Mode	R <sub>INCM</sub>		500			500			GΩ
Input Capacitance	C <sub>IN</sub>		3			3			pF
OUTPUT CHARACTERISTICS									
Output Voltage Swing	V <sub>O</sub>	R <sub>L</sub> = 2 kΩ	±13	±13.7		±13	±13.7		V
		R <sub>L</sub> = 10 kΩ, T <sub>MIN</sub> - T <sub>MAX</sub>	±13	±14		±13	±14		V
		R <sub>L</sub> = 10 kΩ	±13	±13.5		±13	±13.5		V
Short Circuit	I <sub>SC</sub>			±25			±25		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V <sub>S</sub> = ±2 V to ±20 V	114	135		114	135		dB
		V <sub>S</sub> = ±2.5 V to ±20 V, T <sub>MIN</sub> - T <sub>MAX</sub>	108	120		108	120		dB
Supply Current (per Amplifier)	I <sub>SY</sub>	No load		525	625		525	625	μA
		T <sub>MIN</sub> - T <sub>MAX</sub>		580	750		580	750	μA
Supply Voltage Range	V <sub>S</sub>	Operating range	±2		±20	±2		±20	V
		T <sub>MIN</sub> - T <sub>MAX</sub>	±2.5		±20	±2.5		±20	V
DYNAMIC PERFORMANCE									
Slew Rate	SR		0.05	0.15		0.05	0.15		V/μs
Gain Bandwidth Product	GBW			500			500		kHz
Channel Separation	CS	V <sub>O</sub> = 20 V p-p, f <sub>o</sub> = 10 Hz		150			150		dB
NOISE PERFORMANCE									
Voltage Noise	e <sub>n</sub> p-p	0.1 Hz to 10 Hz		0.3			0.3		μV/p-p
Voltage Noise Density	e <sub>n</sub>	e <sub>n</sub> = 10 Hz		17			17		nV/√Hz
		e <sub>n</sub> = 1 kHz		15			15		nV/√Hz
Current Noise Density	i <sub>n</sub>	i <sub>n</sub> = 10 Hz		20			20		fA/√Hz

<sup>1</sup> Guaranteed by CMR test.

# OP497

## ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply to packaged parts.

**Table 2.**

Parameter	Rating
Supply Voltage	±20 V
Input Voltage <sup>1</sup>	20 V
Differential Input Voltage <sup>1</sup>	40 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

<sup>1</sup>For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case mounting conditions, that is,  $\theta_{JA}$  is specified for a device in socket for the PDIP package, and  $\theta_{JA}$  is specified for a device soldered to the printed circuit board (PCB) for the SOIC package.

**Table 3.**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
14-Lead PDIP (N-14)	76	33	°C/W
16-Lead SOIC (RW-16)	92	23	°C/W

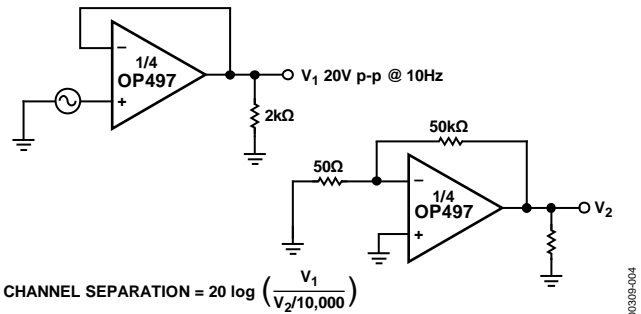


Figure 4. Channel Separation Test Circuit

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

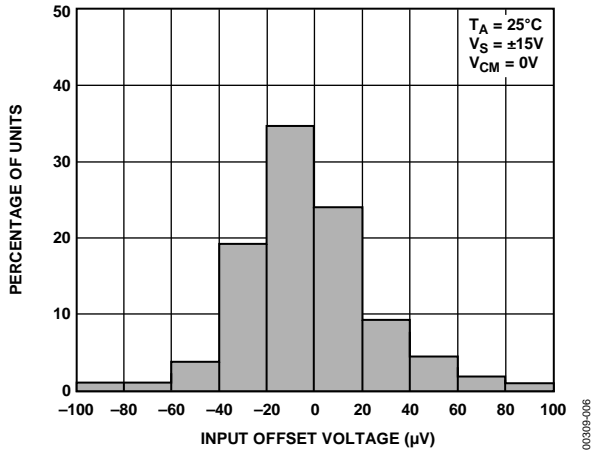


Figure 5. Typical Distribution of Input Offset Voltage

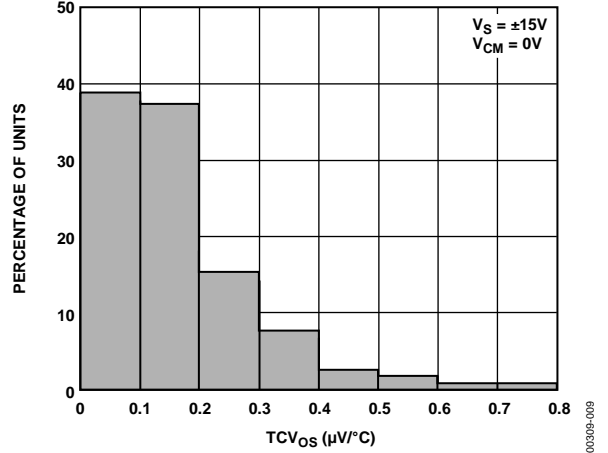


Figure 8. Typical Distribution of  $TCV_{OS}$

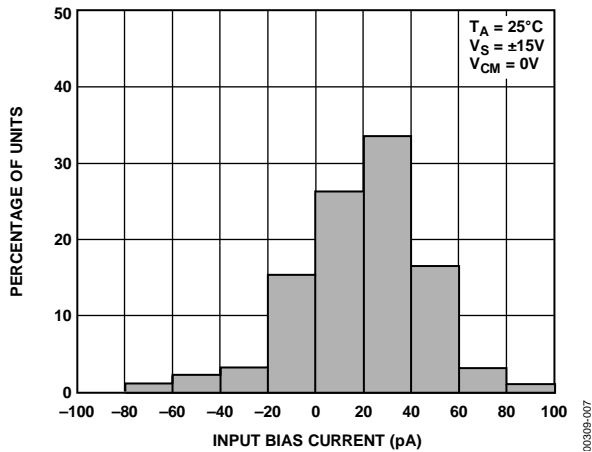


Figure 6. Typical Distribution of Input Bias Current

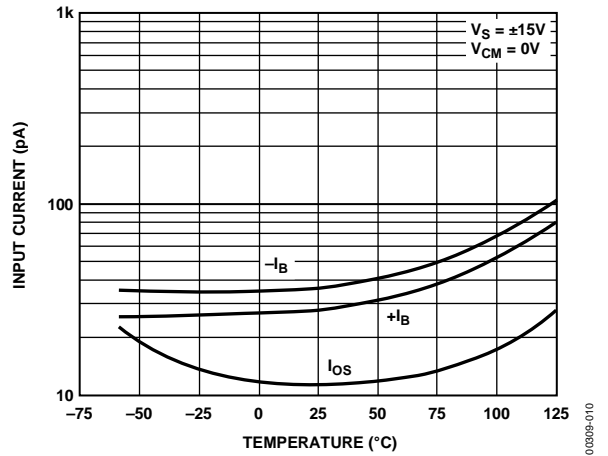


Figure 9. Input Bias, Offset Current vs. Temperature

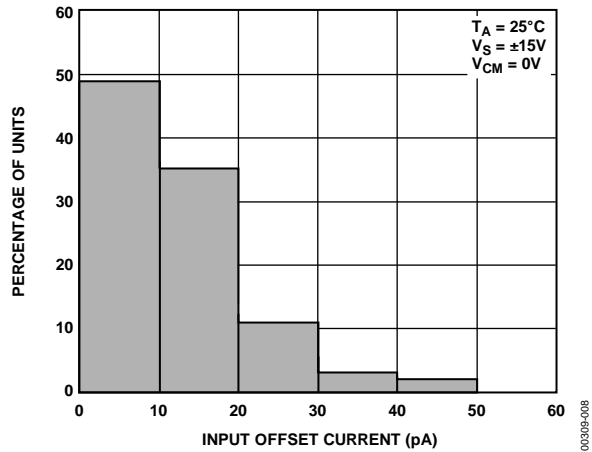


Figure 7. Typical Distribution of Input Offset Current

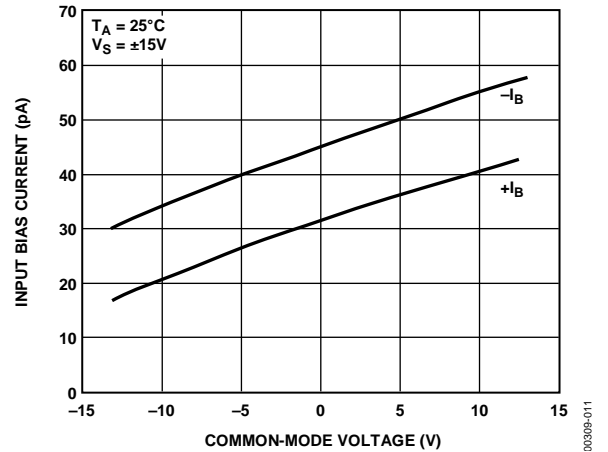


Figure 10. Input Bias Current vs. Common-Mode Voltage

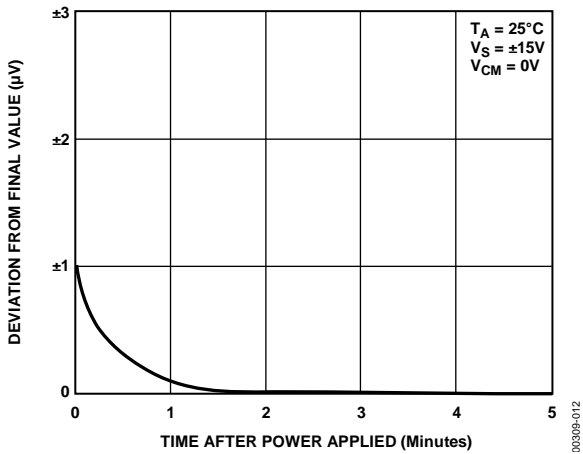


Figure 11. Input Offset Voltage Warm-Up Drift

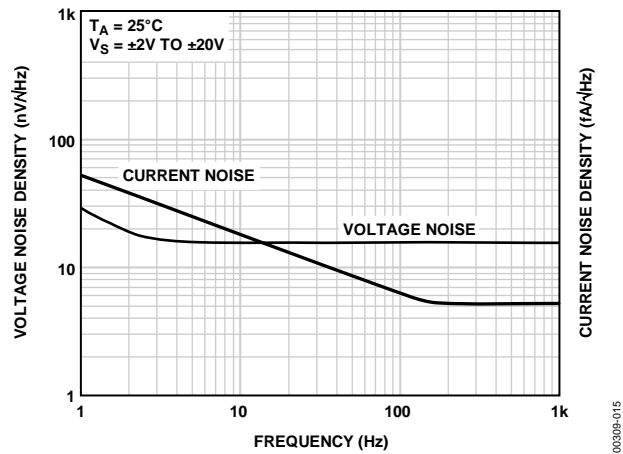


Figure 14. Voltage Noise Density vs. Frequency

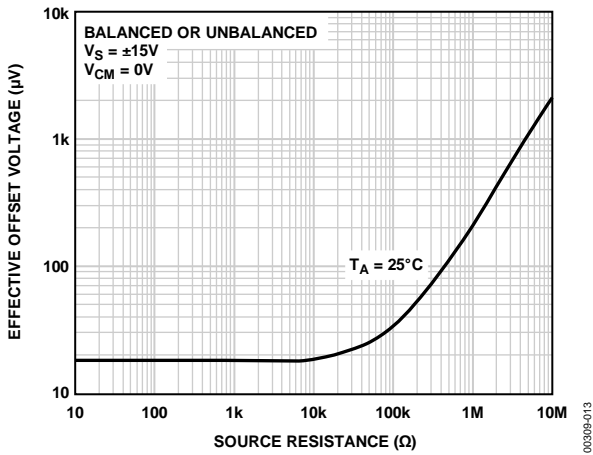


Figure 12. Effective Offset Voltage vs. Source Resistance

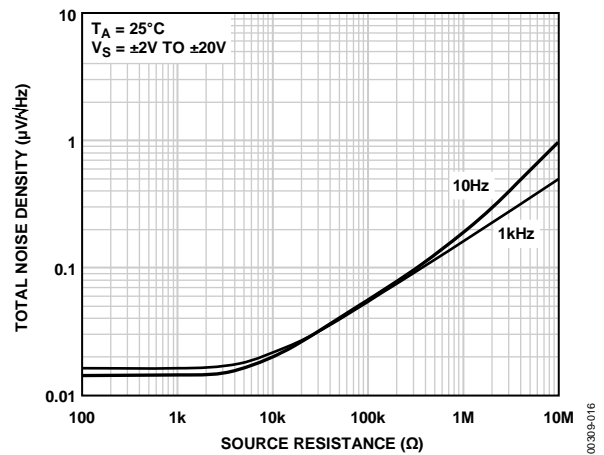


Figure 15. Total Noise Density vs. Source Resistance

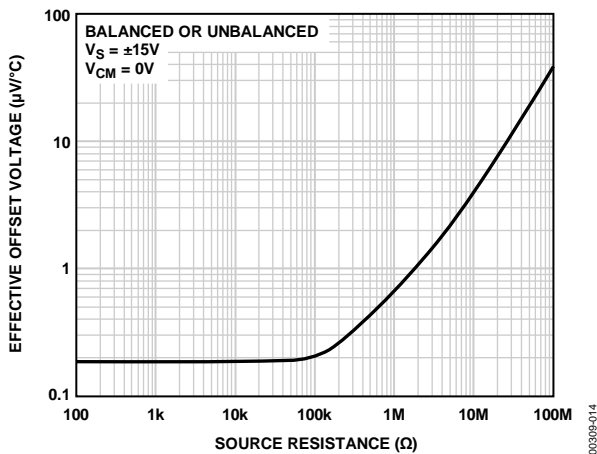


Figure 13. Effective  $TCV_{OS}$  vs. Source Resistance

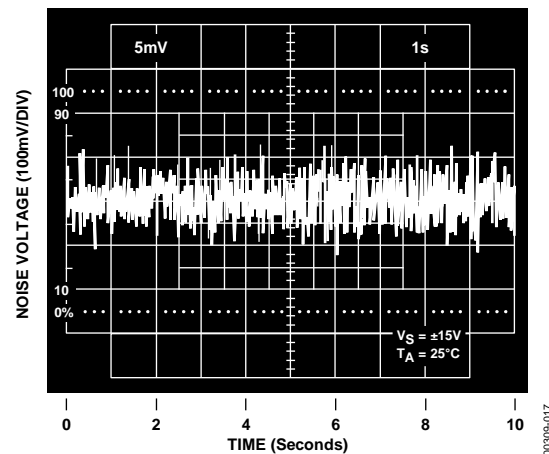


Figure 16. 0.1 Hz to 10 Hz Noise Voltage

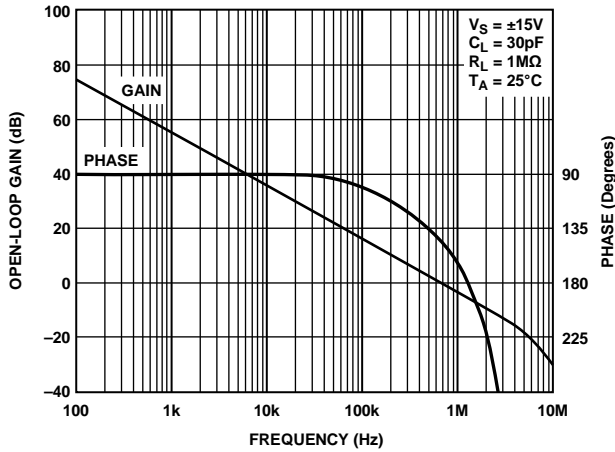


Figure 17. Open-Loop Gain and Phase vs. Frequency

00309-018

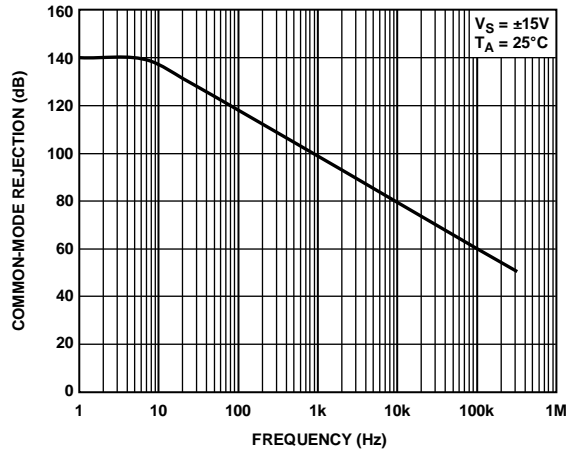


Figure 20. Common-Mode Rejection vs. Frequency

00309-021

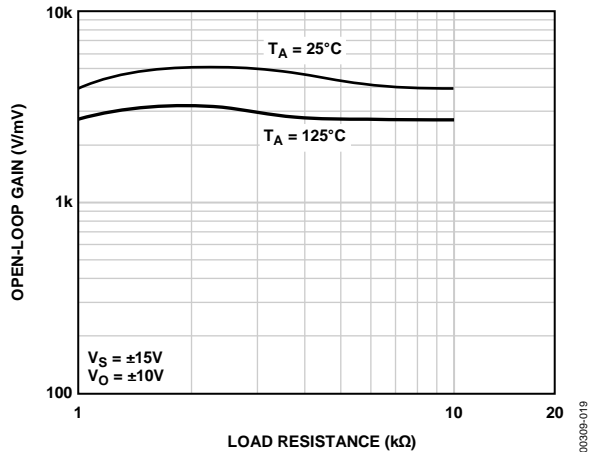


Figure 18. Open-Loop Gain vs. Load Resistance

00309-019

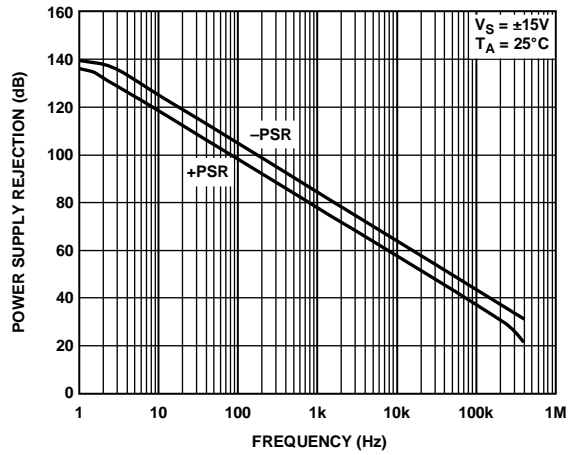


Figure 21. Power Supply Rejection vs. Frequency

00309-022

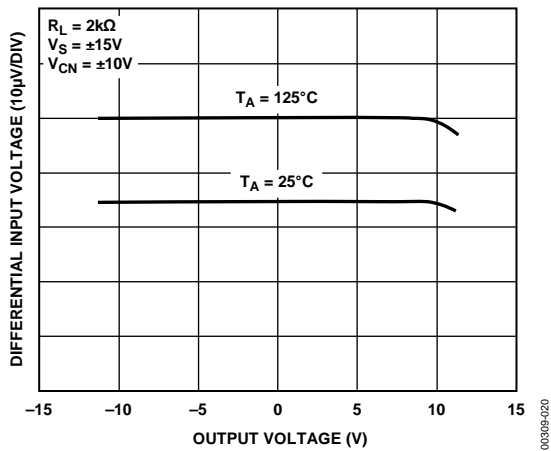


Figure 19. Open-Loop Gain Linearity

00309-020

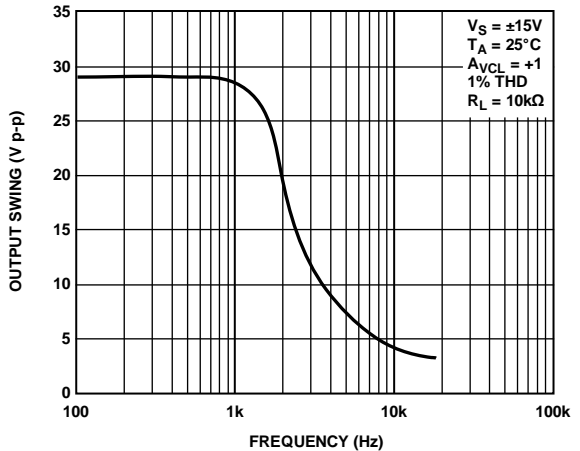


Figure 22. Maximum Output Swing vs. Frequency

00309-023

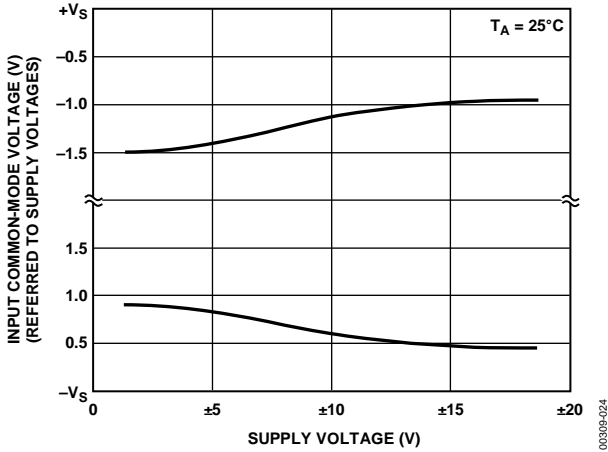


Figure 23. Input Common-Mode Voltage Range vs. Supply Voltage

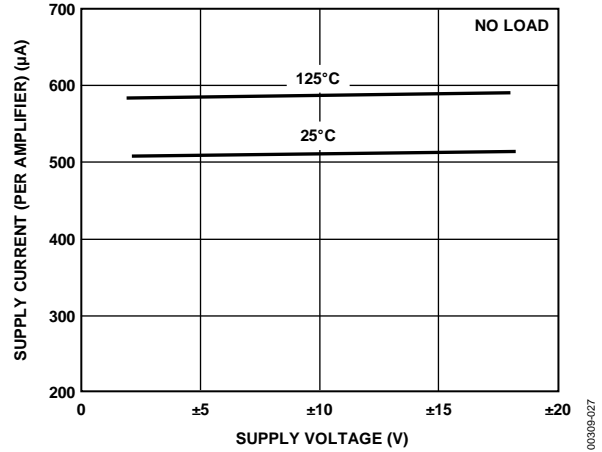


Figure 26. Supply Current (per Amplifier) vs. Supply Voltage

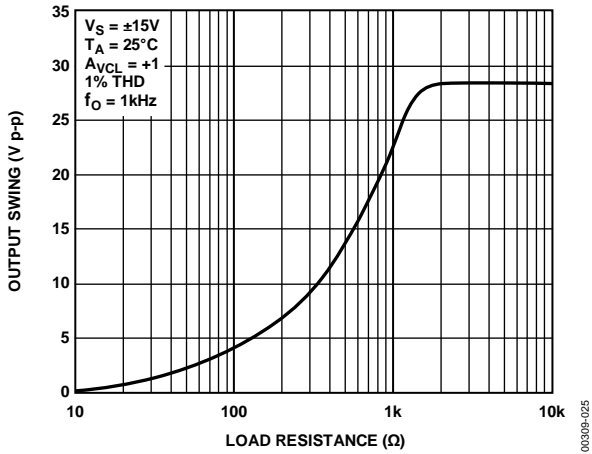


Figure 24. Maximum Output Swing vs. Load Resistance

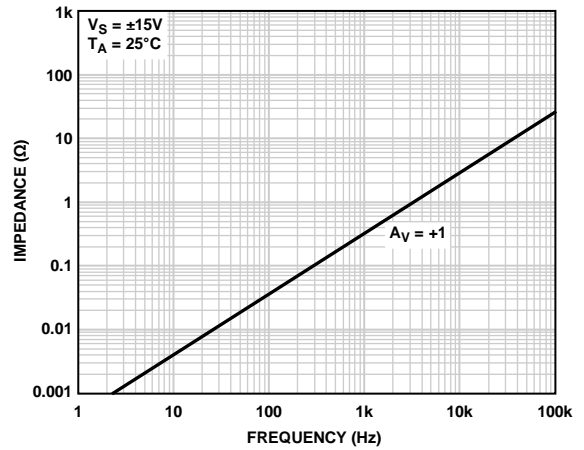


Figure 27. Closed-Loop Output Impedance vs. Frequency

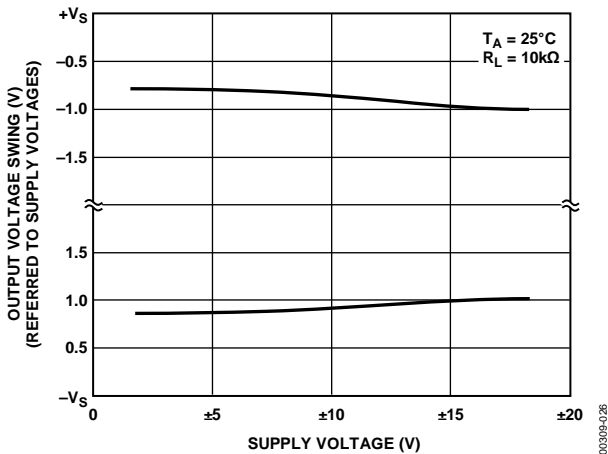


Figure 25. Output Voltage Swing vs. Supply Voltage

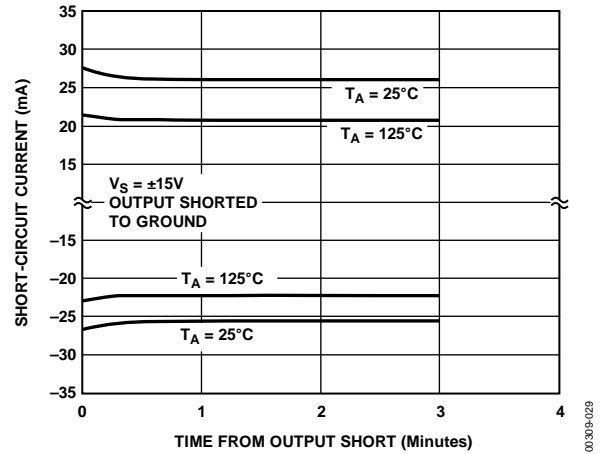


Figure 28. Short-Circuit Current vs. Time at Various Temperatures

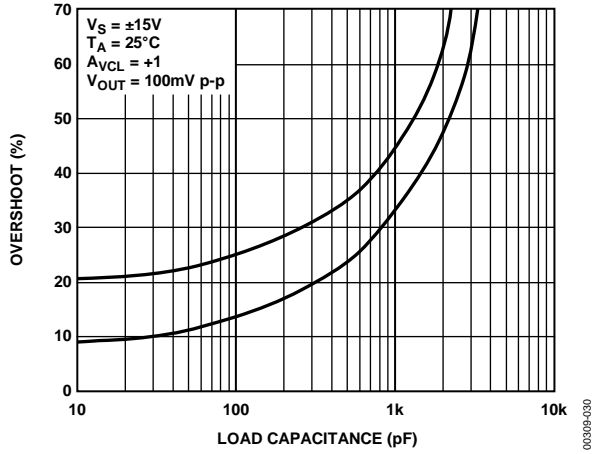


Figure 29. Small-Signal Overshoot vs. Load Capacitance



## APPLICATIONS INFORMATION

Extremely low bias current makes the OP497 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the OP497. High source resistance, even when unbalanced, only minimally degrades the offset voltage and  $TCV_{os}$ .

The input pins of the OP497 are protected against large differential voltage by back-to-back diodes and current-limiting resistors. Common-mode voltages at the inputs are not restricted and may vary over the full range of the supply voltages used.

The OP497 requires very little operating headroom about the supply rails and is specified for operation with supplies as low as  $\pm 2$  V. Typically, the common-mode range extends to within 1 V of either rail. When using a 10 k $\Omega$  load, the output typically swings to within 1 V of the rails.

## AC PERFORMANCE

The ac characteristics of the OP497 are highly stable over its full operating temperature range. Figure 30 shows the unity-gain small signal response. Extremely tolerant of capacitive loading on the output, the OP497 displays excellent response even with 1000 pF loads (see Figure 31).

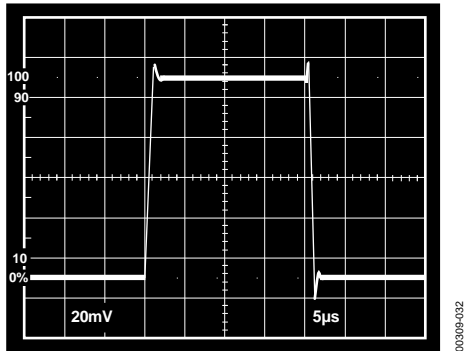


Figure 30. Small Signal Transient Response ( $C_{LOAD} = 100$  pF,  $A_{VCL} = +1$ )

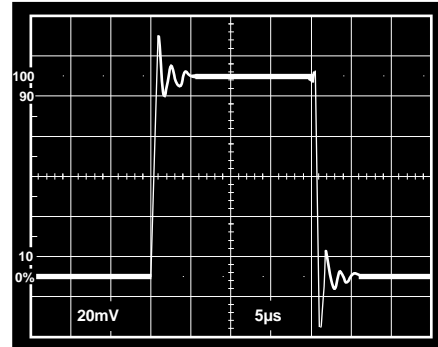


Figure 31. Small Signal Transient Response ( $C_{LOAD} = 1000$  pF,  $A_{VCL} = +1$ )

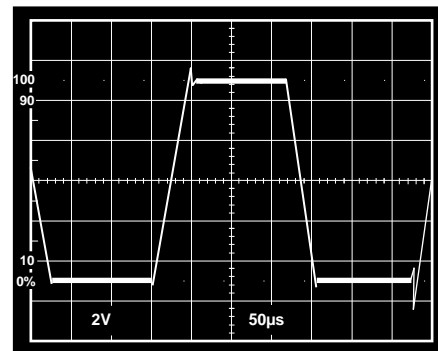


Figure 32. Large Signal Transient Response ( $A_{VCL} = +1$ )

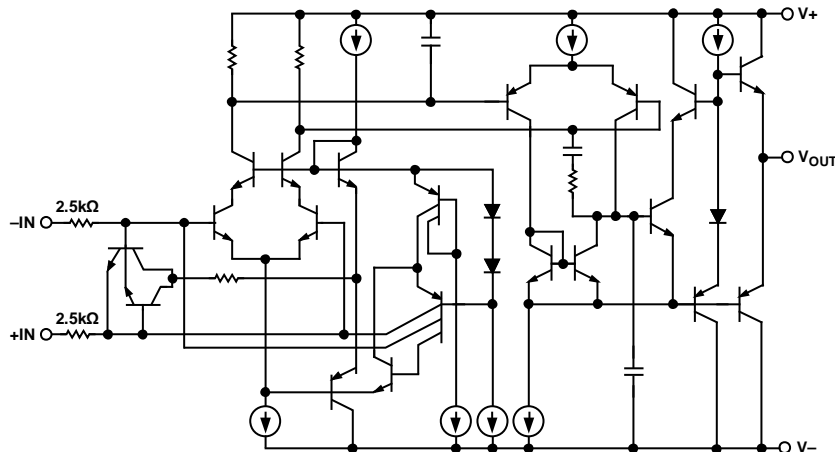


Figure 33. Simplified Schematic Showing One Amplifier

**GUARDING AND SHIELDING**

To maintain the extremely high input impedances of the OP497, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PCB can have 100 pA of leakage currents between adjacent traces; therefore, use guard rings around the inputs. Guard traces are operated at a voltage close to that on the inputs, as shown in Figure 34, so that leakage currents become minimal. In noninverting applications, connect the guard ring to the common-mode voltage at the inverting input. In inverting applications, both inputs remain at ground; therefore, the guard trace should be grounded. Place guard traces on both sides of the circuit board.

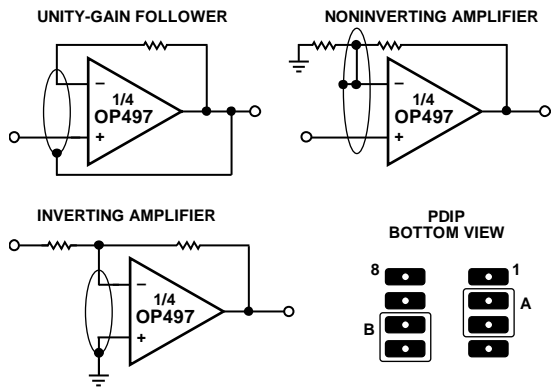


Figure 34. Guard Ring Layout and Connections

**OPEN-LOOP GAIN LINEARITY**

The OP497 has both an extremely high gain of 2000 V/mV typical and constant gain linearity. This enhances the precision of the OP497 and provides for very high accuracy in high closed-loop gain applications. Figure 35 illustrates the typical open-loop gain linearity of the OP497.

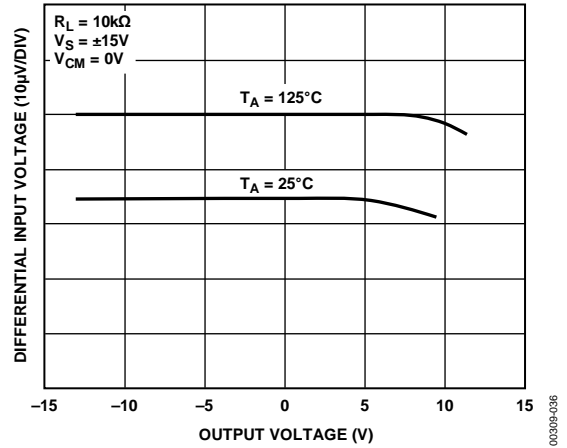


Figure 35. Open-Loop Gain Linearity

## APPLICATIONS CIRCUIT

### PRECISION ABSOLUTE VALUE AMPLIFIER

The circuit in Figure 36 is a precision absolute value amplifier with an input impedance of 30 M $\Omega$ . The high gain and low TC $V_{OS}$  of the OP497 ensure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP497 exceeds 120 dB, yielding an error of less than 2 ppm.

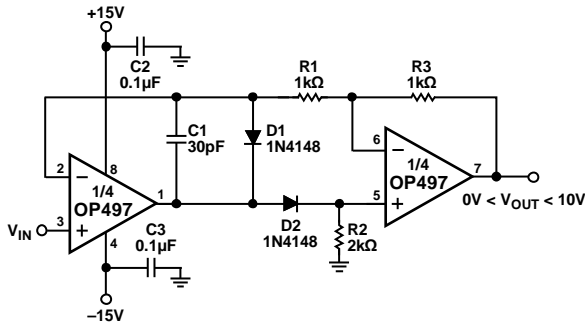


Figure 36. Precision Absolute Value Amplifier

### PRECISION CURRENT PUMP

Maximum output current of the precision current pump shown in Figure 37 is  $\pm 10$  mA. Voltage compliance is  $\pm 10$  V with  $\pm 15$  V supplies. Output impedance of the current transmitter exceeds 3 M $\Omega$  with linearity better than 16 bits.

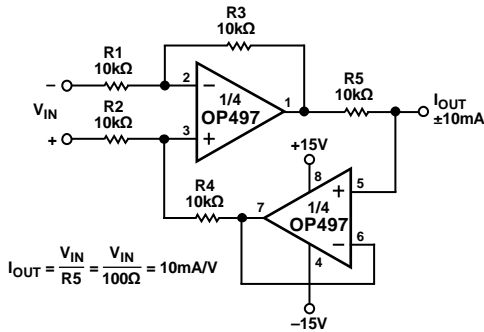


Figure 37. Precision Current Pump

### PRECISION POSITIVE PEAK DETECTOR

In Figure 38, the  $C_H$  must be of polystyrene, Teflon<sup>®</sup>, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of  $C_H$  and the bias current of the OP497.

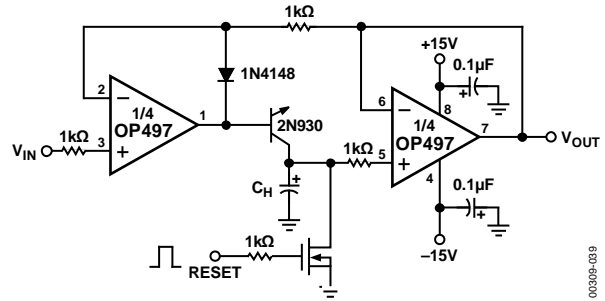


Figure 38. Precision Positive Peak Detector

### SIMPLE BRIDGE CONDITIONING AMPLIFIER

Figure 39 shows a simple bridge conditioning amplifier using the OP497. The transfer function is

$$V_{OUT} = V_{REF} \left( \frac{\Delta R}{R + \Delta R} \right) \frac{R_F}{R}$$

The REF43 provides an accurate and stable reference voltage for the bridge. To maintain the highest circuit accuracy,  $R_F$  should be 0.1% or better with a low temperature coefficient.

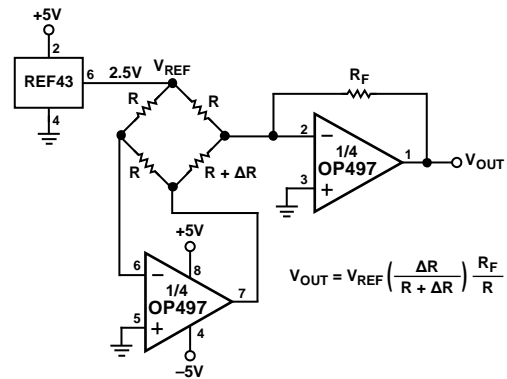


Figure 39. Simple Bridge Conditioning Amplifier Using the OP497

**NONLINEAR CIRCUITS**

Due to its low input bias currents, the OP497 is an ideal log amplifier in nonlinear circuits, such as the squaring amplifier and square root amplifier circuits shown in Figure 40 and Figure 41. Using the squaring amplifier circuit in Figure 40 as an example, the analysis begins by writing a voltage loop equation across Transistors Q1, Q2, Q3, and Q4.

$$V_{T1}I_n\left(\frac{I_{IN}}{I_{S1}}\right) + V_{T2}I_n\left(\frac{I_{IN}}{I_{S2}}\right) = V_{T3}I_n\left(\frac{I_{O}}{I_{S3}}\right) + V_{T4}I_n\left(\frac{I_{REF}}{I_{S4}}\right)$$

All the transistors in the MAT04 are precisely matched and at the same temperature; therefore, the  $I_S$  and  $V_T$  terms cancel, giving

$$2InI_{IN} = InI_O + InI_{REF} = In(I_O \times I_{REF})$$

Exponentiating both sides of the thick equation lead to

$$I_O = \frac{(I_{IN})^2}{I_{REF}}$$

Op amp A2 forms a current-to-voltage converter which results in  $V_{OUT} = R2 \times I_O$ . Substituting  $(V_{IN}/R1)$  for  $I_{IN}$  and the previous equation for  $I_O$  yields

$$V_{OUT} = \left(\frac{R2}{I_{REF}}\right)\left(\frac{V_{IN}}{R1}\right)^2$$

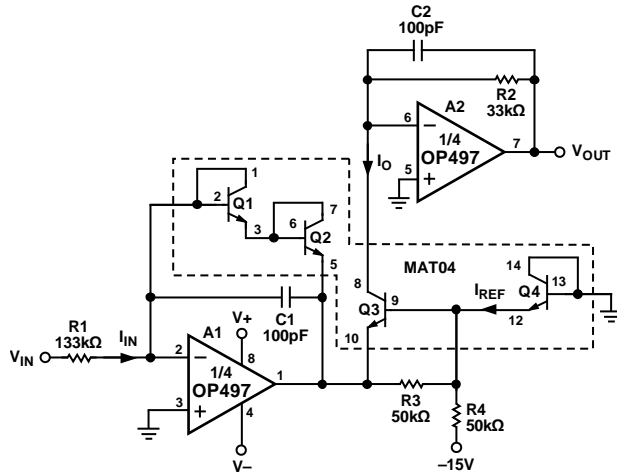


Figure 40. Squaring Amplifier

A similar analysis made for the square root amplifier circuit in Figure 41 leads to its transfer function

$$V_{OUT} = R2\sqrt{\frac{(V_{IN})(I_{REF})}{R1}}$$

In these circuits,  $I_{REF}$  is a function of the negative power supply. To maintain accuracy, the negative supply should be well regulated. For applications where very high accuracy is required, a voltage reference can be used to set  $I_{REF}$ . An important consideration for the squaring circuit is that a sufficiently large input voltage can force the output beyond the operating range of the output op amp. Resistor R4 can be changed to scale  $I_{REF}$ , or R1 and R2 can be varied to keep the output voltage within the usable range.

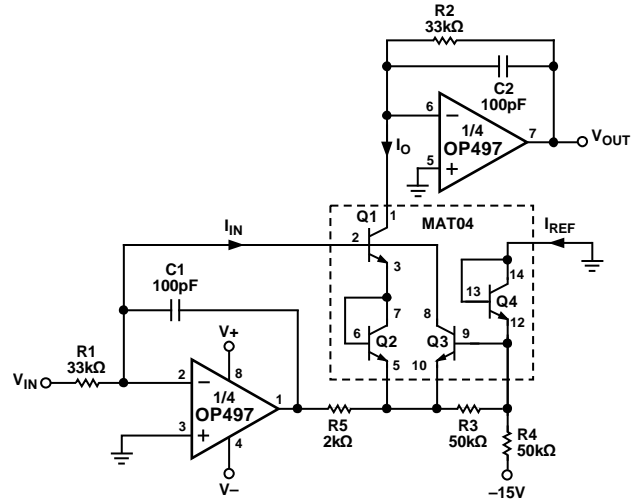
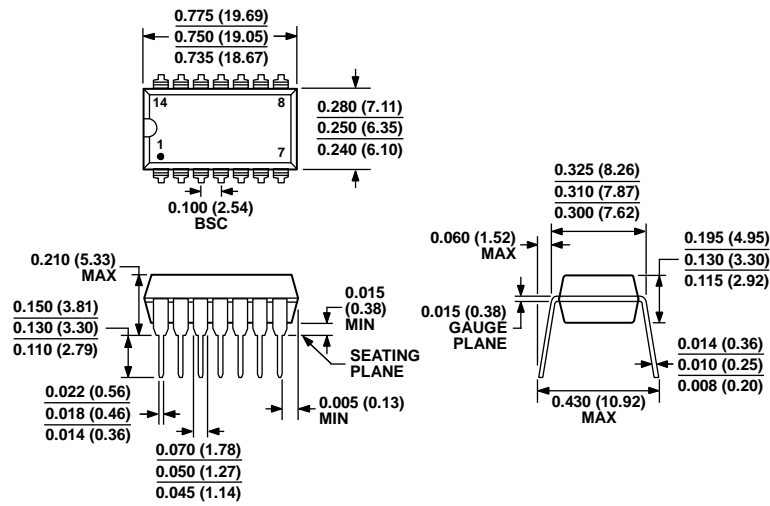


Figure 41. Square Root Amplifier

Unadjusted accuracy of the square root circuit is better than 0.1% over an input voltage range of 100 mV to 10 V. For a similar input voltage range, the accuracy of the squaring circuit is better than 0.5%.

OUTLINE DIMENSIONS

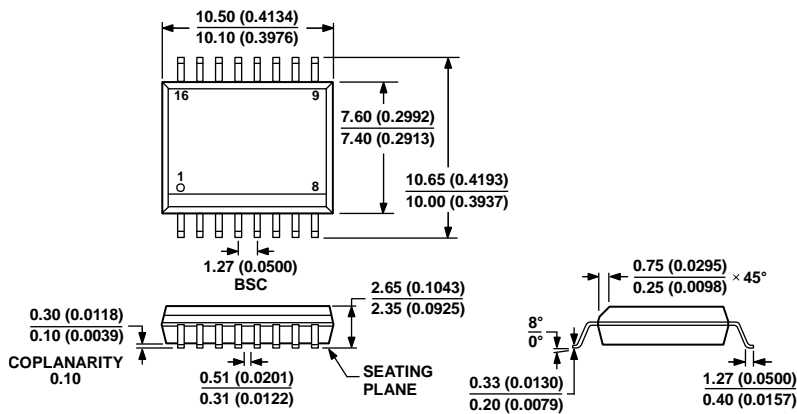


COMPLIANT TO JEDEC STANDARDS MS-001  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 42. 14-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-14)

Dimensions shown in inches and (millimeters)

070606-A



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 43. 16-Lead Standard Small Outline Package [SOIC\_W] Wide Body (RW-16)

Dimensions shown in millimeters and (inches)

032707-B

**ORDERING GUIDE**

<b>Model</b>	<b>Temperature Range</b>	<b>Package Description</b>	<b>Package Option</b>
OP497FP	-40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
OP497FPZ <sup>1</sup>	-40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
OP497GP	-40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
OP497GPZ <sup>1</sup>	-40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
OP497FS	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
OP497FS-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
OP497FSZ <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
OP497FSZ-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
OP497GS	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
OP497GS-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
OP497GSZ <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
OP497GSZ-REEL <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16

<sup>1</sup> Z = RoHS Compliant Part.

**OP497**

**NOTES**

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