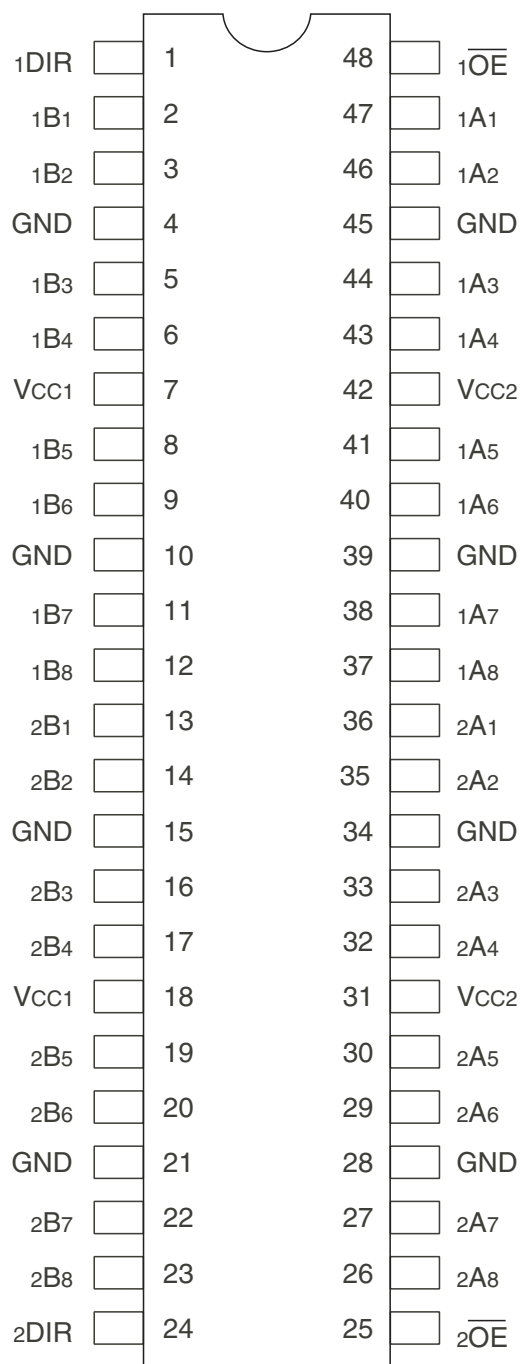


PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

POWER SUPPLY SEQUENCING

In the 74FCT164245T, the condition of $V_{CC1} \geq (V_{CC2} - 0.5V)$ must be maintained at all times. For the range of $V_{CC1} = (V_{CC2} - 0.5V)$ to $V_{CC1} = (V_{CC2} + 0.9V)$, both the A and B ports will remain in a High-Impedance state.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC1}+0.5$	V
T_A	Operating Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1	W
I_{OUT}	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All devices except V_{CC2} .
- Power supply terminal V_{CC2} .

CAPACITANCE ($T_A = +25^\circ\text{C}$, $F = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	3.5	6	pF
$C_{I/O}$	I/O Capacitance	$V_{OUT} = 0V$	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
\overline{xOE}	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
\overline{xOE}	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT, 3.3V)

Following Conditions Apply Unless Otherwise Specified:

VCC1 = 5V ±10%, VCC2 = 2.7V to 3.6V, Industrial: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level	2	—	5.5	V
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	VCC1 = Max. V _I = 5.5V	—	—	±5	μA
	Input HIGH Current (I/O pins)	VCC2 = Max. V _I = VCC2	—	—	±15	
I _{IL}	Input LOW Current (Input pins)	V _I = GND	—	—	±5	
	Input LOW Current (I/O pins)	V _I = GND	—	—	±15	
V _{IK}	Clamp Diode Voltage	VCC2 = Min., I _{IN} = -18mA	—	-0.7	-1.2	V
V _{OH}	Output HIGH Voltage	VCC1 = VCC2 = Min. V _{IN} = V _{IH} or V _{IL} I _{OH} = -0.1mA	VCC2 -0.2	—	—	V
		VCC2 = 3V V _{IN} = V _{IH} or V _{IL} I _{OH} = -8mA	2.4	3	—	
V _{OL}	Output LOW Voltage	VCC1 = Min. VCC2 = Min. V _{IN} = V _{IH} or V _{IL} I _{OL} = 0.1mA	—	—	0.2	V
		I _{OL} = 16mA	—	0.2	0.4	
		I _{OL} = 24mA	—	0.3	0.55	
		VCC = 3V V _{IN} = V _{IH} or V _{IL} I _{OL} = 24mA	—	0.3	0.5	
I _{OFF}	Input/Output Power Off Leakage	VCC1 = 0V, VCC2 = 0V, V _{IN} or V _O ≤ 4.5V	—	—	±100	μA
I _{OS}	Short Circuit Current ⁽⁴⁾	VCC1 = Max., VCC2 = Max., V _O = GND ⁽³⁾	-70	-105	-150	mA
I _O	Output Drive Current	VCC1 = Max., VCC2 = Max., V _O = 1.5V ⁽³⁾	-40	-60	-90	mA
V _H	Input Hysteresis	—	—	150	—	mV
I _{CC2L} I _{CC2H} I _{CC2Z}	Quiescent Power Supply Current	VCC1 = Max. VCC2 = Max. V _{IN} = GND or VCC2	—	0.35	2	mA

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC1 = 5V, VCC2 = 3.3V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (B PORT, 5V)

Following Conditions Apply Unless Otherwise Specified:

V_{CC1} = 5V ±10%, V_{CC2} = 2.7V to 3.6V, Industrial: T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level	2	—	5.5	V
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	V _{CC1} = Max. V _I = V _{CC1}	—	—	±5	μA
	Input HIGH Current (I/O pins)	V _{CC2} = Max.	—	—	±15	
I _{IL}	Input LOW Current (Input pins)	V _I = GND	—	—	±5	
	Input LOW Current (I/O pins)		—	—	±15	
V _{IK}	Clamp Diode Voltage	V _{CC1} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V
V _{OH}	Output HIGH Voltage	V _{CC1} = Min. I _{OH} = -3mA	2.5	3.5	—	V
		V _{CC2} = Min. I _{OH} = -15mA	2.4	3.5	—	
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -32mA ⁽⁵⁾	2	3	—	
V _{OL}	Output LOW Voltage	V _{CC1} = Min. V _{CC2} = Min. V _{IN} = V _{IH} or V _{IL} I _{OL} = 64mA	—	0.2	0.55	V
I _{OFF}	Input/Output Power Off Leakage	V _{CC1} = 0V, V _{CC2} = 0V, V _{IN} or V _O ≤ 4.5V	—	—	±100	μA
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC1} = Max., V _{CC2} = Max., V _O = GND ⁽³⁾	-80	-140	-225	mA
I _O	Output Drive Current	V _{CC1} = Max., V _{CC2} = Max., V _O = 2.5V ⁽³⁾	-50	-75	-180	mA
V _H	Input Hysteresis	—	—	150	—	mV
I _{CC1L} I _{CC1H} I _{CC1Z}	Quiescent Power Supply Current	V _{CC1} = Max. V _{CC2} = Max. V _{IN} = GND or V _{CC2}	—	0.08	1.5	mA

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1} = 5V, V_{CC2} = 3.3V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. Duration of the condition cannot exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC1} = \text{Max.}, V_{CC2} = \text{Max.}$ $V_{IN} = V_{CC2} - 0.6V^{(3)}$		—	12	30	μA
I_{CCD}	Dynamic Power Supply Current(4)	$V_{CC1} = \text{Max.}, V_{CC2} = \text{Max.}$ Outputs Open $\overline{xOE} = xDIR = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC2}$ $V_{IN} = GND$	—	75	120	$\mu A/$ MHz
I_C	Total Power Supply Current(6)	$V_{CC1} = \text{Max.}, V_{CC2} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = GND$ One Bit Toggling	$V_{IN} = V_{CC2} - 0.6V$ $V_{IN} = GND$	—	1.2	4.7	mA
		$V_{CC1} = \text{Max.}, V_{CC2} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = GND$ Sixteen Bits Toggling	$V_{IN} = V_{CC2} - 0.6V$ $V_{IN} = GND$	—	3.5	8.5(5)	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC1} = 5V, V_{CC2} = 3.3V, +25^\circ C$ ambient.
- Per TTL driven input. All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC1} + I_{CC2} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC1} = \text{Quiescent Current (} I_{CC1L}, I_{CC1H} \text{ and } I_{CC1Z})$
 $I_{CC2} = \text{Quiescent Current (} I_{CC2L}, I_{CC2H} \text{ and } I_{CC2Z})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

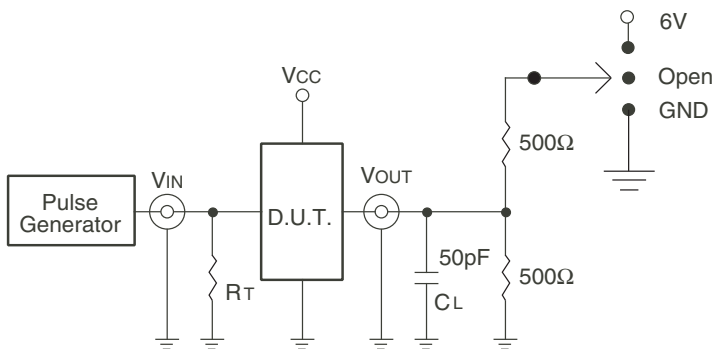
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter	Condition ⁽¹⁾	Min. ⁽²⁾	Max.	Unit
t _{PLH} t _{PHL}	Propagation Delay A to B	CL = 50pF RL = 500Ω	1.5	5	ns
t _{PLH} t _{PHL}	Propagation Delay B to A		1.5	5	ns
t _{PZH} t _{PZL}	Output Enable Time x \overline{OE} to B		1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time x \overline{OE} to B		1.5	6	ns
t _{PZH} t _{PZL}	Output Enable Time x \overline{OE} to A		1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time x \overline{OE} to A		1.5	6	ns
t _{PZH} t _{PZL}	Output Enable Time xDIR to B ⁽³⁾		1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time xDIR to B ⁽³⁾		1.5	6	ns
t _{PZH} t _{PZL}	Output Enable Time xDIR to A ⁽³⁾		1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time xDIR to A ⁽³⁾		1.5	6	ns

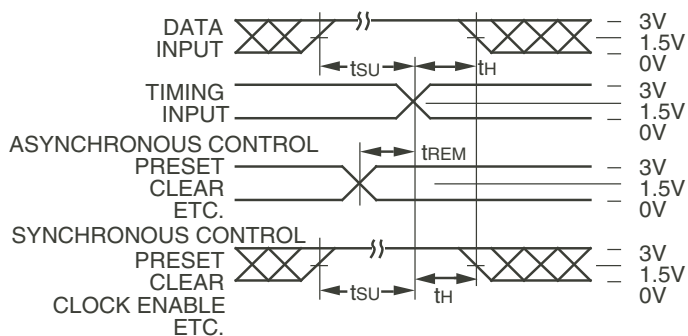
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

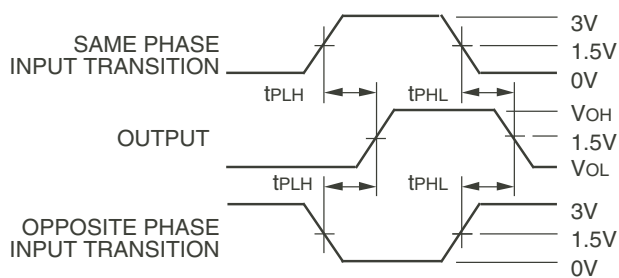
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



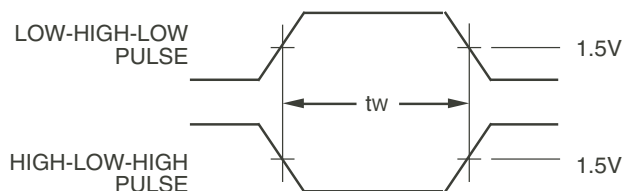
Propagation Delay

SWITCH POSITION

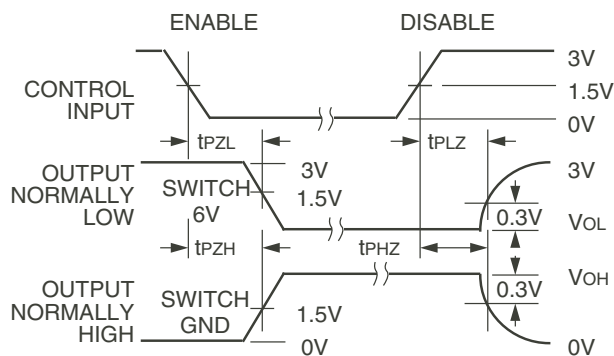
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

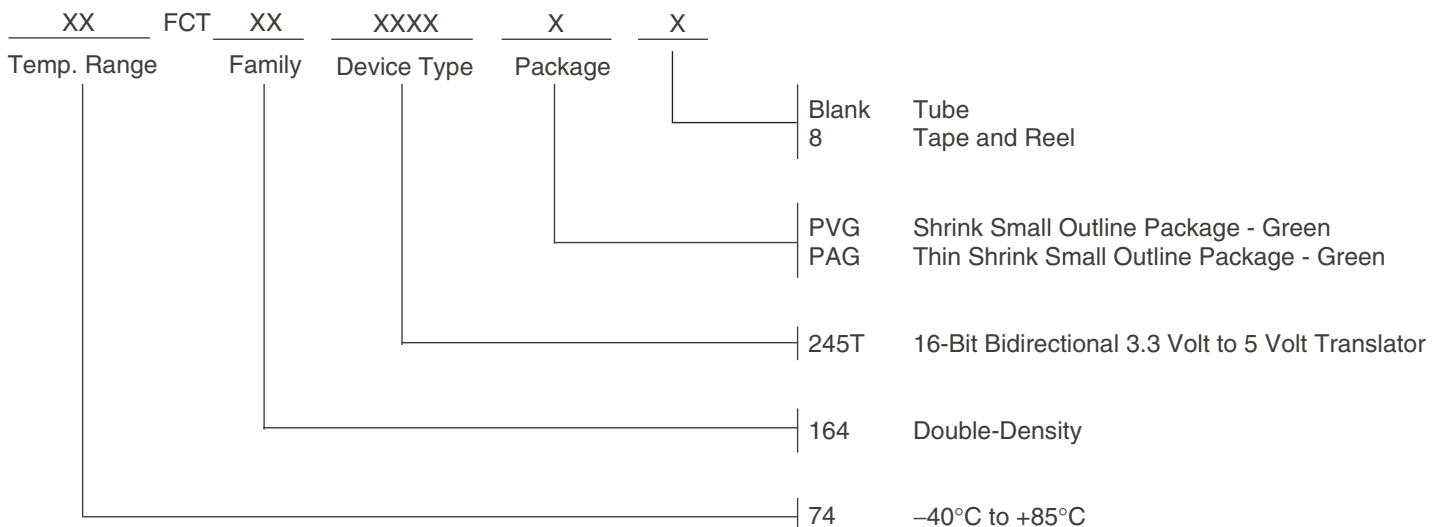


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

09/28/2009	pg. 8	Updated the ordering information by removing the "IDT" notation and non RoHS part.
04/30/2015	pgs. 3, 4 and 8	Updated typo in DC Electrical Characteristics table and updated ordering information by adding Tape & Reel.
05/12/2016	pgs. 8	Corrected temperature symbol and removed Tray from ordering information.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Renesas Electronics:](#)

[74FCT164245TPAG8](#) [74FCT164245TPVG8](#) [74FCT164245TPAG](#) [74FCT164245TPVG](#)