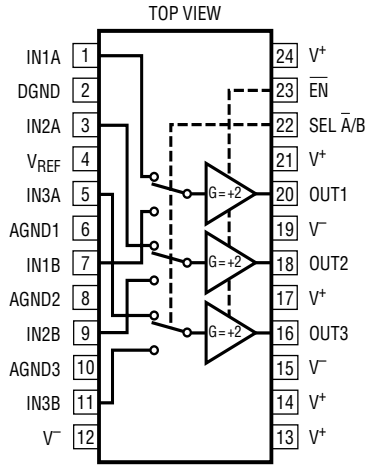
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) ..... ±10mA
Output Current (Continuous) ..... ±70mA
$\overline{EN}$ to DGND Voltage (Note 2) 5.5V
SEL to DGND Voltage (Note 2) 8V
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) ... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C

Junction Temperature
SSOP ..... 150°C
QFN ..... 125°C
Storage Temperature Range
SSOP ..... –65°C to 150°C
QFN ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
SSOP ..... 300°C

PACKAGE/ORDER INFORMATION

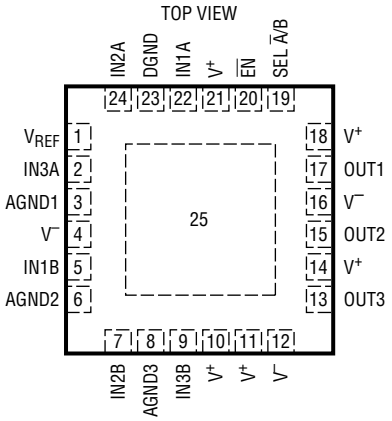


GN PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER PART NUMBER

LT6555CGN
LT6555IGN



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 2.6°C/W
EXPOSED PAD (PIN 25) IS V^-
MUST BE SOLDERED TO PCB

ORDER PART NUMBER

LT6555CUF
LT6555IUF

UF PART* MARKING

6555

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, R_L = 150Ω, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{AGND}, V_{DGND}, V_{VREF} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Referred Offset Voltage	V_{IN} = 0V, V_{OS} = V_{OUT}/2	 ●		5	±16 ±24	mV mV
I_{IN}	Input Current		●		–17	±45	µA
R_{IN}	Input Resistance	V_{IN} = ±1V	●	100	400		kΩ
C_{IN}	Input Capacitance	f = 100kHz			1		pF
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±6V (Note 6)	●	56	62		dB
I_{PSRR}	Input Current Power Supply Rejection	V_S = ±2.25V to ±6V (Note 6)	●		1	±4	µA/V
A_V ERR	Gain Error	V_{OUT} = ±2V, Nominal Gain 2V/V	●			±2.5	%
A_V MATCH	Gain Matching	Any One Channel to Another			±0.33		%
V_{OUT}	Output Voltage Swing	(Note 7)	 ●	±3.15 ±3.0	±3.4		V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, R_L = 150Ω, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{AGND}, V_{DGND}, V_{VREF} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Supply Current, Per Amplifier	R_L = ∞			9	12	mA
			●			14	mA
	Supply Current, Disabled, Per Amplifier	$V_{\overline{EN}}$ = 4V, R_L = ∞	●		47	500	µA
		$V_{\overline{EN}}$ = Open, R_L = ∞	●		42	500	µA
$I_{\overline{EN}}$	Enable Pin Current	$V_{\overline{EN}}$ = 0.4V	●	–200	–95		µA
		$V_{\overline{EN}}$ = 4V	●	–75	–21		µA
I_{SEL}	Select Pin Current	V_{SEL} = 0.4V	●	–50	–5		µA
		V_{SEL} = 4V	●	–50	–1		µA
I_{SC}	Output Short-Circuit Current	R_L = 0Ω, V_{IN} = ±1V	●	±50	±105		mA
SR	Slew Rate	±1V on ±2.5V Output Step (Note 8)		1600	2200		V/µs
–3dB BW	Small-Signal –3dB Bandwidth	V_{OUT} = 200mV_{P-P}			650		MHz
0.1dB BW	Gain Flatness ±0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}			120		MHz
FPBW	Full Power Bandwidth 2V	V_{OUT} = 2V_{P-P} (Note 9)		250	350		MHz
	Full Power Bandwidth 4V	V_{OUT} = 4V_{P-P} (Note 9)			175		MHz
	All-Hostile Crosstalk	f = 10MHz, V_{IN} = 1V_{P-P}			–72		dB
		f = 100MHz, V_{IN} = 1V_{P-P}			–50		dB
	Selected Channel to Unselected Channel Crosstalk	f = 10MHz, V_{IN} = 1V_{P-P}			–80		dB
		f = 100MHz, V_{IN} = 1V_{P-P}			–55		dB
	Channel Select Output Transient	INA = INB = 0V			200		mV_{P-P}
	Channel-to-Channel Select Time	INA = –1V, INB = 1V from 50% SEL to V_{OUT} = 0V			8		ns
t_S	Settling Time	0.1% of V_{FINAL}, V_{STEP} = 2V			6.5		ns
t_R, t_F	Small-Signal Rise and Fall Time	10% to 90%, V_{OUT} = 400mV_{P-P}			520		ps
dG	Differential Gain	(Note 10)			0.033		%
dP	Differential Phase	(Note 10)			0.022		Deg
HD2	2nd Harmonic Distortion	f = 10MHz, V_{OUT} = 2V_{P-P}			–80		dBc
HD3	3rd Harmonic Distortion	f = 10MHz, V_{OUT} = 2V_{P-P}			–70		dBc

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This parameter is guaranteed to meet specified performance through design and characterization. It is not production tested.

Note 3: As long as output current and junction temperature are kept below the Absolute Maximum Ratings, no damage to the part will occur. Depending on the supply voltage, a heat sink may be required.

Note 4: The LT6555C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT6555C is guaranteed to meet specified performance from 0°C to 70°C. The LT6555C is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA sampled at these temperatures. The LT6555I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: In order to follow the constraints for 4.5V operation for PSRR and I_{PSRR} testing at ±2.25V, the DGND pin is set to V^-, the $\overline{EN}$ pin is set to V^- + 0.4V, and the SEL pin is set to either V^- + 0.4V or V^- + 4V. At ±6V and all other cases, DGND is set to ground and the $\overline{EN}$ and SEL pins are referenced from it.

Note 7: The V_{REF} pin is set to 1V when testing positive swing and –1V when testing negative swing to ensure that the internal input clamps do not limit the output swing.

Note 8: Slew rate is 100% production tested using both inputs of channel 2. Slew rates of channels 1 and 3 are guaranteed through design and characterization.

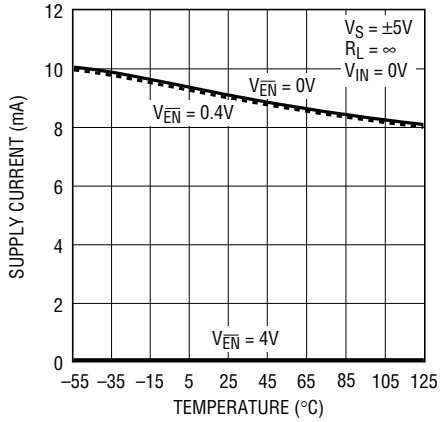
Note 9: Full power bandwidth is calculated from the slew rate:

$FPBW = SR/(\pi \bullet V_{P-P})$

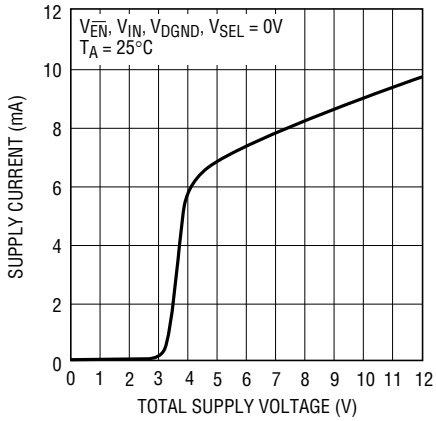
Note 10: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R video measurement set. The resolution of this equipment is better than 0.05% and 0.05°. Nine identical amplifier stages were cascaded giving an effective resolution of better than 0.0056% and 0.0056%.

TYPICAL PERFORMANCE CHARACTERISTICS

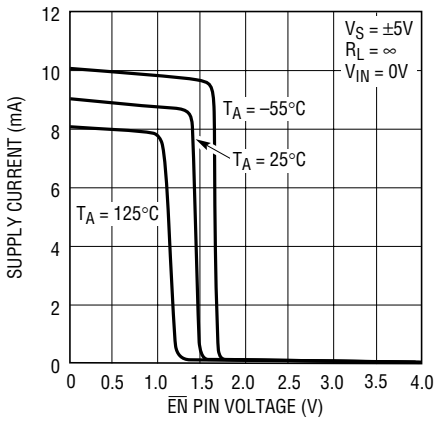
Supply Current per Amplifier vs Temperature



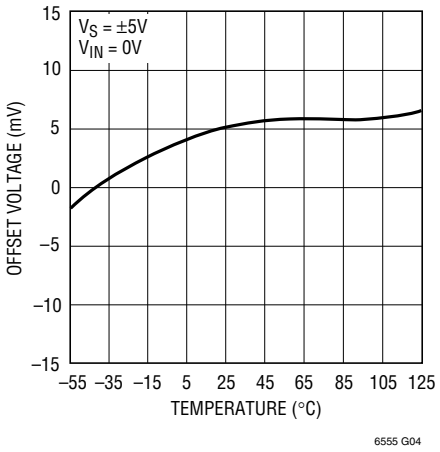
Supply Current per Amplifier vs Supply Voltage



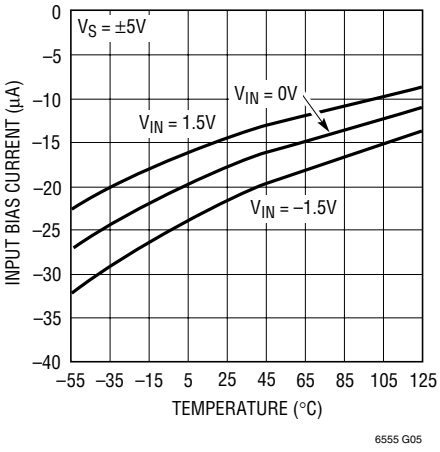
Supply Current per Amplifier vs $\overline{EN}$ Pin Voltage



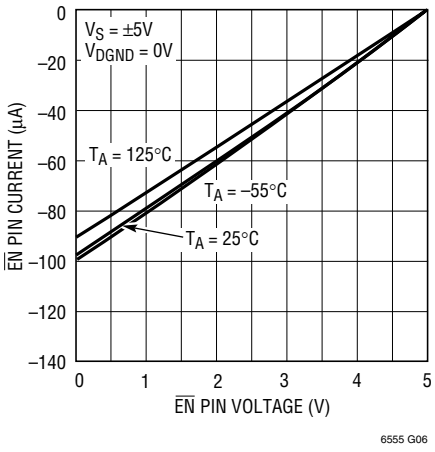
Input Referred Offset Voltage vs Temperature



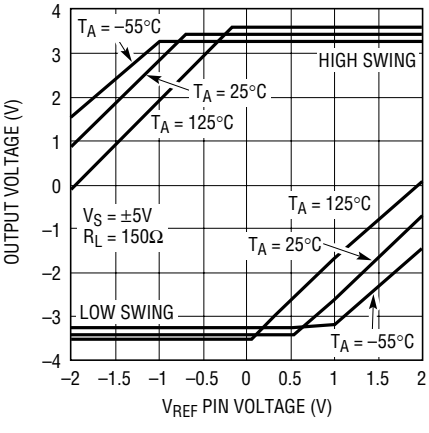
Input Bias Current vs Temperature



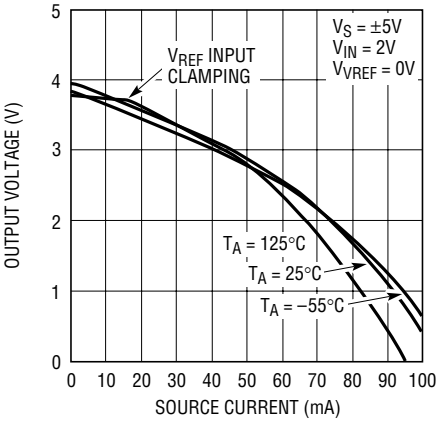
$\overline{EN}$ Pin Current vs $\overline{EN}$ Pin Voltage



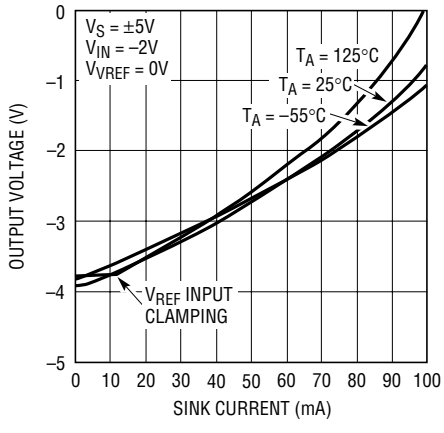
Maximum Output Voltage Swing vs V_{REF} Pin Voltage



Output Voltage Swing vs I_{LOAD} (Output High)

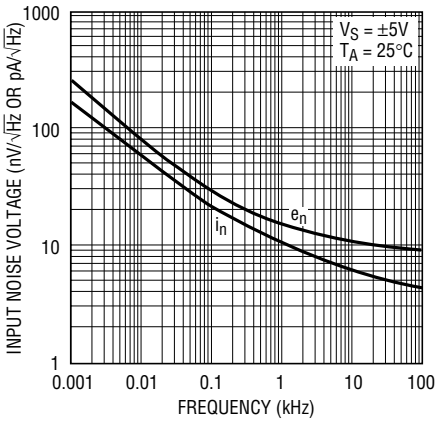


Output Voltage Swing vs I_{LOAD} (Output Low)

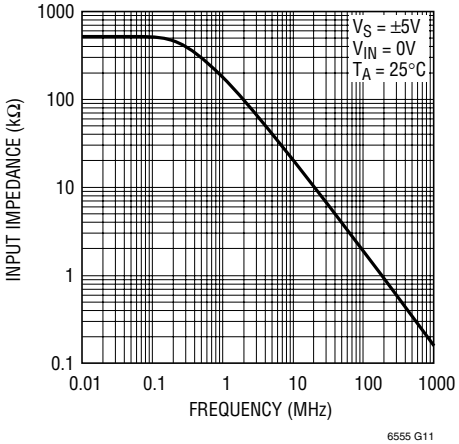


TYPICAL PERFORMANCE CHARACTERISTICS

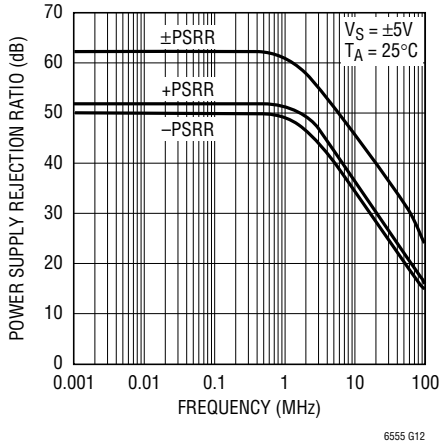
Input Noise Spectral Density



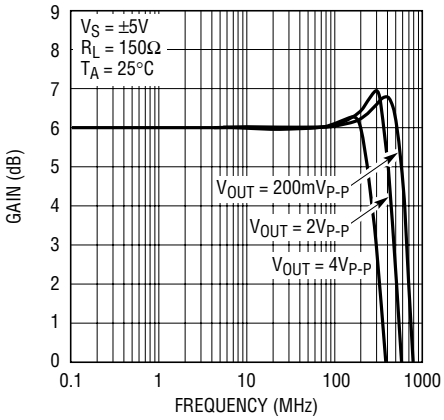
Input Impedance vs Frequency



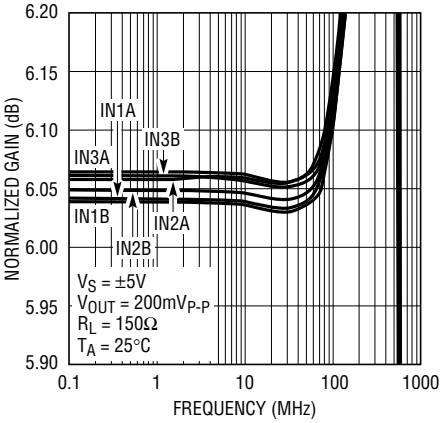
Input Referred PSRR vs Frequency



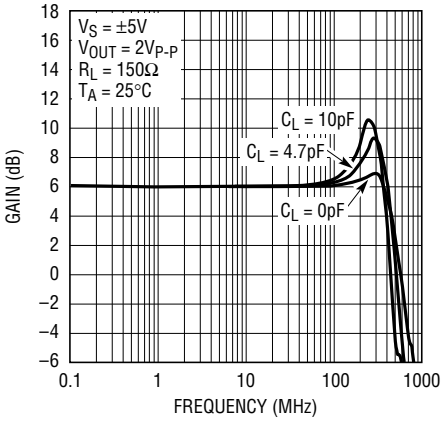
Frequency Response vs Output Amplitude



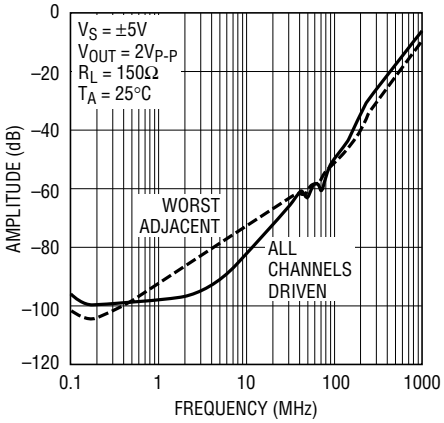
Gain Flatness vs Frequency



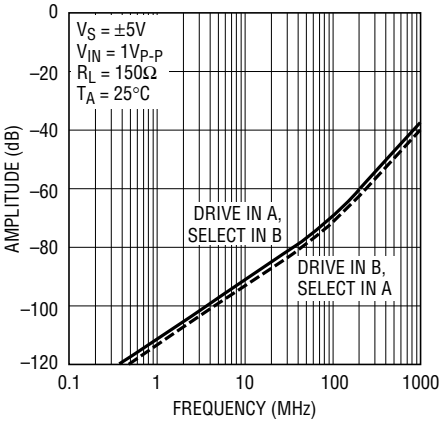
Frequency Response with Capacitive Loads



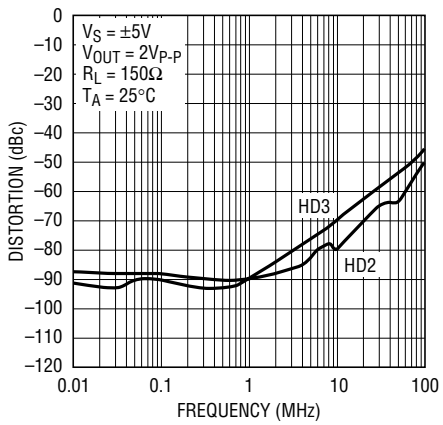
Crosstalk vs Frequency



Crosstalk vs Frequency

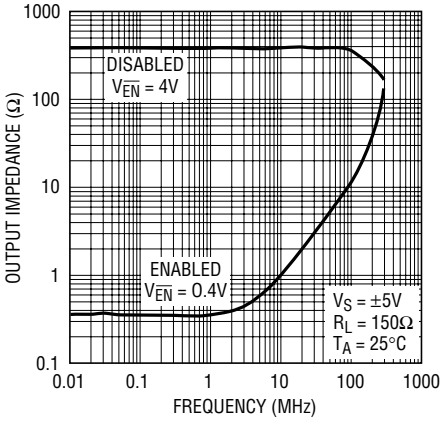


Harmonic Distortion vs Frequency

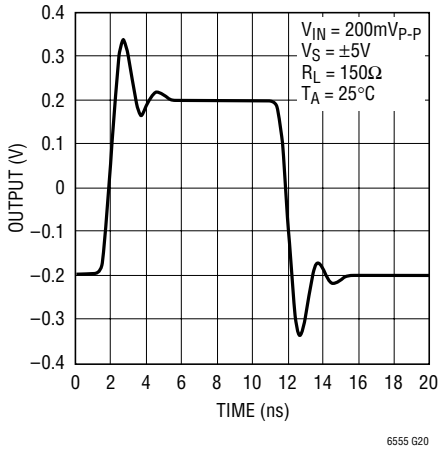


TYPICAL PERFORMANCE CHARACTERISTICS

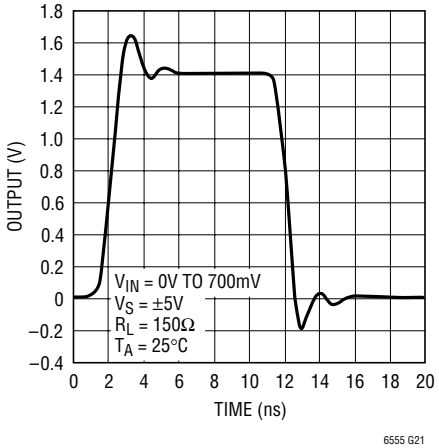
Output Impedance vs Frequency



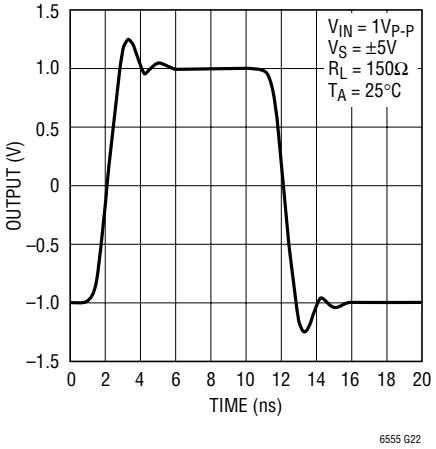
Small-Signal Transient Response



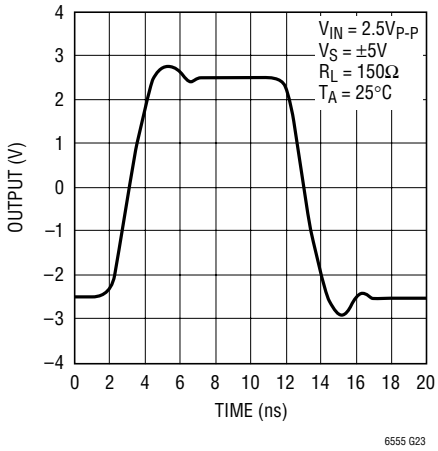
Video Amplitude Transient Response



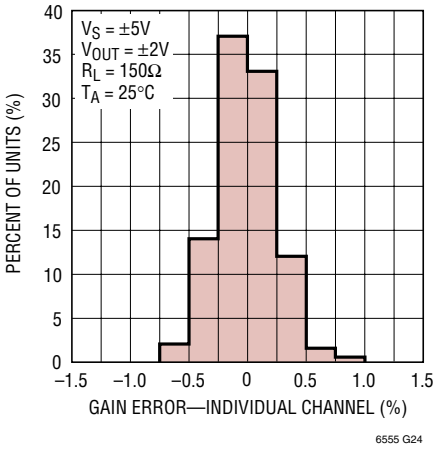
Large-Signal Transient Response



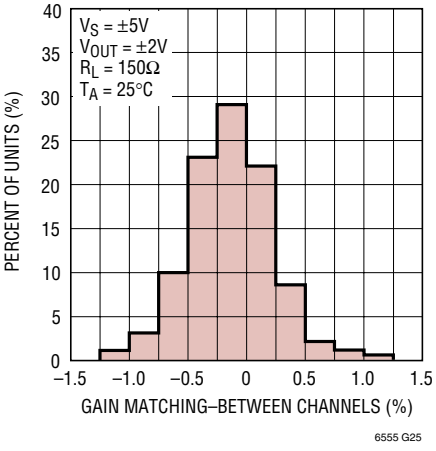
Large-Signal Transient Response



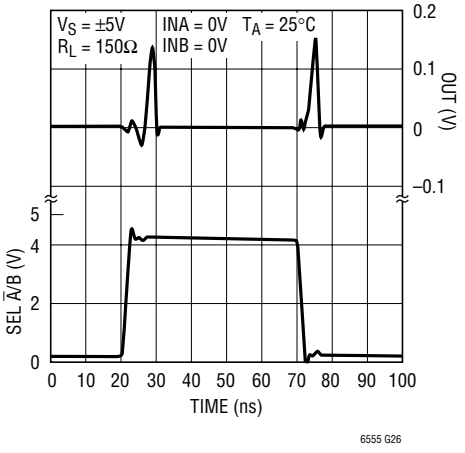
Gain Error Distribution



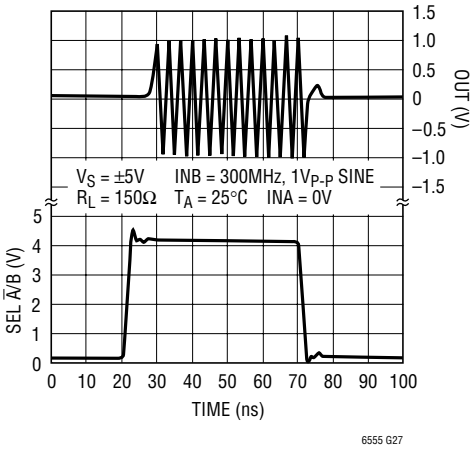
Gain Matching Distribution



Channel Switching Transient



Channel Switching Transient



PIN FUNCTIONS (GN24 Package)

IN1A (Pin 1): Channel 1 Input A. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

DGND (Pin 2): Digital Ground Reference for Enable Pin. This pin is normally connected to ground.

IN2A (Pin 3): Channel 2 Input A. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

V_{REF} (Pin 4): Voltage Reference for Input Clamping. This is the tap to an internal voltage divider that defines mid-supply. It is normally connected to ground in dual supply, DC coupled applications.

IN3A (Pin 5): Channel 3 Input A. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

AGND1 (Pin 6): Analog Ground for the 360Ω Gain Resistor of Channel 1.

IN1B (Pin 7): Channel 1 Input B. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

AGND2 (Pin 8): Analog Ground for the 360Ω Gain Resistor of Channel 2.

IN2B (Pin 9): Channel 2 Input B. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

AGND3 (Pin 10): Analog Ground for the 360Ω Gain Resistor of Channel 3.

IN3B (Pin 11): Channel 3 Input B. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

V^- (Pin 12): Negative Supply Voltage. V^- pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V^+ (Pins 13, 14, 24): Positive Supply Voltage. V^+ pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V^- (Pin 15): Negative Supply Voltage for Channel 3 Output Stage. V^- pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUT3 (Pin 16): Channel 3 Output. It is twice the selected channel 3 input and performs optimally with a 150Ω load (a double terminated 75Ω cable).

V^+ (Pin 17): Positive Supply Voltage for Channels 2 and 3 Output Stages. V^+ pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUT2 (Pin 18): Channel 2 Output. It is twice the selected channel 2 input and performs optimally with a 150Ω load (a double terminated 75Ω cable).

V^- (Pin 19): Negative Supply Voltage for Channels 1 and 2 Output Stages. V^- pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUT1 (Pin 20): Channel 1 Output. It is twice the selected channel 1 input and performs optimally with a 150Ω load (a double terminated 75Ω cable).

V^+ (Pin 21): Positive Supply Voltage for Channel 1 Output Stage. V^+ pins are not internally connected to each other and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

SEL (Pin 22): Select Pin. This high impedance pin selects which set of inputs are sent to the output pins. When the pin is pulled low, the A inputs are selected. When the pin is pulled high, the B inputs are selected.

$\overline{EN}$ (Pin 23): Enable Control Pin. An internal pull-up resistor of 46k defines the pin's impedance and will turn the part off if the pin is unconnected. When the pin is pulled low, the amplifiers are enabled.

Exposed Pad (Pin 25, QFN Only): The Exposed Pad is V^- and must be soldered to the PCB. It is internally connected to the QFN Pin 4, V^-.

APPLICATIONS INFORMATION

Power Supplies

The LT6555 is optimized for ±5V supplies but can be operated on as little as ±2.25V or a single 4.5V supply and as much as ±6V or a single 12V supply. Internally, each supply is independent to improve channel isolation. **Do not leave any supply pins disconnected or the part may not function correctly!**

Enable/Shutdown

The LT6555 has a shutdown mode controlled by the $\overline{EN}$ pin and referenced to the DGND pin. If the amplifier will be enabled at all times, the $\overline{EN}$ pin can be connected directly to DGND. If the enable function is desired, either driving the pin above 2V or allowing the internal 46k pull-up resistor to pull the $\overline{EN}$ pin to the top rail will disable the amplifier. When disabled, the DC output impedance will rise to approximately 360Ω through the internal feedback and gain resistors. Supply current into the amplifier in the disabled state will be:

$$I_S = \frac{V^+ - V_{\overline{EN}}}{46k} + \frac{V^+ - V^-}{80k}$$

It is important that the following constraints on the DGND, $\overline{EN}$ and SEL pins are always followed:

$$\mathbf{V^+ - V_{DGND} \geq 4.5V}$$
$$\mathbf{V_{EN} - V_{DGND} \leq 5.5V}$$
$$\mathbf{V_{SEL} - V_{DGND} \leq 8V}$$

In dual supply cases where V^+ is less than 4.5V, DGND should be connected to a potential below ground, such as V^-. Since the EN and SEL pins are referenced to DGND, they may need to be pulled below ground in those cases.

In single supply applications above 5.5V, an additional resistor may be needed from the EN pin to DGND if the pin is ever allowed to float. For example, on a 12V single supply, a 33k resistor would protect the pin from floating too high while still allowing the internal pull-up resistor to disable the part.

On dual ±2.25V supplies, connecting the DGND pin to V^- is the only way of ensuring that $V^+ - V_{DGND} \geq 4.5V$.

The DGND pin should not be pulled above the $\overline{EN}$ pin since doing so will turn on an ESD protection diode. If the $\overline{EN}$ pin voltage is forced a diode drop below the DGND pin, current should be limited to 10mA or less.

The enable/disable times of the LT6555 are fast when driven with a logic input. Turn on (from 50% $\overline{EN}$ input to 50% output) typically occurs in less than 50ns. Turn off is slower, but is typically below 500ns.

Channel Select

The SEL pin uses the same internal threshold as the $\overline{EN}$ pin and is also referenced to DGND. When the pin is logic low, the channel A inputs are passed to the output. When the pin is logic high, the channel B inputs are passed to the output. The pin should not be floated but can be tied to DGND to force the outputs to always be channel A or to V^+ (when less than 8V) to force the outputs to always be channel B.

Truth Table

SEL $\overline{A}$/B	$\overline{EN}$	OUT
0	0	2 × IN A
1	0	2 × IN B
X	1	OFF

Input Considerations

The LT6555 uses input clamps referenced to the V_{REF} pin to prevent damage to the input stage on the unselected channel. Three transistors in series limit the input voltage to within three diode drops (±) from V_{REF}. V_{REF} is nominally set to half of the sum of the supplies by the 40k resistors. A simplified schematic is shown in Figure 1.

To improve clamping, the pin's DC impedance should be minimized by connecting the V_{REF} pin directly to ground in the symmetric dual supply case with a common mode voltage of 0V. While loaded output swing limits the useful input voltage range in that case, if the common mode voltage is not centered at ground or the input voltage exceeds plus or minus three diodes from ground, an external resistor to either supply can be added to shift the

APPLICATIONS INFORMATION

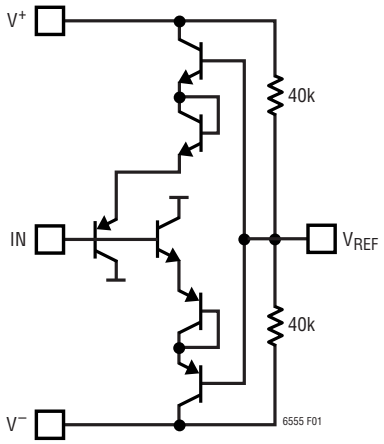


Figure 1. Simplified Schematic of V_{REF} Pin and Input Clamping

V_{REF} voltage to the desired level. The only way to cover the full common mode voltage range of V^- + 1V to V^+ – 1V is to shift V_{REF} up or down. Note that on a single supply, the unclamped input range limits the output low swing to 2V (1V multiplied by the internal gain of 2).

The V_{REF} pin can also be directly driven with a DC source. Bypassing the V_{REF} pin is not necessary.

The inputs can be driven beyond the point at which the output clips so long as input currents are limited to less than ±10mA. Continuing to drive the input beyond the output limit can result in increased current drive and slightly increased swing, but will also increase supply current and may result in delays in transient response at larger levels of overdrive.

Layout and Grounding

It is imperative that care is taken in PCB layout in order to benefit from the very high speed and very low crosstalk of the LT6555. Separate power and ground planes are highly recommended and trace lengths should be kept as short as possible. If input or output traces must be run over a distance of several centimeters, they should use a controlled impedance with matching series and shunt resistances (nominally 75Ω) to maintain signal fidelity.

Series termination resistors should be placed as close to the output pins as possible to minimize output capacitance. See the Typical Performance Characteristics section for a plot of frequency response with various output capacitors—only 10pF of parasitic output capacitance before the series termination resistor causes 6dB of peaking in the frequency response!

Low ESL/ESR bypass capacitors should be placed as close to the positive and negative supply pins as possible. One 4700pF ceramic capacitor is recommended for both V^+ and V^- supply busses. Additional 470pF ceramic capacitors with minimal trace length on each supply pin will further improve AC and transient response as well as channel isolation. For high current drive and large-signal transient applications, additional 1µF to 10µF tantalums should be added on each supply. The smallest value capacitors should be placed closest to the package.

If the AGND pins are not connected to ground, they must be carefully bypassed to maintain minimal impedance over frequency. Although crosstalk will vary depending upon board layout, a recommended starting point for bypass capacitors would be 470pF as close as possible to each AGND pin with a single 4700pF capacitor in parallel.

APPLICATIONS INFORMATION

To maintain the LT6555's channel isolation, it is beneficial to shield parallel input and parallel output traces using a ground plane or power supply traces. Vias between topside and backside metal may be required to maintain a low inductance ground near the part where numerous traces converge. See Figures 6 and 7 for photos of an optimized layout.

Input Expansion

In applications with more than two inputs per channel, multiple LT6555s can be connected by several different methods. The simplest method is to connect the outputs after the 75Ω series termination, as shown in Figure 2. The compromise of this approach is that the internal gain setting resistors cause a 435Ω shunt across the 75Ω cable termination, resulting in increased gain error.

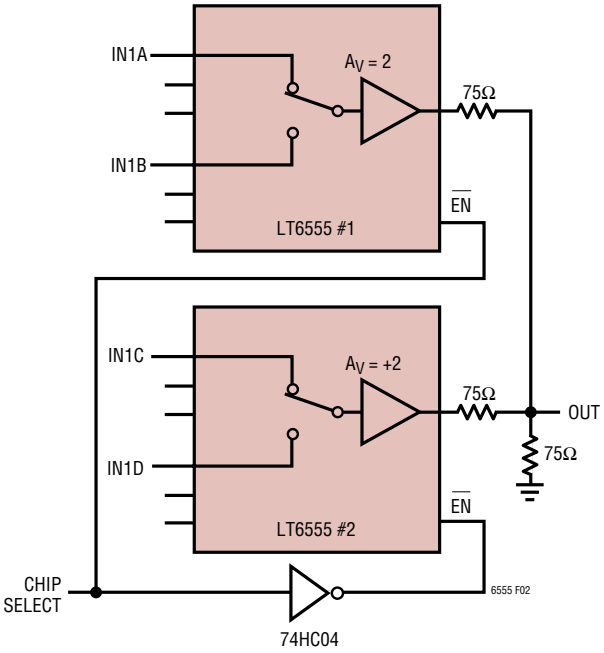


Figure 2. Two LT6555s Build a 4-Input Router

Figure 3 illustrates the loading effect of expanding the number of inputs. The resultant gain error can be calculated by the following formula using n as the number of LT6555s:

$$\text{Gain Error (dB)} = 6\text{dB} + 20\log\left(\frac{\frac{435\Omega}{n-1}\|75\Omega}{75+\frac{435\Omega}{n-1}\|75\Omega}\right)\text{dB}$$

For example, two LT6555s would result in a gain error of –0.74dB per channel. Three LT6555s (i.e., six red inputs, six green inputs and six blue inputs), would have a gain error of –1.4dB.

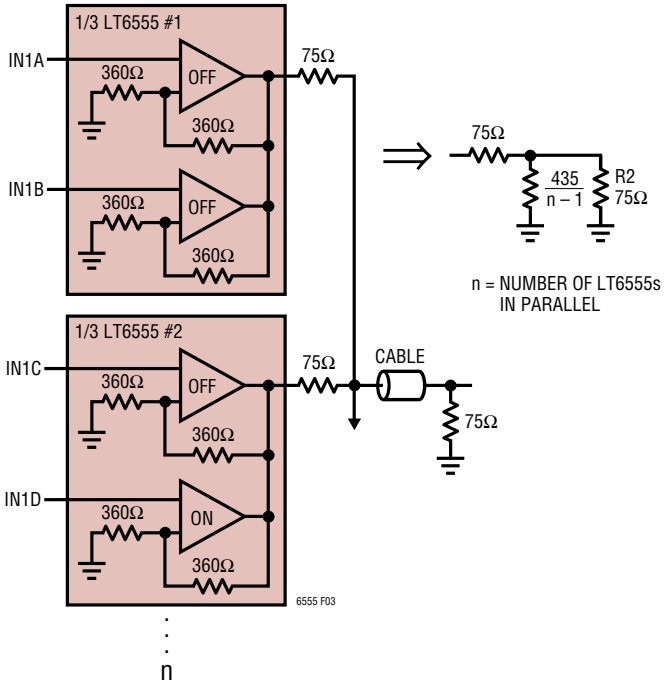


Figure 3. Disabled Amplifiers Load the Cable Termination with 435Ω Each

APPLICATIONS INFORMATION

This systematic gain error can be significantly reduced by lowering the value of the 75Ω series termination resistors. The compromise of this approach is an increased dependence on the accuracy of the 75Ω shunt termination at the receiving end of the line. A table of values for 1% series termination resistors from n = 2 to n = 4 is shown below.

NUMBER OF DEVICES (n)	SERIES R_T
2	63.9
3	56.2
4	49.9

Another approach that does not compromise gain accuracy is to connect the outputs directly together before the series termination. In this case, there will be slightly increased output glitching and supply current spiking during the EN pin switching, but the additional output loading will not increase the gain error, and the series termination resistors remain at their ideal value for AC response. See Figure 4 for a scope photo showing the result of the outputs connected both before and after the series terminations, and Figure 8 for a full schematic of a 4:1 RGB multiplexer with the output pins directly connected together. It is imperative that the output traces be as short as possible before the series termination in order to reduce capacitance and minimize AC peaking.

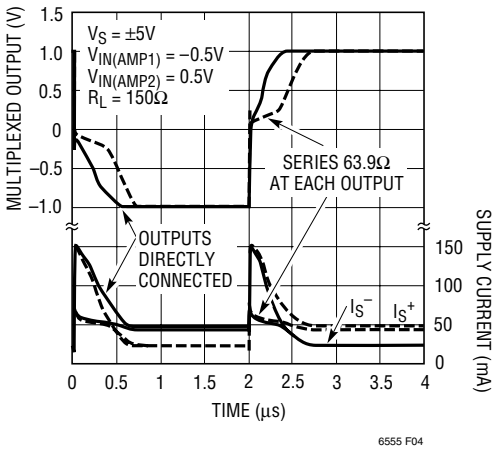


Figure 4. 4-Input Router Switching with Outputs Directly Connected and with Outputs Connected After 63.9Ω Series Termination

ESD Protection

The LT6555 has reverse-biased ESD protection diodes on all pins. If any pins are forced a diode drop above the positive supply or a diode drop below the negative supply, large currents may flow through these diodes. If the current is kept below 10mA, no damage to the devices will occur.

TYPICAL APPLICATION

RGB Multiplexer Demo Board

The DC858A Demo Board illustrates optimal routing, bypassing and termination using the LT6555 as an RGB video multiplexer. The schematic is shown in Figure 5. All inputs and outputs are routed to have a characteristic impedance of 75Ω and 75Ω input shunt and output series terminations are connected as close to the part as possible. The board is fabricated with four layers with internal ground and power planes. For ideal operation, a 75Ω load termination should be connected at the output. The LT6555's gain of 2 will compensate for the resulting divider between the series and load termination resistors. Figures 6 and 7 show the topside and bottom side board layout and placement.

TYPICAL APPLICATION

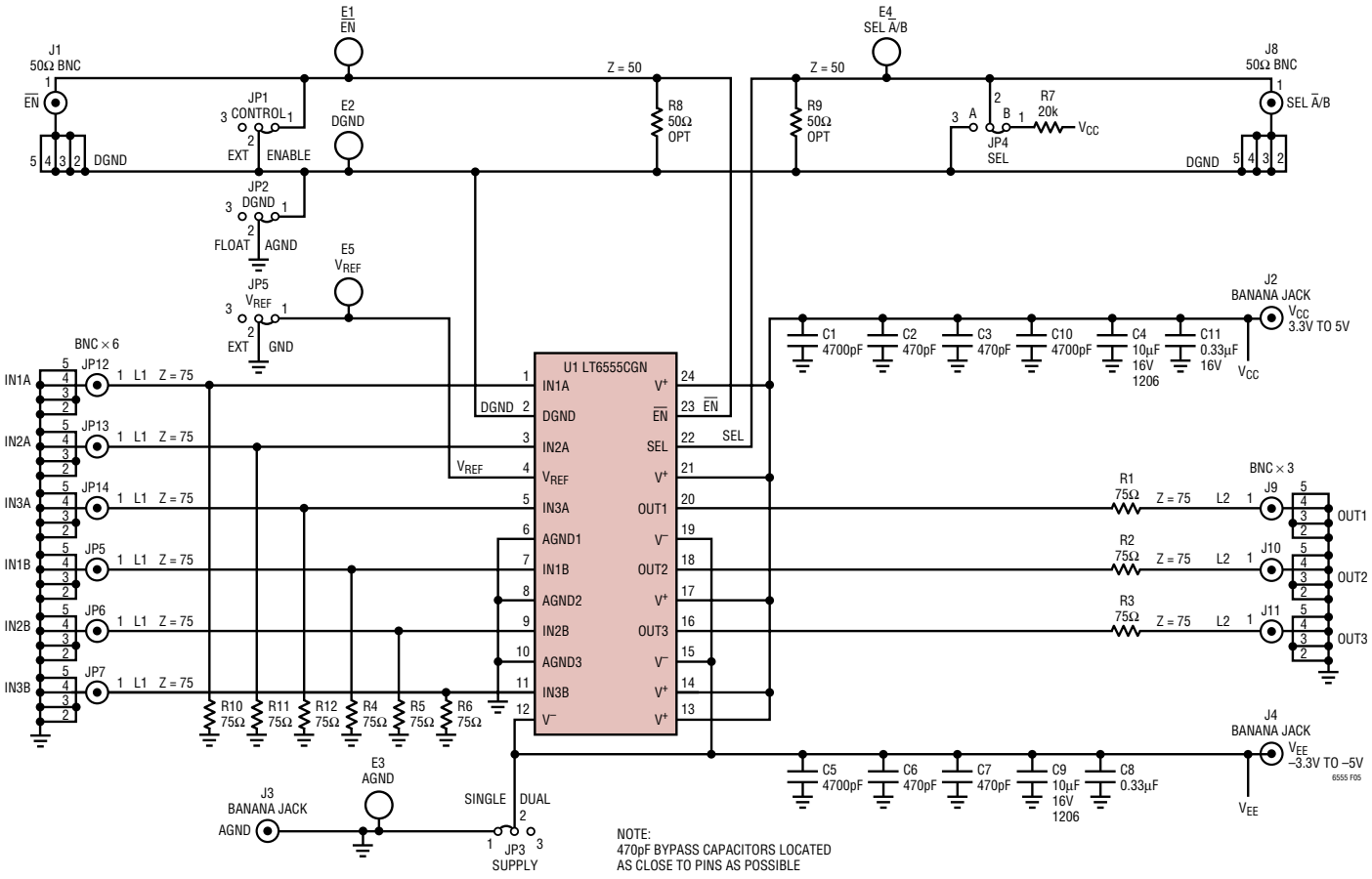


Figure 5. Demo Board Schematic

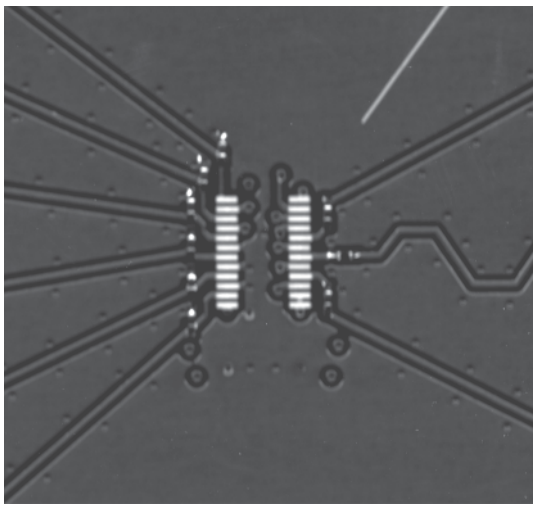


Figure 6. Demo Board Topside (IC Removed for Clarity)

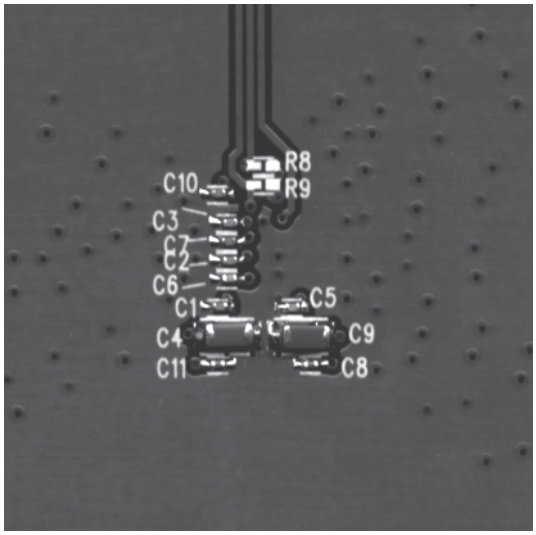
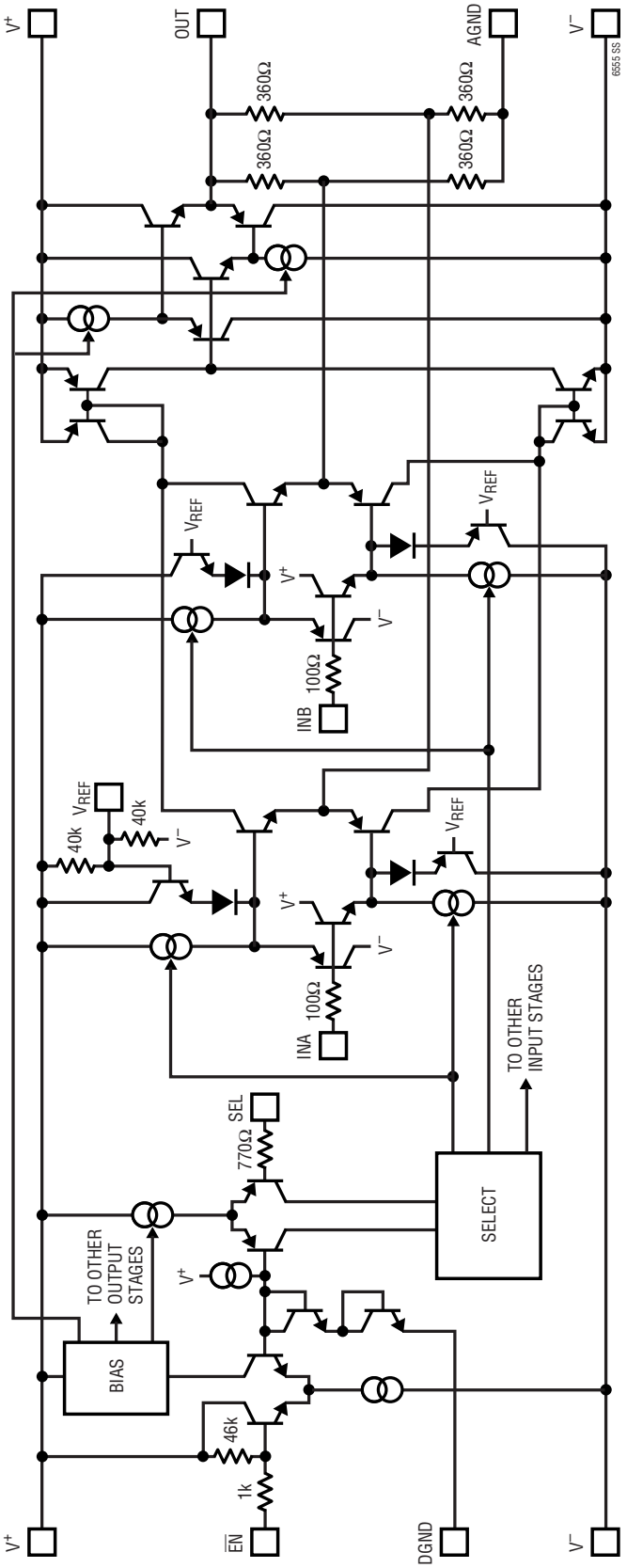


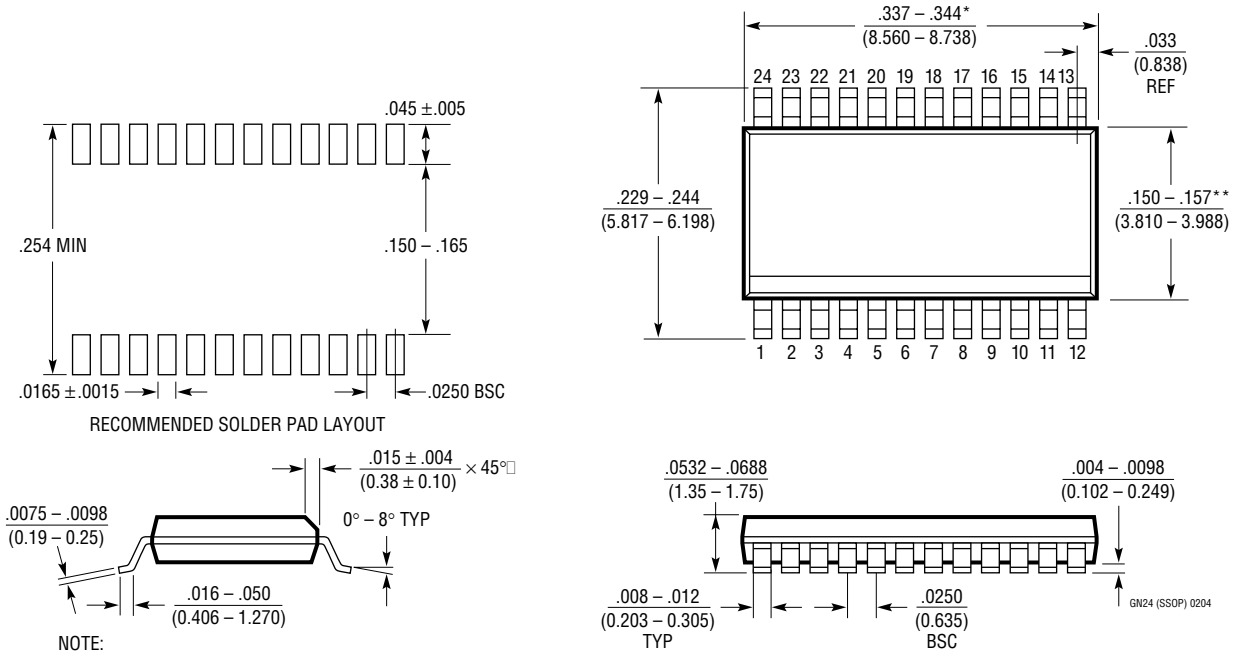
Figure 7. Demo Board Bottom Side

SIMPLIFIED SCHEMATIC (One channel shown)



PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



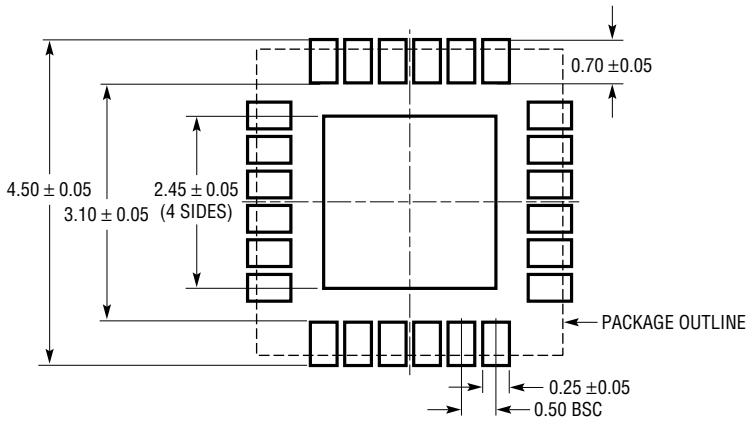
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

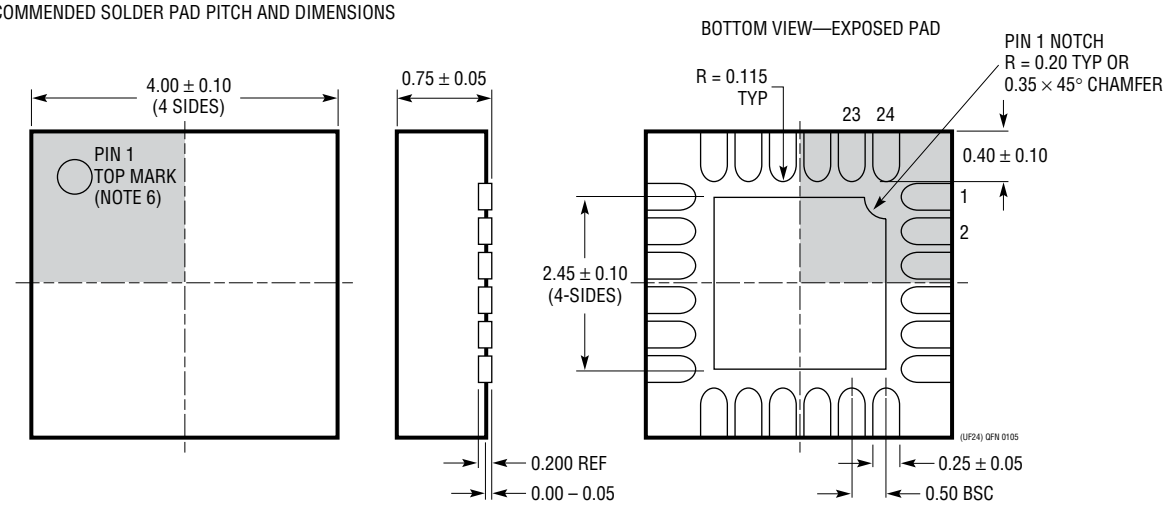
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

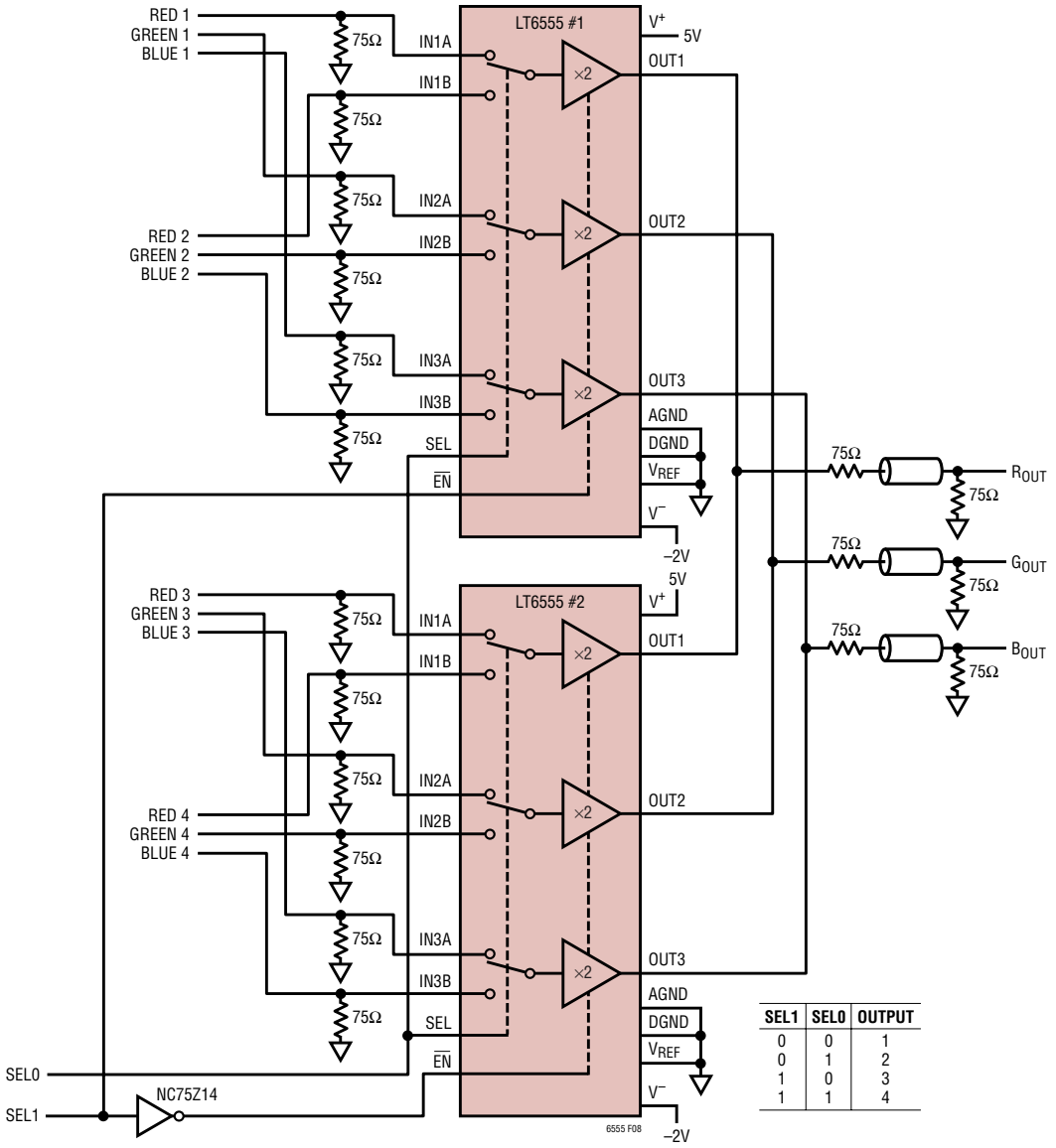


Figure 8. 4:1 RGB Multiplexer

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1203	150MHz Single 2:1 Multiplexer	Single SPDT Video Switch
LT1399	300MHz Triple Current Feedback Amplifier	0.1dB Gain Flatness to 150MHz, Shutdown
LT1675	250MHz Triple RGB Multiplexer	100MHz Pixel Switching, 1100V/µs Slew Rate, 16-Lead SSOP
LT6550/LT6551	3.3V Triple and Quad Video Buffers	110MHz Gain of 2 Buffers in MS Package
LT6553	650MHz Gain of 2 Triple Video Amplifier	Performance Similar to the LT6555 with One Set of Inputs, 16-Lead SSOP
LT6554	650MHz Gain of 1 Triple Video Amplifier	Same Pinout as the LT6553 but Optimized for High Impedance Loads

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