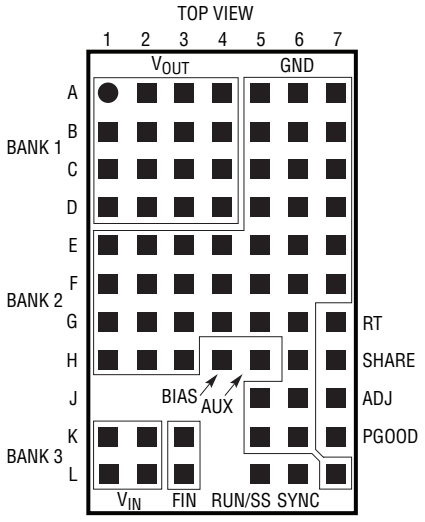
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, FIN, RUN/SS Voltage.....40V
ADJ, RT, SHARE Voltage.....5V
V_{OUT}, AUX.....10V
Current from AUX 100mA
PGOOD, SYNC 30V
BIAS.....25V
V_{IN} + BIAS.....56V
Maximum Junction Temperature (Note 2)..... 125°C
Solder Temperature (Note 3)..... 245°C

PIN CONFIGURATION



LGA PACKAGE
71-LEAD (9mm × 15mm × 2.82mm)

T_{JMAX} = 125°C, θ_{JA} = 20.7°C/W, $\theta_{JC(BOTTOM)}$ = 8.4°C/W,
$\theta_{JC(TOP)}$ = 25.6°C/W, θ_{JBOARD} = 13.8°C/W
θ VALUES DETERMINED PER JESD 51-9
WEIGHT = 1.2g

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM8031EV#PBF	LTM8031EV#PBF	LTM8031V	71-Lead (9mm × 15mm × 2.82mm) LGA	–40°C to 125°C
LTM8031IV#PBF	LTM8031IV#PBF	LTM8031V	71-Lead (9mm × 15mm × 2.82mm) LGA	–40°C to 125°C
LTM8031MPV#PBF	LTM8031MPV#PBF	LTM8031V	71-Lead (9mm × 15mm × 2.82mm) LGA	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, $V_{RUN/SS}$ = 10V, V_{BIAS} = 3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	3.6		36	V
V_{OUT}	Output DC Voltage	0.2A < I_{OUT} ≤ 1A, R_{ADJ} Open 0.2A < I_{OUT} ≤ 1A, R_{ADJ} = 21.6k			0.8 10		V V
I_{OUT}	Continuous Output DC Current	V_{IN} = 24V				1	A
$I_{Q(VIN)}$	V_{IN} Quiescent Current	$V_{RUN/SS}$ = 0.2V V_{BIAS} = 3V, Not Switching V_{BIAS} = 0V, Not Switching	 ● 		0.6 25 88	 60 120	µA µA µA
$I_{Q(BIAS)}$	BIAS Quiescent Current	$V_{RUN/SS}$ = 0.2V V_{BIAS} = 3V, Not Switching V_{BIAS} = 0V, Not Switching	 ● 		0.03 60 1	 120 5	µA µA µA
$\frac{\Delta V_{OUT}}{V_{OUT}}$	Line Regulation	10V ≤ V_{IN} ≤ 36V, I_{OUT} = 1A, V_{OUT} = 3.3V			0.1		%
	Load Regulation	V_{IN} = 24V, 0.2A ≤ I_{OUT} ≤ 1A, V_{OUT} = 3.3V			0.3		%
$V_{OUT(AC\_RMS)}$	Output Ripple (RMS)	V_{IN} = 24V, I_{OUT} = 1A, V_{OUT} = 3.3V			6		mV
f_{SW}	Switching Frequency	R_T = 113k			325		kHz
V_{ADJ}	Voltage at ADJ Pin		●	765	790	815	mV
$V_{BIAS(MIN)}$	Minimum BIAS Voltage for Proper Operation				1.9	2.8	V
I_{ADJ}	Current Out of ADJ Pin	$V_{RUN/SS}$ = 0V, V_{ADJ} = 0V, V_{OUT} = 1V			4		µA
$I_{RUN/SS}$	RUN/SS Pin Current	$V_{RUN/SS}$ = 2.5V			5	10	µA
$V_{IH(RUN/SS)}$	RUN/SS Input High Voltage			2.5			V
$V_{IL(RUN/SS)}$	RUN/SS Input Low Voltage					0.2	V
$V_{PG(TH)}$	ADJ Voltage Threshold for PGOOD to Switch				730		mV
I_{PGO}	PGOOD Leakage	V_{PG} = 30V			0.1	1	µA
I_{PGSINK}	PGOOD Sink Current	V_{PG} = 0.4V		200	800		µA
V_{SYNCIL}	SYNC Input Low Threshold	f_{SYNC} = 550kHz				0.5	V
V_{SYNCIH}	SYNC Input High Threshold	f_{SYNC} = 550kHz		0.7			V
$I_{SYNC(BIAS)}$	SYNC Pin Bias Current	V_{SYNC} = 0V, V_{BIAS} = 0V			0.1		µA
$V_{IN(RIPPLE)}$	550kHz Narrowband Conducted Emission 1MHz Narrowband Conducted Emission 3MHz Narrowband Conducted Emission	V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1A, f_{SW} = 550kHz, 5µH LISN			83 63 51		dBµV dBµV dBµV

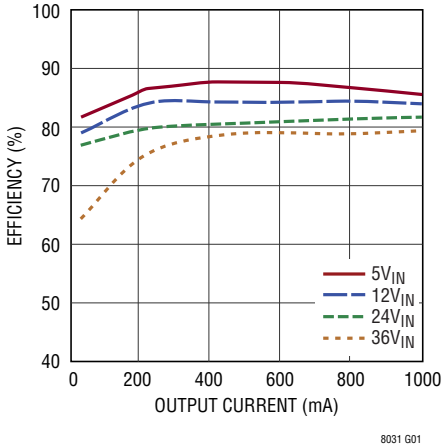
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM8031E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the –40°C to 125°C internal temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8031I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8031MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

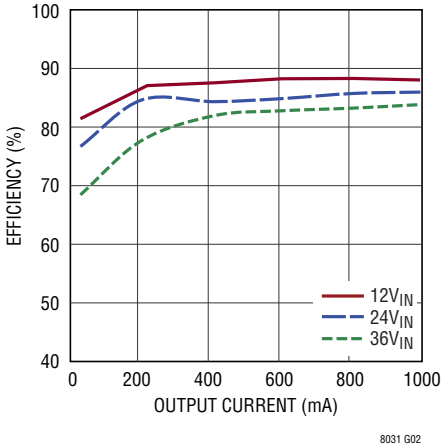
Note 3: See Linear Technology Application Note 100.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

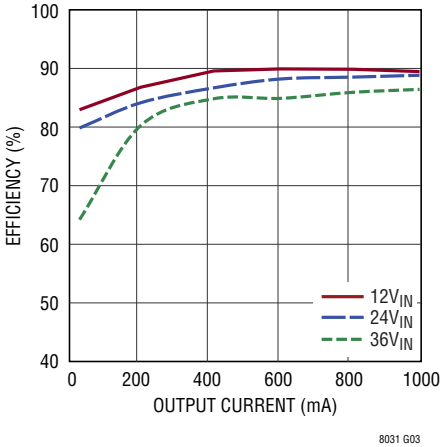
3.3V_{OUT} Efficiency



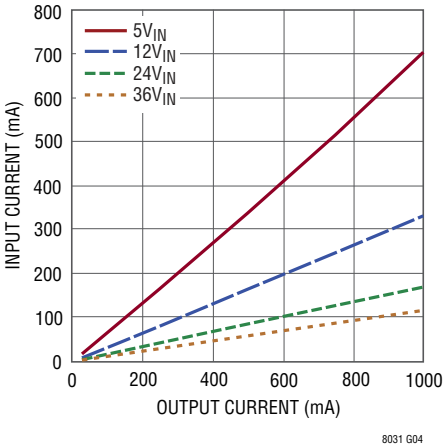
5V_{OUT} Efficiency



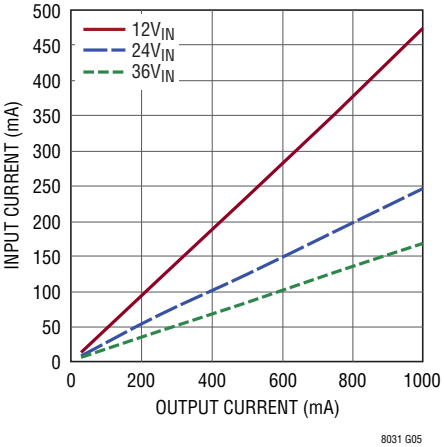
8V_{OUT} Efficiency



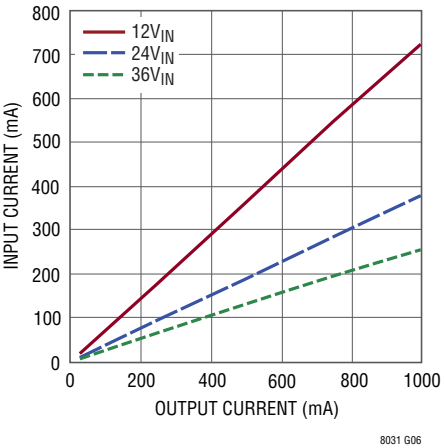
Input Current vs Output Current, 3.3V_{OUT}



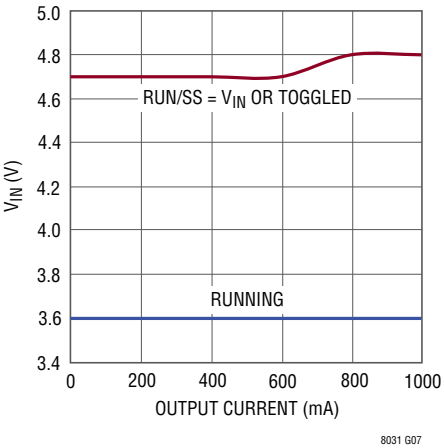
Input Current vs Output Current, 5V_{OUT}



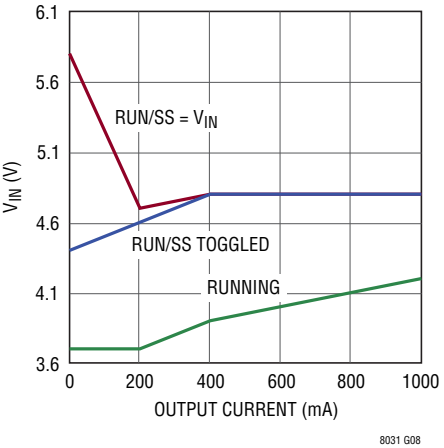
Input Current vs Output Current, 8V_{OUT}



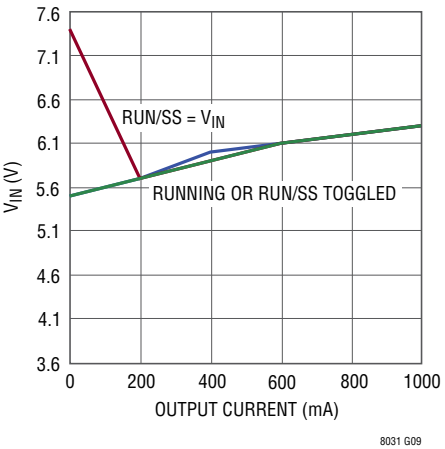
Minimum V_{IN} vs Output Current 2.5V V_{OUT}



Minimum V_{IN} vs Output Current 3.3V V_{OUT}

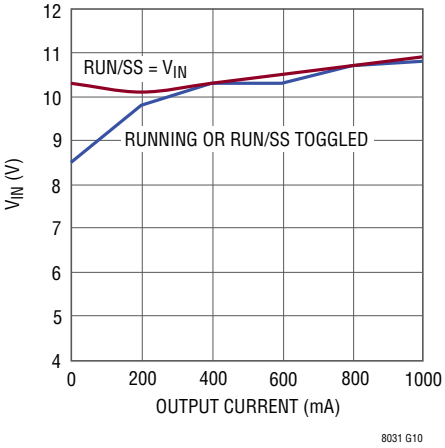


Minimum V_{IN} vs Output Current 5V V_{OUT}

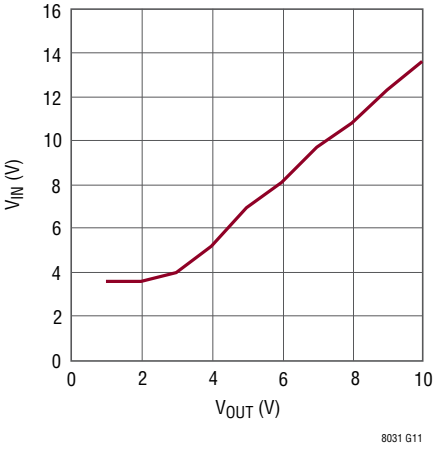


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

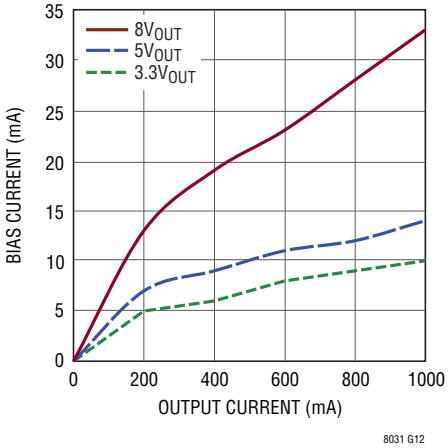
Minimum V_{IN} vs Output Current 8V V_{OUT}



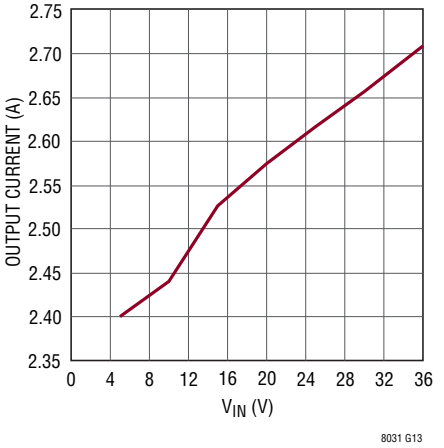
Minimum Input Running Voltage vs Output Voltage, I_{OUT} = 1A



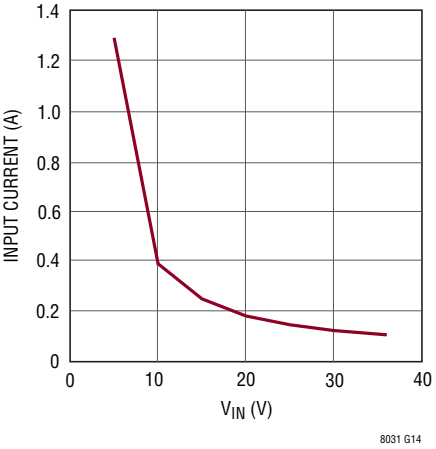
Bias Current vs Output Current



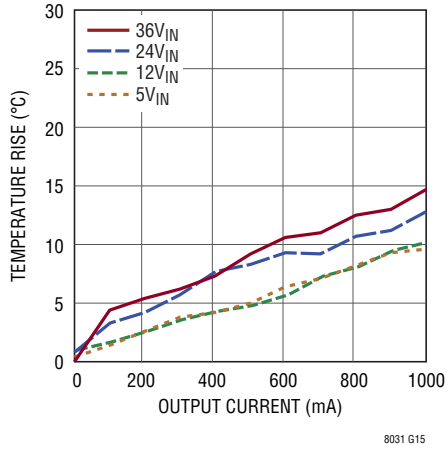
Output Current vs Input Voltage (Output Shorted)



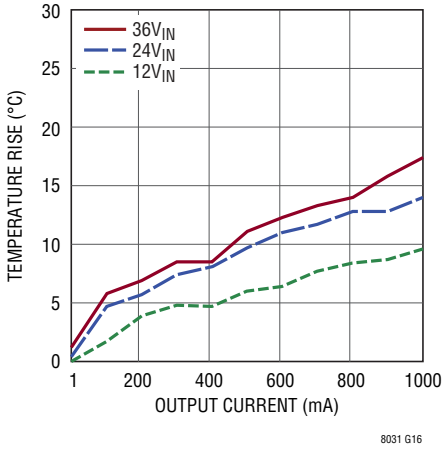
Input Current vs Input Voltage (Output Shorted)



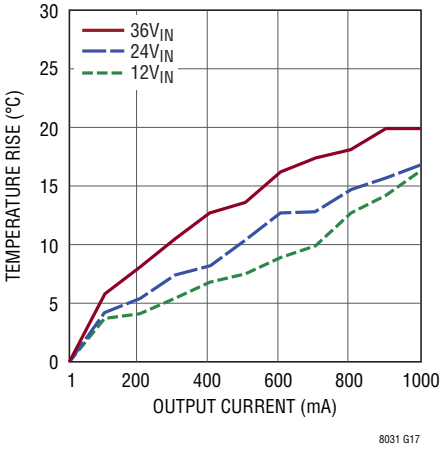
Temperature Rise vs Load Current, V_{OUT} = 3.3V



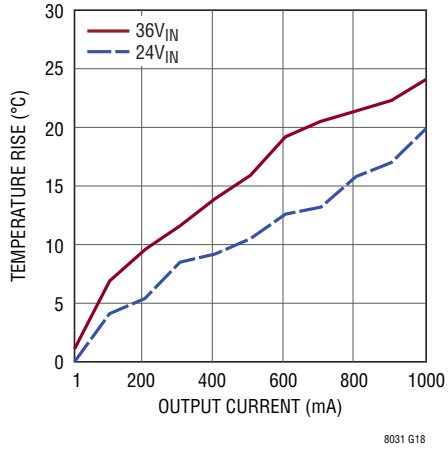
Temperature Rise vs Load Current, V_{OUT} = 5V



Temperature Rise vs Load Current, V_{OUT} = 8V

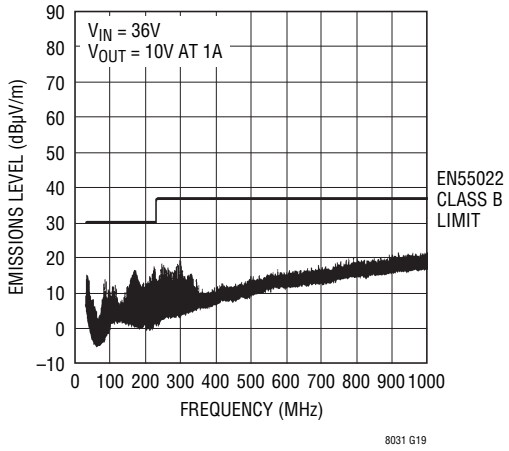


Temperature Rise vs Load Current, V_{OUT} = 10V

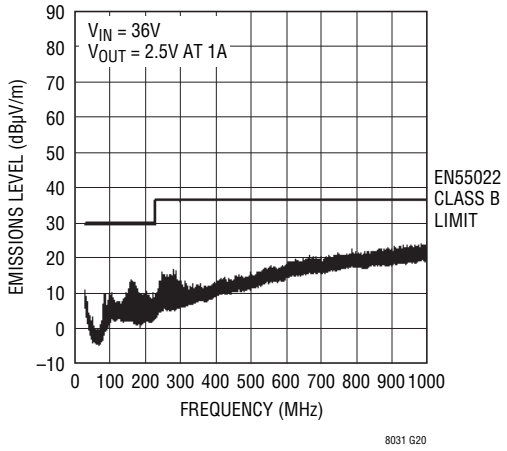


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Radiated Emissions



Radiated Emissions



PIN FUNCTIONS

V_{IN} (Bank 3): The V_{IN} pin supplies current to the LTM8031's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor of at least 1µF.

FIN (K3, L3): Filtered Input. This is the node after the input EMI filter. Use this only if there is a need to modify the behavior of the integrated EMI filter or if V_{IN} rises or falls rapidly; otherwise, leave these pins unconnected. See the Applications Information section for more details.

GND (Bank 2): Tie these GND pins to a local ground plane below the LTM8031 and the circuit components. Return the feedback divider (R_{ADJ}) to this net.

V_{OUT} (Bank 1): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

AUX (Pin H5): Low Current Voltage Source for BIAS. In many designs, the BIAS pin is simply connected to V_{OUT}. The AUX pin is internally connected to V_{OUT} and is placed adjacent to the BIAS pin to ease printed circuit board routing. Although this pin is internally connected to V_{OUT}, **do not** connect this pin to the load. If this pin is not tied to BIAS, leave it floating.

BIAS (Pin H4): The BIAS pin connects to the internal power bus. Connect to a power source greater than 2.8V. If the output is greater than 2.8V, connect this pin to AUX. If the output voltage is less, connect this to a voltage source between 2.8V and 25V. Also, make sure that BIAS + V_{IN} is less than 56V.

RUN/SS (Pin L5): Pull RUN/SS pin to less than 0.2V to shut down the LTM8031. Tie to 2.5V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin. RUN/SS also provides a soft-start function; see the Applications Information section.

RT (Pin G7): The RT pin is used to program the switching frequency of the LTM8031 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin.

SHARE (Pin H7): Tie this to the SHARE pin of another LTM8031 when paralleling the outputs.

PIN FUNCTIONS

SYNC (Pin L6): This is the external clock synchronization input. Ground this pin for low ripple Burst Mode® operation at low output loads. Tie to a stable voltage source greater than 0.7V to disable Burst Mode operation. Do not leave this pin floating. Tie to a clock source for synchronization. Clock edges should have rise and fall times faster than 1µs. See Synchronization section in Applications Information.

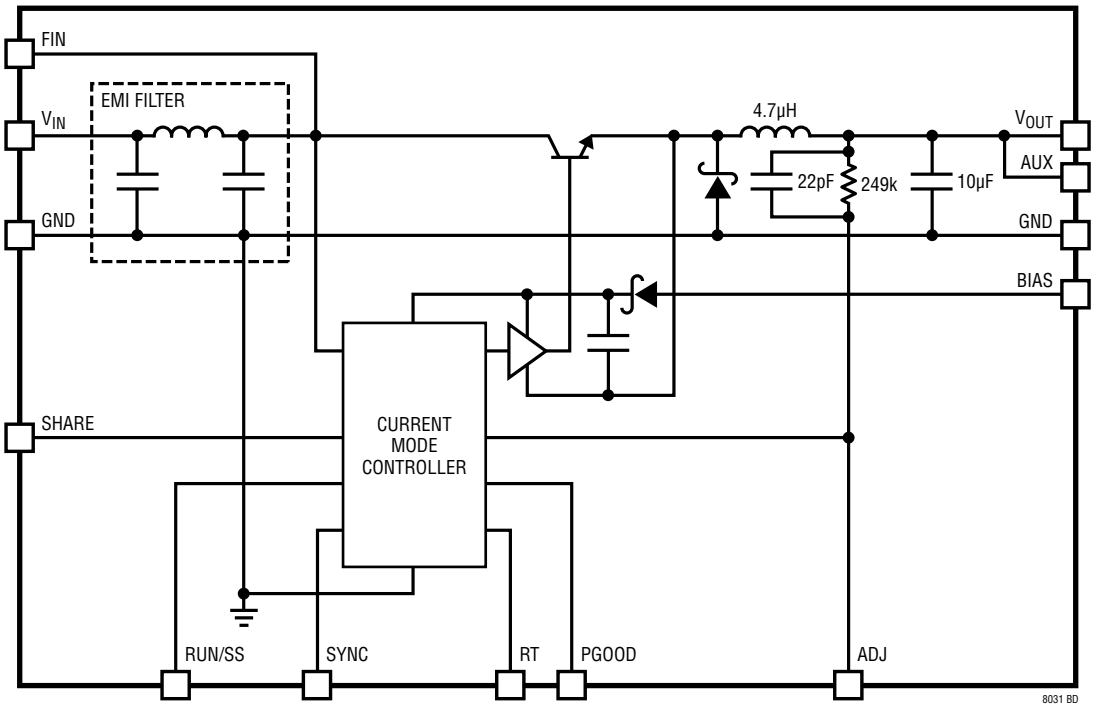
PGOOD (Pin K7): The PGOOD pin is the open-collector output of an internal comparator. PGOOD remains low until the ADJ pin is within 10% of the final regulation voltage. The PGOOD output is valid when V_{IN} is above 3.6V and RUN/SS is high. If this function is not used, leave this pin floating.

ADJ (Pin J7): The LTM8031 regulates its ADJ pin to 0.79V. Connect the adjust resistor from this pin to ground. The value of R_{ADJ} is given by the equation:

$$R_{ADJ} = \frac{196.71}{V_{OUT} - 0.79}$$

where R_{ADJ} is in kΩ.

BLOCK DIAGRAM



OPERATION

The LTM8031 is a standalone nonisolated step-down switching DC/DC power supply. It can deliver up to 1A of DC output current with only bulk external input and output capacitors. This module provides a precisely regulated output voltage programmable via one external resistor from 0.8VDC to 10VDC. The input voltage range is 3.6V to 36V. Given that the LTM8031 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. A simplified Block Diagram is given on the previous page.

The LTM8031 is designed with an input EMI filter and other features to make its radiated emissions compliant with several EMC specifications including EN55022 class B. Compliance with conducted emissions requirements may be obtained by adding a standard input filter.

The LTM8031 contains a current mode controller, power switching element, power inductor, power Schottky diode and a modest amount of input and output capacitance. The LTM8031 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

An internal regulator provides power to the control circuitry. The bias regulator can draw power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 2.8V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LTM8031 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

To further optimize efficiency, the LTM8031 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 50µA in a typical application. The oscillator reduces the LTM8031's operating frequency when the voltage at the ADJ pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LTM8031 contains a power good comparator which trips when the ADJ pin is at 90% of its regulated value. The PGOOD output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PGOOD pin high. Power good is valid when the LTM8031 is enabled and V_{IN} is above 3.6V.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{ADJ} and R_T values.
3. Connect BIAS as indicated.

As the integrated input EMI filter may ring in response to an application of a step input voltage, a bulk capacitance, series resistance or some clamping mechanism may be required. See the Hot-Plugging Safely section for details.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they

APPLICATIONS INFORMATION

Table 1. Recommended Component Values and Configuration (See Typical Performance Characteristics for Load Conditions)

V_{IN}	V_{OUT}	C_{IN}	C_{OUT}	R_{ADJ}	BIAS	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$	f_{MAX}	$R_{T(MIN)}$
3.6V to 36V	0.82V	1µF 0805 50V	2 × 100µF 1206 6.3V	5.11M	≥2.8V, <25V	250kHz	150k	250kHz	150k
3.6V to 36V	1.20V	1µF 0805 50V	100µF//47µF 1206 6.3V	475k	≥2.8V, <25V	300kHz	124k	325kHz	113k
3.6V to 36V	1.80V	1µF 0805 50V	100µF 1206	191k	≥2.8V, <25V	420kHz	84.5k	450kHz	78.7k
3.6V to 36V	2.00V	1µF 0805 50V	100µF 1206	162k	≥2.8V, <25V	450kHz	78.7k	475kHz	73.2k
3.6V to 36V	2.50V	1µF 0805 50V	47µF 0805 6.3V	115k	≥2.8V, <25V	550kHz	61.9k	575kHz	59.0k
4.75V to 36V	3.30V	1µF 0805 50V	22µF 1206 6.3V	78.7k	AUX	675kHz	48.7k	725kHz	44.2k
6.8V to 36V	5.00V	1µF 0805 50V	10µF 1206 6.3V	46.4k	AUX	975kHz	29.4k	1000kHz	28.0k
10.5V to 36V	8.00V	1µF 0805 50V	4.7µF 1206 10V	26.7k	AUX	1200kHz	23.7k	1600kHz	15.8k
13V to 36V	10.00V	1µF 0805 50V	4.7µF 0805 16V	21.0k	AUX	1250kHz	22.6k	2050kHz	10.5k
3.6V to 15V	0.82V	1µF 0805 50V	2 × 100µF 1206 6.3V	5.11M	V_{IN}	500kHz	69.8k	600kHz	56.2k
3.6V to 15V	1.20V	1µF 0805 50V	100µF 1206 6.3V	475k	V_{IN}	600kHz	56.2k	750kHz	42.2k
3.6V to 15V	1.80V	1µF 0805 50V	100µF 1206	191k	V_{IN}	650kHz	51.1k	1000kHz	28.0k
3.6V to 15V	2.00V	1µF 0805 50V	100µF 1206	162k	V_{IN}	650kHz	51.1k	1100kHz	26.7k
3.6V to 15V	2.50V	1µF 0805 50V	47µF 0805 6.3V	115k	V_{IN}	700kHz	47.5k	1350kHz	20.5k
4.75V to 15V	3.30V	1µF 0805 50V	22µF 1206 6.3V	78.7k	AUX	950kHz	32.4k	1650kHz	15.0k
6.8V to 15V	5.00V	1µF 0805 50V	10µF 1206 6.3V	46.4k	AUX	1150kHz	25.5k	2400kHz	7.87k
10.5V to 15V	8.00V	1µF 0805 50V	4.7µF 1206 10V	26.7k	AUX	1200kHz	23.7k	2400kHz	7.87k
9V to 24V	0.82V	1µF 0805 50V	2 × 100µF 1206 6.3V	5.11M	≥2.8V, <25V	350kHz	105k	375kHz	93.1k
9V to 24V	1.20V	1µF 0805 50V	100µF//47µF 1206 6.3V	475k	≥2.8V, <25V	450kHz	78.7k	475kHz	73.2k
9V to 24V	1.80V	1µF 0805 50V	100µF 1206	191k	≥2.8V, <25V	600kHz	56.2k	650kHz	51.1k
9V to 24V	2.00V	1µF 0805 50V	100µF 1206	162k	≥2.8V, <25V	650kHz	51.1k	700kHz	47.5k
9V to 24V	2.50V	1µF 0805 50V	47µF 0805 6.3V	115k	≥2.8V, <25V	700kHz	47.5k	850kHz	37.4k
9V to 24V	3.30V	1µF 0805 50V	22µF 1206 6.3V	78.7k	AUX	950kHz	32.4k	1050kHz	28.0k
9V to 24V	5.00V	1µF 0805 50V	10µF 1206 6.3V	46.4k	AUX	1150kHz	25.5k	1550kHz	16.5k
10.5V to 24V	8.00V	1µF 0805 50V	4.7µF 1206 10V	26.7k	AUX	1200kHz	23.7k	2400kHz	7.87k
13V to 24V	10.00V	1µF 0805 50V	4.7µF 0805 16V	21.0k	AUX	1250kHz	22.6k	2400kHz	7.87k

Note: An input bulk capacitor is required.

APPLICATIONS INFORMATION

may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected. Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8031's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8031 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. The input capacitor can be a parallel combination of a 1µF ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8031. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8031 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Electromagnetic Compliance

The LTM8031 is compliant with the radiated emissions requirements of EN55022 class B. Graphs of the LTM8031's EMC performance are given in the Typical Performance Characteristics section. Further data, operating conditions and test setup are detailed in an EMI Test report available from Linear Technology.

Frequency Selection

The LTM8031 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.4MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.2	187
0.3	124
0.4	88.7
0.5	69.8
0.6	56.2
0.7	47.5
0.8	39.2
0.9	34
1.0	28.0
1.2	23.7
1.4	19.1
1.5	16.2
1.8	13.3
2	11.5
2.2	9.76
2.4	8.66

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8031 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8031 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or unnecessarily large output capacitor. The maximum frequency (and attendant R_T value) at which the LTM8031 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

APPLICATIONS INFORMATION

BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate internal circuitry. For proper operation, it must be powered by at least 2.8V. If the output voltage is programmed to be 2.8V or higher, simply tie BIAS to AUX. If V_{OUT} is less than 2.8V, BIAS can be tied to V_{IN} or some other voltage source. In all cases, ensure that the maximum voltage at the BIAS pin is both less than 25V and the sum of V_{IN} and BIAS is less than 56V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the LTM8031.

Load Sharing

Two or more LTM8031s may be paralleled to produce higher currents. This may, however, alter the EMI performance of the LTM8031s. To do this, tie the V_{IN}, ADJ, V_{OUT} and SHARE pins of all the paralleled LTM8031s together. To ensure that paralleled modules start up together, the RUN/SS pins may be tied together, as well. Synchronize the LTM8031s to an external clock to eliminate beat frequencies, if required. If the RUN/SS pins are not tied together, make sure that the same valued soft-start capacitors are used for each module. An example of two LTM8031 modules configured for load sharing is given in the Typical Applications section. For 2A applications also see the LTM8032, 2A EMC DC/DC µModule regulator

Burst Mode Operation

To enhance efficiency at light loads, the LTM8031 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8031 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are reduced to typically 25µA and 60µA respectively during the sleep time. As the load current decreases towards a no-load condition, the percentage of time that the LTM8031 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher efficiency. Burst Mode operation is enabled by tying SYNC to GND. To disable Burst Mode operation, tie SYNC to a stable voltage above 0.7V. Do not leave the SYNC pin floating.

Minimum Input Voltage

The LTM8031 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. In addition, the input voltage required to turn on is higher than that required to run, and depends upon whether the RUN/SS is used. As shown in the Typical Performance Characteristics section, it takes only about $3.6V_{IN}$ for the LTM8031 to run a 3.3V output at light load. If RUN/SS is pulled up to V_{IN}, it takes $5.7V_{IN}$ to start. If the LTM8031 is enabled via the RUN/SS pin, the minimum voltage to start at light loads is lower, about 4.4V. Similar curves for $2.5V_{OUT}$, $5V_{OUT}$ and $8V_{OUT}$ operation are also provided in the Typical Performance Characteristics section.

Soft-Start

The RUN/SS pin can be used to soft-start the LTM8031, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC network to create a voltage ramp at this pin. Figure 1 shows the start-up and shutdown waveforms with the soft-start circuit. By choosing an appropriate RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply at least 20µA when the RUN/SS pin reaches 2.5V.

APPLICATIONS INFORMATION

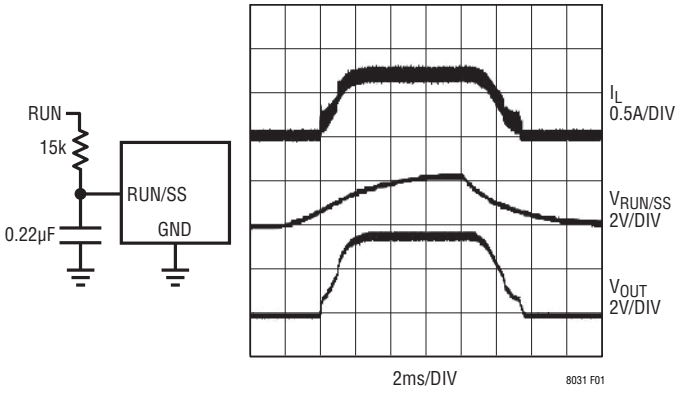


Figure 1. To Soft-Start the LTM8031, Add a Resistor and Capacitor to the RUN/SS Pin

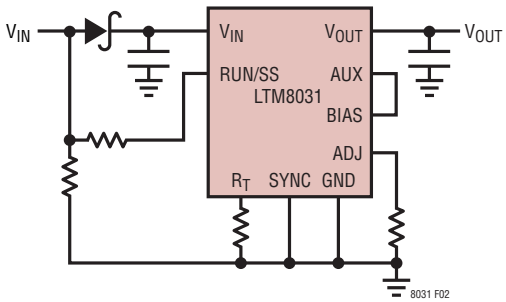


Figure 2. The Input Diode Prevents a Shorted Input from Discharging a Back-Up Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8031 Runs Only When the Input is Present

Synchronization

The internal oscillator of the LTM8031 can be synchronized by applying an external 250kHz to 2MHz clock to the SYNC pin. Do not leave this pin floating. The resistor tied from the RT pin to ground should be chosen such that the LTM8031 oscillates 20% lower than the intended synchronization frequency (see the Frequency Selection section). The LTM8031 will not enter Burst Mode operation while synchronized to an external clock, but will instead skip pulses to maintain regulation.

Shorted Input Protection

Care needs to be taken in systems where the output will be held high when the input to the LTM8031 is absent. This may occur in battery charging applications or in battery back-up systems where a battery or some other supply is diode ORed with the LTM8031's output. If the V_{IN} pin is allowed to float and the RUN/SS pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8031's internal circuitry will pull its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN/SS pin, the internal switch current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LTM8031 can pull large currents from the output through the V_{IN} pin, potentially damaging the device. Figure 2 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8031. The LTM8031 is nevertheless a switching power supply and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout.

Ensure that the grounding and heat sinking are acceptable. A few rules to keep in mind are:

1. Place the R_{ADJ} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8031. If a capacitor is connected to the FIN terminals, place it as close as possible to the FIN terminals, such that its ground connection is as close as possible to that of the C_{IN} capacitor.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8031.

APPLICATIONS INFORMATION

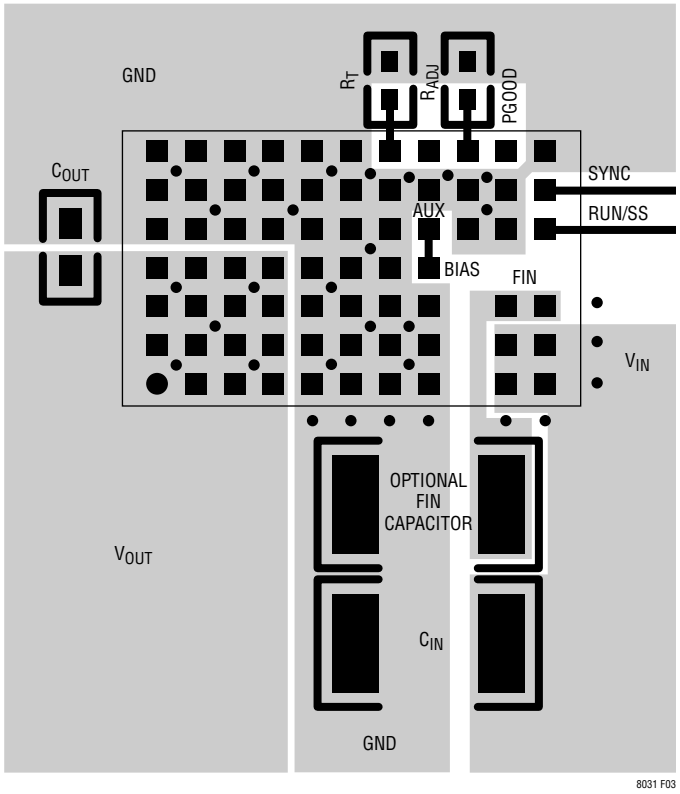


Figure 3. Layout Showing Suggested External Components, GND Plane and Thermal Vias

4. Place the C_{IN} and C_{OUT} capacitors such that their ground currents flow directly adjacent or underneath the LTM8031.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8031.
6. Use vias to connect the GND copper area to the board's internal ground plane. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8031. However, these capacitors can cause problems if the LTM8031 is plugged into a live or fast rising or falling supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an under-damped tank circuit, and the voltage at the V_{IN} pin of the LTM8031 can ring to twice the nominal input voltage, possibly exceeding the LTM8031's rating and damaging the part. A similar phenomenon can occur inside the LTM8031 module, at the output of the integrated EMI filter, with the same potential of damaging the part.

If the input supply is poorly controlled or the user will be plugging the LTM8031 into an energized supply, the input network should be designed to prevent this overshoot. Figure 4 shows the waveforms that result when an LTM8031 circuit is connected to a 24V supply through six feet of 24-gauge twisted pair. The first plot (4a) is the response with a 2.2µF ceramic capacitor at the input. The input voltage

APPLICATIONS INFORMATION

rings as high as 35V and the input current peaks at 20A. One method of damping the tank circuit is to add another capacitor with a series resistor to the circuit, as shown in Figure 4b. A 0.7Ω resistor is added in series with the input to eliminate the voltage overshoot (it also reduces the peak input current). A 0.1µF capacitor improves high frequency filtering. For high input voltages its impact on efficiency is minor, reducing efficiency less than one-half percent for a 5V output at full load operating from 24V. By far the most popular method of controlling overshoot is shown in Figure 4c, where an aluminum electrolytic capacitor has been connected to FIN. This capacitor's high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit. Placing the electrolytic capacitor at the FIN terminals can also improve the LTM8031's EMI filtering as well as guard against overshoots caused by the Q of the integrated filter.

Thermal Considerations

The LTM8031 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by a LTM8031 mounted to a 35cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The junction-to-air and junction-to-board thermal resistances given in the Pin Configuration diagram may also be used to estimate the LTM8031 internal temperature. These thermal coefficients are determined per JESD 51-9 (JEDEC standard, test boards for area array surface mount package thermal measurements) through analysis and physical correlation. Bear in mind that the actual thermal resistance of the LTM8031 to the printed circuit board depends upon the design of the circuit board. The die temperature of the LTM8031 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8031.

The bulk of the heat flow out of the LTM8031 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

Finally, be aware that at high ambient temperatures the internal Schottky diode will have significant leakage current increasing the quiescent current of the LTM8031.

TYPICAL APPLICATIONS

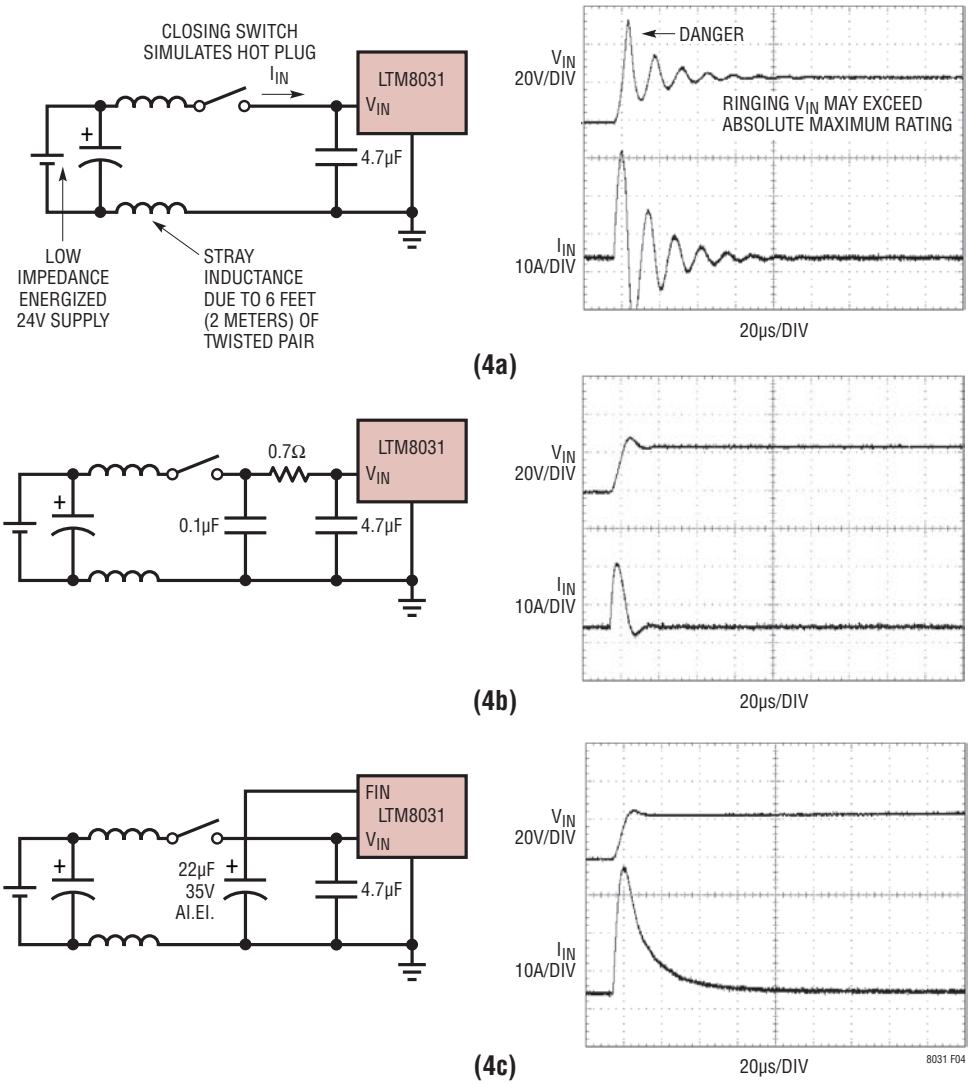
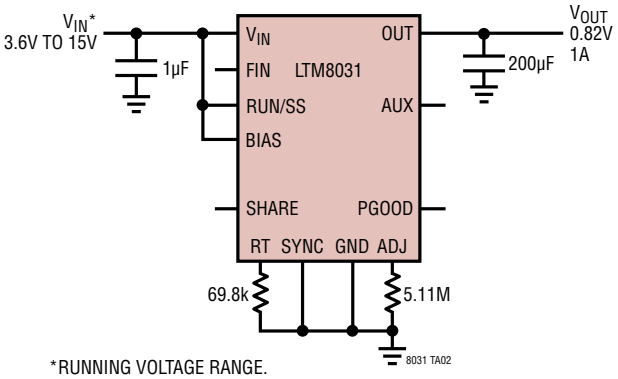


Figure 4. A Well Chosen Input Network Prevents Input Voltage Overshoot and Ensures Reliable Operation When the LTM8031 is Hot-Plugged to a Live Supply

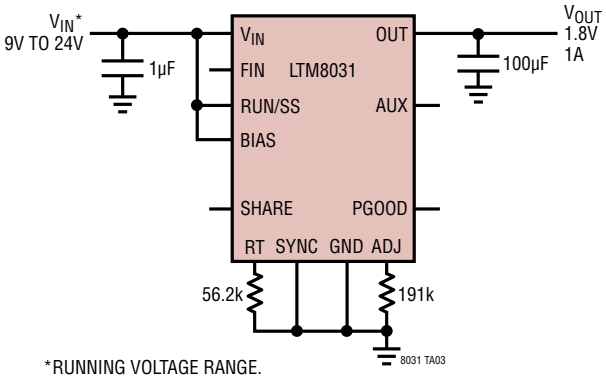
TYPICAL APPLICATIONS

0.82V Step-Down Converter



*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

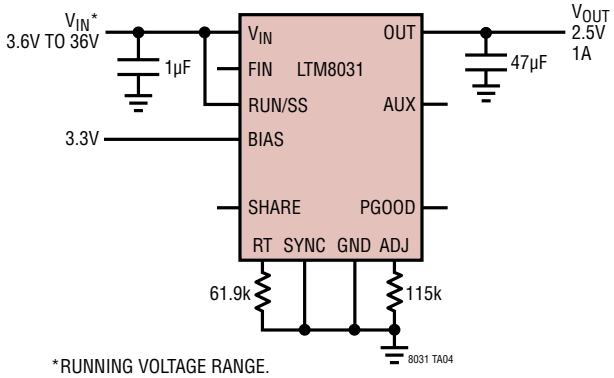
1.8V Step-Down Converter



*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

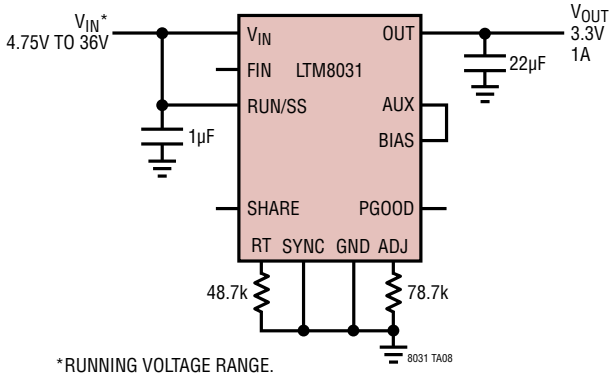
TYPICAL APPLICATIONS

2.5V Step-Down Converter



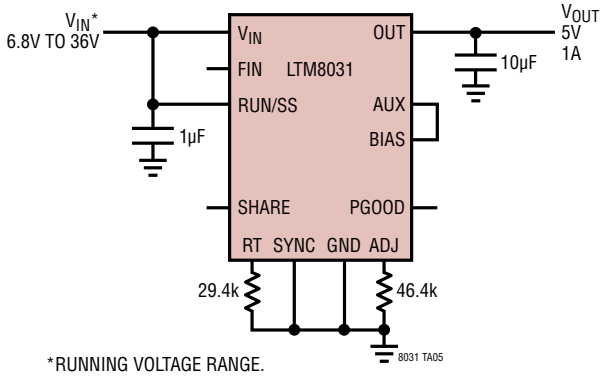
*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

3.3V Step-Down Converter



*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

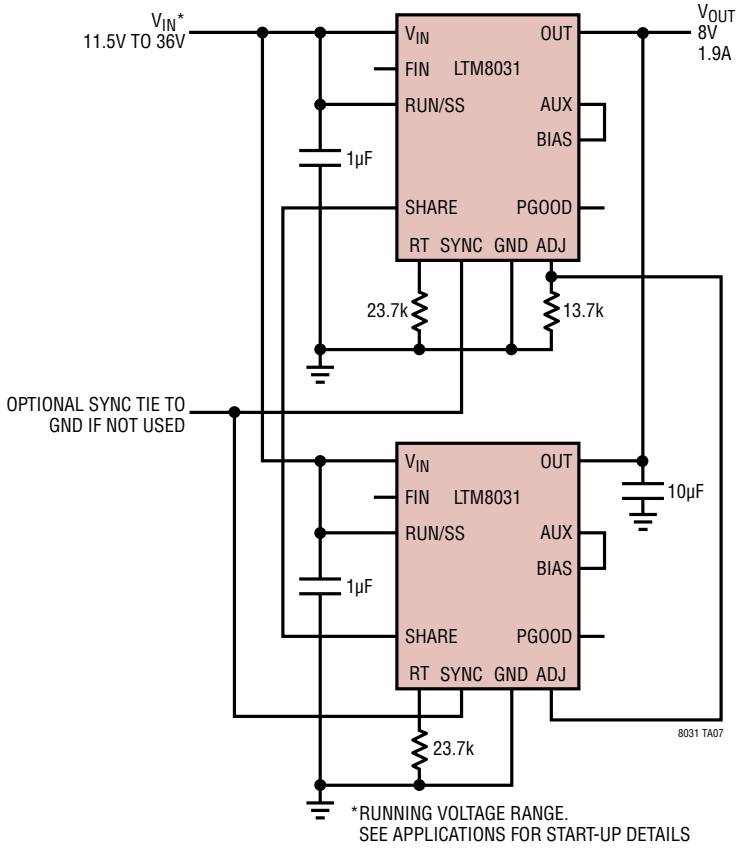
5V Step-Down Converter



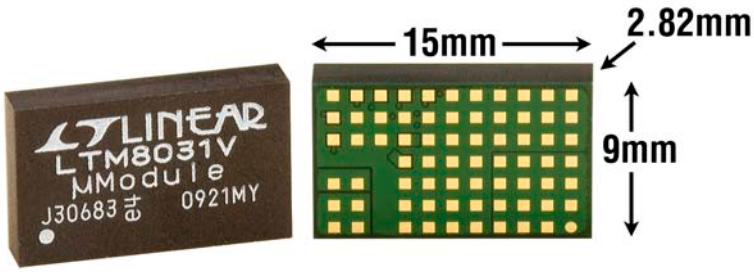
*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

TYPICAL APPLICATIONS

Two LTM8031s Operating in Parallel (Also See the LTM8032, 2A Pin Compatible)

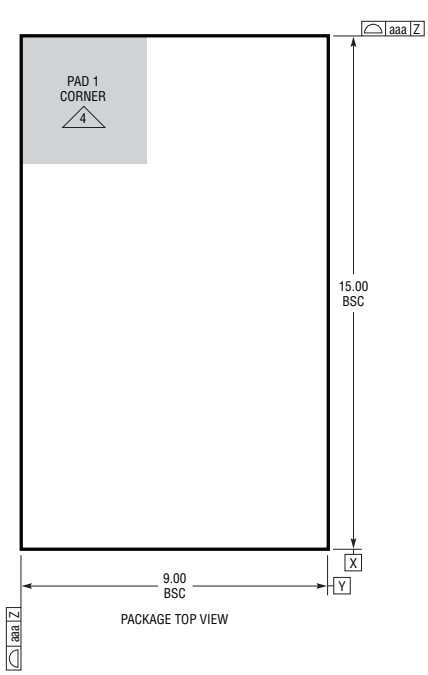


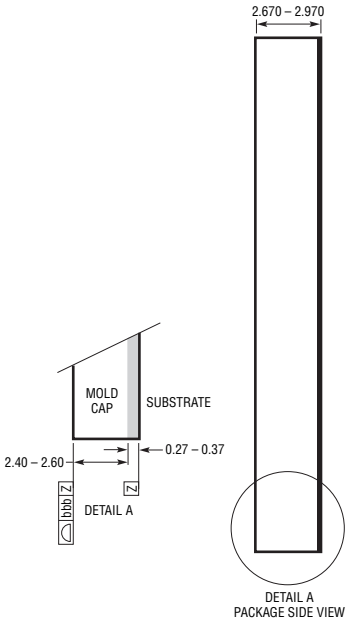
PACKAGE PHOTOGRAPH

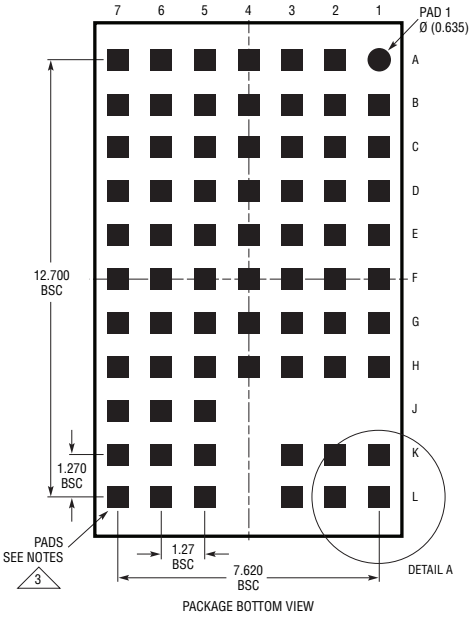


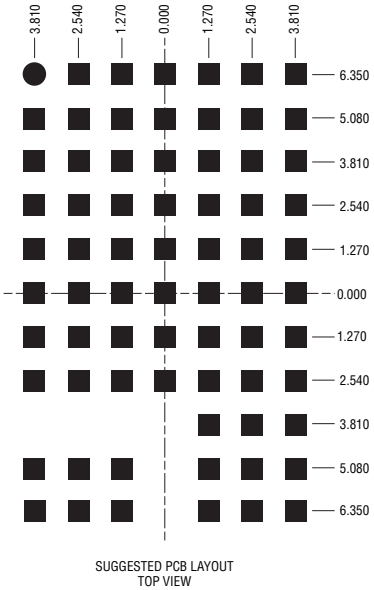
PACKAGE DESCRIPTION

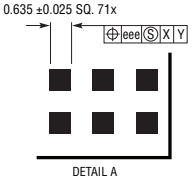
LGA Package
71-Lead (15mm × 9mm × 2.82mm)
(Reference LTC DWG # 05-08-1823 Rev Ø)





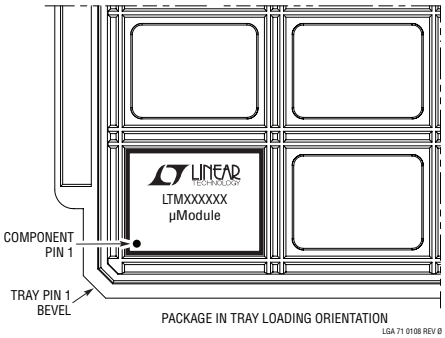






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010 AND SPP-020
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 71

SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10
eee	0.05



PACKAGE DESCRIPTION

Table 3. LTM8031 Pinout (Sorted by Pin Number)

PIN	SIGNAL DESCRIPTION
A1	V_{OUT}
A2	V_{OUT}
A3	V_{OUT}
A4	V_{OUT}
A5	GND
A6	GND
A7	GND
B1	V_{OUT}
B2	V_{OUT}
B3	V_{OUT}
B4	V_{OUT}
B5	GND
B6	GND
B7	GND
C1	V_{OUT}
C2	V_{OUT}
C3	V_{OUT}
C4	V_{OUT}
C5	GND
C6	GND
C7	GND
D1	V_{OUT}
D2	V_{OUT}
D3	V_{OUT}
D4	V_{OUT}
D5	GND
D6	GND
D7	GND
E1	GND
E2	GND
E3	GND
E4	GND
E5	GND
E6	GND
E7	GND

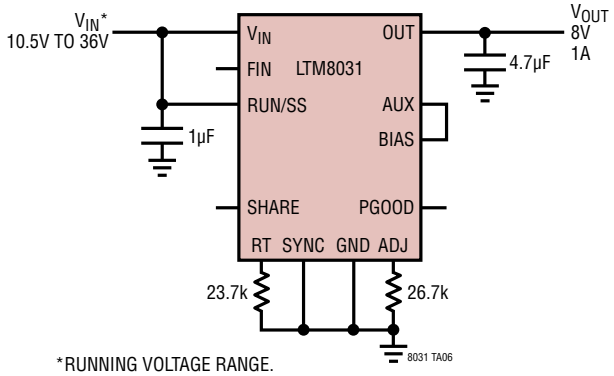
PIN	SIGNAL DESCRIPTION
F1	GND
F2	GND
F3	GND
F4	GND
F5	GND
F6	GND
F7	GND
G1	GND
G2	GND
G3	GND
G4	GND
G5	GND
G6	GND
G7	RT
H1	GND
H2	GND
H3	GND
H4	BIAS
H5	AUX
H6	GND
H7	SHARE
J5	GND
J6	GND
J7	ADJ
K1	V_{IN}
K2	V_{IN}
K3	FIN
K5	GND
K6	GND
K7	PGOOD
L1	V_{IN}
L2	V_{IN}
L3	FIN
L5	RUN/SS
L6	SYNC
L7	GND

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/10	Addition to Features	1
		Changes to Applications Information	11
B	04/12	Added MP-Grade part. Reflected throughout the data sheet	1-22

TYPICAL APPLICATION

8V Step-Down Converter



*RUNNING VOLTAGE RANGE.
SEE APPLICATIONS FOR START-UP DETAILS

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4606	Ultralow Noise 6A DC/DC µModule Regulator	$4.5V \le V_{IN} \le 28V$, $0.6V \le V_{OUT} \le 5V$, 15mm × 15mm × 2.8mm LGA
LTM4612	Ultralow Noise High V_{OUT} DC/DC µModule Regulator	5A, $5V \le V_{IN} \le 36V$, $3.3V \le V_{OUT} \le 15V$, 15mm × 15mm × 2.8mm LGA
LTM8023	36V, 2A DC/DC µModule Regulator	$3.6V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$, 9mm × 11.75mm × 2.8mm LGA
LTM8025	36V, 3A DC/DC µModule Regulator	$3.6V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 24V$, 9mm × 15mm × 4.32mm LGA
LTM8032	36V, 2A EMC DC/DC µModule Regulator	EN55022 Class B, 9mm × 15mm × 2.8mm LGA. Pin Compatible with the LTM8031

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

LTM8031EV#PBF LTM8031MPV#PBF LTM8031IV#PBF