Digital Camera Step-Down Power Supply

ABSOLUTE MAXIMUM RATINGS

VDDM, VH, ONM to GND .....-0.3V to +12V
PGNDM, PGND to GND .....-0.3V to +0.3V
VH to VDDM .....-6V to +0.3V
VL to VDDM .....-12V to +0.3V
VL, ONC, ON1, FB_, DCON_ to GND .....-0.3V to +6V
VDDC, REF, OSC, COMP_ to GND .....-0.3V to (VL + 0.3V)
DHM, DLM to PGNDM.....-0.3V to (VDDM + 0.3V)
LXM to PGNDM .....-0.6V to (VDDM + 0.6V)
DL1, DL2, DL3, LXC to PGND .....-0.3V to (VDDC + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFP (derate 11.1mW/°C above +70°C).....889mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range. .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3V, PGNDM = PGND = GND, DCON1 = REF, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{IN}		2.5		11	V
SUPPLY CURRENT						
Shutdown Supply Current (from VDDM and VDDC)		V_{ONM} = 0		3	20	µA
Main DC-DC Converter Supply Current (from VDDM)		V_{FBM} = 1.5V, V_{VDDC} = 0		370	600	µA
		V_{FBM} = 1.5V, V_{VDDC} = 3V		35	55	
Main DC-DC Converter Supply Current (from VDDC)		V_{FBM} = 1.5V, V_{VDDC} = 3V		270	450	µA
Main plus Core Supply Current (from VDDC)		V_{FBM} = V_{FBC} = 1.5V, V_{ONC} = 3V		410	700	µA
Main plus Auxiliary 1 Supply Current (from VDDC)		V_{FBM} = V_{FB1} = 1.5V, V_{ON1} = 3V		470	750	µA
Main plus Auxiliary 2 Supply Current (from VDDC)		V_{FBM} = V_{FB2} = 1.5V, V_{DCON2} = 3V		470	750	µA
Main plus Auxiliary 3 Supply Current (from VDDC)		V_{FBM} = V_{FB3} = 1.5V, V_{DCON3} = 3V		470	750	µA
Total Supply Current (from VDDC)		V_{FBM} = V_{FBC} = V_{FB1} = V_{FB2} = V_{FB3} = 1.5V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 3V		960	1700	µA
VL REGULATOR						
VL Output Voltage		6V < V_{VDDM} < 11V, 0.1mA < I_{LOAD} < 10mA	2.83	3.00	3.12	V
VL Supply Rejection		3.5V < V_{VDDM} < 11V, V_{VDDC} = 0			3	%
VL Undervoltage Lockout Threshold		VL rising, 40mV hysteresis	2.25	2.40	2.50	V
VL Switchover Voltage to VDDC		VL rising, 100mV hysteresis	2.3	2.4	2.5	V
VL to VDDC Switch Resistance					7	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3V, PGNDM = PGND = GND, DCON1 = REF, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
Reference Output Voltage	V_{REF}	I_{REF} = 20µA	1.235	1.248	1.260	V
REF Load Regulation		10µA < I_{REF} < 200µA		5	9	mV
REF Line Rejection		2.7V < V_{OUT} < 5.5V		1	5	mV
REF Undervoltage Lockout Threshold		REF rising, 20mV hysteresis	0.9	1	1.1	V
OSCILLATOR						
OSC Discharge Trip Level		OSC rising	1.225	1.250	1.275	V
OSC Input Bias Current		V_{OSC} = 1.1V		0.2	100	nA
OSC Discharge Resistance		V_{OSC} = 1.5V		30	100	Ω
OSC Discharge Pulse Width				100		ns
LOGIC INPUTS (ONM, ONC, ON1)						
Input Low Level	V_{IL}				0.4	V
Input High Level	V_{IH}	ONM	1.8			V
		ONC, ON1	1.6			
Input Leakage Current		ONM: V_{IN} = 0 or 11V; ONC, ON1: V_{IN} = 0 or 5V		0.01	1	µA
MAIN DC-DC CONVERTER						
Main Output Voltage Adjust Range	V_{OUT}		2.7		5.5	V
Main Idle Mode™ Threshold		V_{OSC} = 0.625V, measured between VDDM and LXM	8	20	32	mV
Main Current-Sense Amplifier Voltage Gain	A_{VCSM}	Measured between VDDM and LXM	8.4	9.3	10.2	V/V
Main N Channel Turn-Off Threshold		Measured between LXM and PGNDM	-26	-17	-8	mV
Main Slope Compensation Gain	A_{VSWM}		0.16	0.20	0.24	V/V
MAIN ERROR AMPLIFIER						
FBM Regulation Voltage		Unity gain configuration, FBM = COMPM	1.233	1.248	1.263	V
FBM to COMPM Transconductance	G_{EA}	Unity gain configuration, FBM = COMPM, -5µA < I_{LOAD} < 5µA	70	100	160	µS
FBM Input Leakage Current		V_{FBM} = 1.35V		5	100	nA
COMPM Minimum Output Voltage		V_{FBM} = 1.35V, COMPM open	0.3			V
COMPM Maximum Output Voltage	$V_{COMPM(MAX)}$	V_{FBM} = 1.15V, COMPM open	2.00	2.14	2.27	V

Idle Mode is a trademark of Maxim Integrated Products.

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3V, PGNDM = PGND = GND, DCON1 = REF, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SOFT-START						
Soft-Start Interval		OSC falling edge		1024		OSC cycles
MAIN DRIVERS (DHM, DLM)						
Output Low Voltage		I_{SINK} = 10mA			0.11	V
Output High Voltage		I_{SOURCE} = 10mA	V_{VDDM} - 0.11			V
Driver Resistance		I_{DHM} = 10mA, I_{DLM} = 10mA		4	11	Ω
Drive Current		Sourcing or sinking, V_{DHM} or V_{VL} = V_{VDDM} / 2		400		mA
CORE DC-DC CONVERTER (V_{ONC} = 3V)						
Core Output Voltage Adjust Range	V_{OUT}		1.25		5.5	V
Core Idle Mode Threshold		V_{OSC} = 0.625V	70	190	320	mA
Core Current-Sense Amplifier Transresistance	R_{CSC}		0.7	1.0	1.3	V/A
Core Slope Compensation Gain	A_{VSWC}		0.16	0.20	0.24	V/V
CORE ERROR AMPLIFIER (V_{ONC} = 3V)						
FBC Regulation Voltage		Unity gain configuration, FBC = COMPC	1.233	1.248	1.263	V
FBC to COMPC Transconductance	G_{EA}	Unity gain configuration, FBC = COMPC, -5µA < I_{LOAD} < 5µA	70	100	160	µS
FBC Input Leakage Current		V_{FBC} = 1.35V		5	100	nA
COMPC Minimum Output Voltage		V_{FBC} = 1.35V, COMPC open	0.3			V
COMPC Maximum Output Voltage	$V_{COMPM(MAX)}$	V_{FBC} = 1.15V, COMPC open	2.00	2.14	2.27	V
CORE SOFT-START (V_{ONC} = 3V)						
Soft-Start Interval				1024		OSC cycles
CORE POWER SWITCHES (V_{ONC} = 3V)						
LXC Leakage Current		V_{LXC} = 0, 5.5V		0.01	20	µA
Switch On-Resistance	R_{DSN}	N-channel, I_{LXC} = 0.75A		150	350	mΩ
	R_{DSP}	P-channel, I_{LXC} = 0.75A		180	400	
P-Channel Current Limit		V_{OSC} = 0.625V		0.75		A
N-Channel Turn-Off Current			18	100	180	mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3V, PGNDM = PGND = GND, DCON1 = REF, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AUXILIARY DC-DC CONTROLLERS 1, 2, 3 (V_{ON1} = $V_{CON\_}$ = 3V)						
INTERNAL CLOCK						
OSC Clock Low Trip Level		OSC falling edge	0.2	0.25	0.3	V
OSC Clock High Trip Level		$V_{DCON\_}$ = 0.625V	0.575	0.625	0.675	V
		$V_{DCON\_}$ = 1.25V to V_{VL}	1.00	1.05	1.10	
Maximum Duty Cycle Adjustment Range			40		90	%
Maximum Duty Cycle		$V_{DCON\_}$ = 0.625V		43		%
Default Maximum Duty Cycle		$V_{DCON\_}$ = 1.25V to V_{VL}		76		%
DCON_ Input Leakage Current		$V_{DCON\_}$ = 0V to 3V		0.01	1	µA
DCON_ Input Sleep-Mode Threshold		$V_{DCON\_}$ rising, 50mV hysteresis	0.35	0.4	0.45	V
AUXILIARY ERROR AMPLIFIER						
FB_ Regulation Voltage		Unity gain configuration, FB_ = COMP_	1.233	1.248	1.263	V
FB_ to COMP_ Transconductance	G_{EA}	Unity gain configuration, FB_ = COMP_, -5µA < ILOAD < 5µA	70	100	160	µs
FB_ Input Leakage Current		$V_{FB\_}$ = 1.35V		5	100	nA
AUXILIARY DRIVERS (DL1, DL2, DL3)						
DL_ Driver Resistance		Output high or low		4	11	Ω
DL_ Drive Current		Sourcing or sinking, $V_{DL\_}$ = V_{VDDC} / 2		400		mA
AUXILIARY SOFT-START						
Soft-Start Interval				1024		OSC cycles
AUXILIARY SHORT-CIRCUIT PROTECTION						
Fault Interval				1024		OSC cycles

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ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3V, PGNDM = PGND = GND, DCON1 = REF, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{IN}		2.5		11	V
SUPPLY CURRENT						
Shutdown Supply Current (from VDDM and VDDC)		V_{ONM} = 0			20	µA
Main DC-DC Converter Supply Current (from VDDM)		V_{FBM} = 1.5V, V_{VDDC} = 0			600	µA
		V_{FBM} = 1.5V, V_{VDDC} = 3V			55	
Main DC-DC Converter Supply Current (from VDDC)		V_{FBM} = 1.5V, V_{VDDC} = 3V			450	µA
Main plus Core Supply Current (from VDDC)		V_{FBM} = V_{FBC} = 1.5V, V_{ONC} = 3V			700	µA
Main plus Auxiliary 1 Supply Current (from VDDC)		V_{FBM} = V_{FB1} = 1.5V, V_{ON1} = V_{DCON1} = 3V			750	µA
Main plus Auxiliary 2 Supply Current (from VDDC)		V_{FBM} = V_{FB2} = 1.5V, V_{DCON2} = 3V			750	µA
Main plus Auxiliary 3 Supply Current (from VDDC)		V_{FBM} = V_{FB3} = 1.5V, V_{DCON3} = 3V			750	µA
Total Supply Current (from VDDC)		V_{FBM} = V_{FBC} = V_{FB1} = V_{FB2} = V_{FB3} = 1.5V, V_{ONC} = V_{ON1} = V_{DCON1} = V_{DCON2} = V_{DCON3} = 3V			1700	µA
VL REGULATOR						
VL Output Voltage		6V < V_{VDDM} < 11V, 0.1mA < I_{LOAD} < 10mA	2.83		3.12	V
VL Supply Rejection		3.5V < V_{VDDM} < 11V, V_{VDDC} = 0			3	%
VL Undervoltage Lockout Threshold		V_L rising, 40mV hysteresis	2.25		2.50	V
VL Switchover Voltage to VDDC		V_L rising, 100mV hysteresis	2.3		2.5	V
VL to VDDC Switch Resistance					7	Ω
REFERENCE						
Reference Output Voltage	V_{REF}	I_{REF} = 20µA	1.230		1.262	V
REF Load Regulation		10µA < I_{REF} < 200µA			9	mV
REF Line Rejection		2.7V < V_{OUT} < 5.5V			5	mV
REF Undervoltage Lockout Threshold		REF rising, 20mV hysteresis	0.9		1.1	V
OSCILLATOR						
OSC Discharge Trip Level		OSC rising	1.225		1.275	V
OSC Input Bias Current		V_{OSC} = 1.1V			100	nA
OSC Discharge Resistance		V_{OSC} = 1.5V			100	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3V, PGNDM = PGND = GND, DCON1 = REF, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (ONM, ONC, ON1)						
Input Low Level	V_{IL}				0.4	V
Input High Level	V_{IH}	ONM	1.8			V
		ONC, ON1	1.6			
Input Leakage Current		ONM: V_{IN} = 0 or 11V; ONC, ON1: V_{IN} = 0 or 5V			1	µA
MAIN DC-DC CONVERTER						
Main Output Voltage Adjust Range	V_{OUT}		2.7		5.5	V
Main Idle Mode Threshold		V_{OSC} = 0.625V, measured between VDDM and LXM	2		35	mV
Main Current-Sense Amplifier Voltage Gain	A_{VCSM}	Measured between VDDM and LXM	8.4		10.2	V/V
Main Zero-Crossing Threshold		Measured between LXM and PGNDM	-20		-8	mV
Main Slope Compensation Gain	A_{VSWM}		0.16		0.24	V/V
MAIN ERROR AMPLIFIER						
FBM Regulation Voltage		Unity gain configuration, FBM = COMPM	1.230		1.265	V
FBM to COMPM Transconductance	G_{EA}	Unity gain configuration, FBM = COMPM, -5µA < I_{LOAD} < 5µA	70		160	µS
FBM Input Leakage Current		V_{FBM} = 1.35V			100	nA
COMPM Minimum Output Voltage		V_{FBM} = 1.35V, COMPM open	0.3			V
COMPM Maximum Output Voltage	$V_{COMPM(MAX)}$	V_{FBM} = 1.15V, COMPM open	2.00		2.27	V
MAIN DRIVERS (DHM, DLM)						
Output Low Voltage		I_{SINK} = 10mA			0.11	V
Output High Voltage		I_{SOURCE} = 10mA	V_{VDDM} - 0.11			V
Driver Resistance		I_{DHM} = 10mA, I_{DLM} = 10mA			11	Ω
CORE DC-DC CONVERTER (V_{ONC} = 3V)						
Core Output Voltage Adjust Range	V_{OUT}		1.25		5.5	V
Core Idle Mode Threshold		V_{OSC} = 0.625V	40		360	mA
Core Current-Sense Amplifier Transresistance	R_{CSC}		0.7		1.3	V/A
Core Slope Compensation Gain	A_{VSWC}		0.16		0.24	V/V
CORE ERROR AMPLIFIER (V_{ONC} = 3V)						
FBC Regulation Voltage		Unity gain configuration, FBC = COMPC	1.230		1.265	V
FBC to COMPC Transconductance	G_{EA}	Unity gain configuration, FBC = COMPC, -5µA < I_{LOAD} < 5µA	70		160	µS

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3V, PGNDM = PGND = GND, DCON1 = REF, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

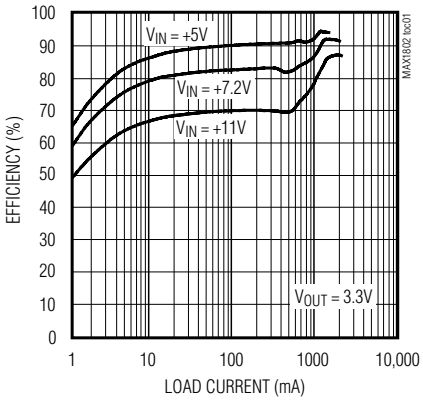
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FBC Input Leakage Current		V_{FBC} = 1.35V			100	nA
COMPC Minimum Output Voltage		V_{FBC} = 1.35V, COMPC open	0.3			V
COMPC Maximum Output Voltage	$V_{COMPC(MAX)}$	V_{FBC} = 1.15V, COMPC open	2.00		2.27	V
CORE POWER SWITCHES (V_{ONC} = 3V)						
LXC Leakage Current		V_{LXC} = 0, 5.5V			20	µA
Switch On-Resistance	R_{DSN}	N-channel, I_{LXC} = 0.75A			350	mΩ
	R_{DSP}	P-channel, I_{LXC} = 0.75A			400	
N-Channel Turn-Off Current			5		190	mA
AUXILIARY DC-DC CONTROLLERS 1, 2, 3 (V_{ON1} = $V_{DCON\_}$ = 3V)						
INTERNAL CLOCK						
OSC Clock Low Trip Level		OSC falling edge	0.2		0.3	V
OSC Clock High Trip Level		$V_{DCON\_}$ = 0.625V	0.575		0.675	V
		$V_{DCON\_}$ = 1.25V to V_{VL}	1.00		1.10	
Maximum Duty Cycle Adjustment Range			40		90	%
DCON_ Input Leakage Current		$V_{DCON\_}$ = 0V to 3V			1	µA
DCON_ Input Sleep-Mode Threshold		$V_{DCON\_}$ rising, 50mV hysteresis	0.35		0.45	V
AUXILIARY ERROR AMPLIFIER						
FB_ Regulation Voltage		Unity gain configuration, FB_ = COMP_	1.230		1.265	V
FB_ to COMP_ Transconductance	G_{EA}	Unity gain configuration, FB_ = COMP_, -5µA < I_{LOAD} < 5µA	70		160	µs
FB_ Input Leakage Current		$V_{FB\_}$ = 1.35V			100	nA
AUXILIARY DRIVERS (DL1, DL2, DL3)						
DL_ Driver Resistance		Output high or low			11	Ω

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

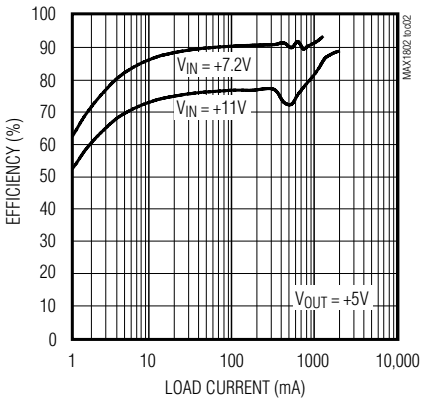
Typical Operating Characteristics

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3.3V, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, T_A = +25°C, unless otherwise noted.)

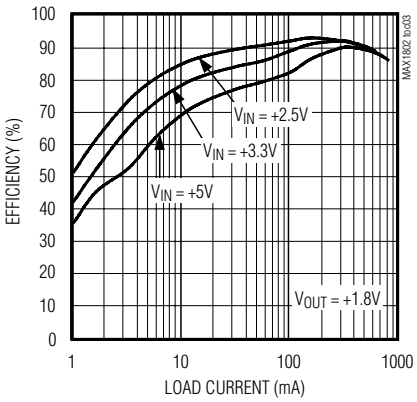
EFFICIENCY vs. LOAD CURRENT (MAIN CONVERTER)



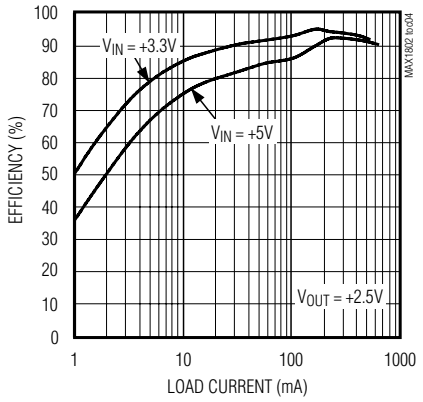
EFFICIENCY vs. LOAD CURRENT (MAIN CONVERTER)



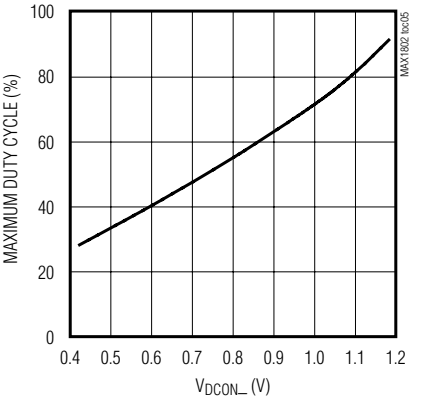
EFFICIENCY vs. LOAD CURRENT (CORE CONVERTER)



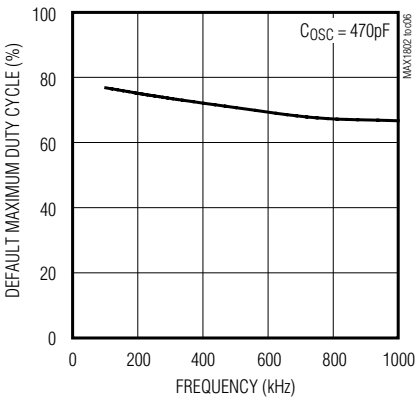
EFFICIENCY vs. LOAD CURRENT (CORE CONVERTER)



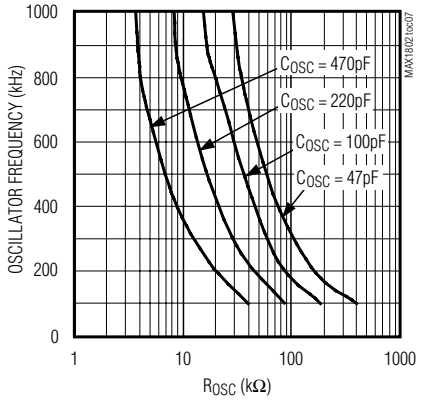
MAXIMUM DUTY CYCLE vs. $V_{DCON\_}$



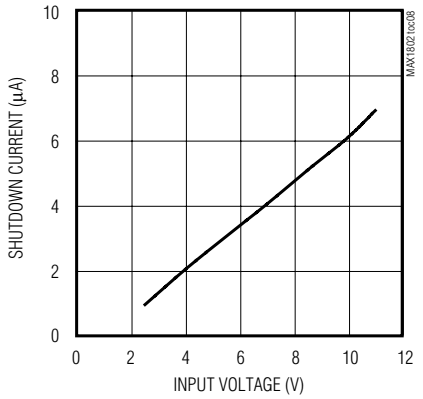
DEFAULT MAXIMUM DUTY CYCLE vs. FREQUENCY



OSCILLATOR FREQUENCY vs. R_{OSC}



SHUTDOWN CURRENT vs. INPUT VOLTAGE

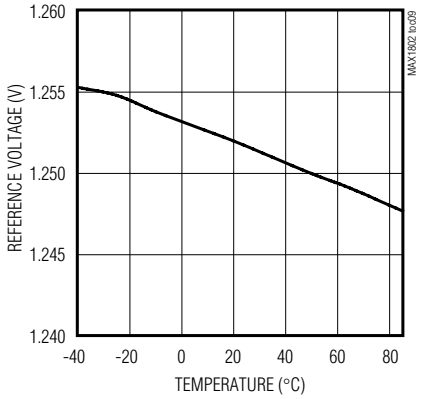


Digital Camera Step-Down Power Supply

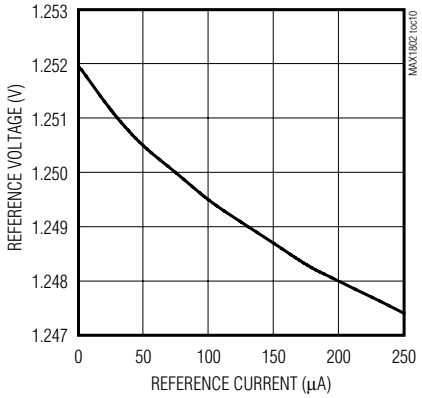
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3.3V, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, T_A = +25°C, unless otherwise noted.)

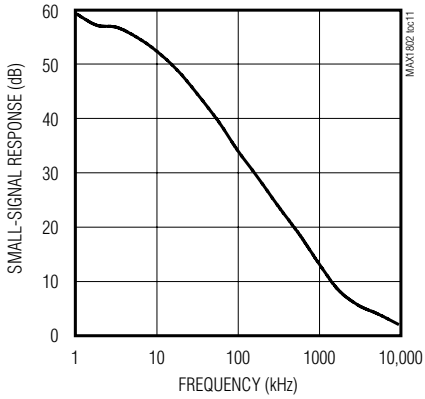
REFERENCE VOLTAGE vs. TEMPERATURE



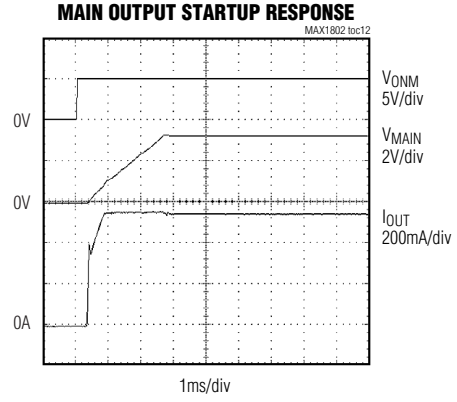
REFERENCE VOLTAGE vs. REFERENCE CURRENT



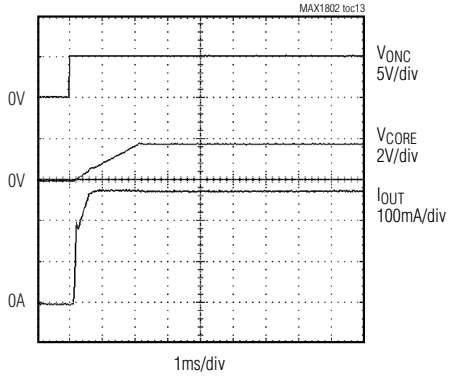
FB_ TO COMP_ SMALL-SIGNAL OPEN-LOOP FREQUENCY RESPONSE



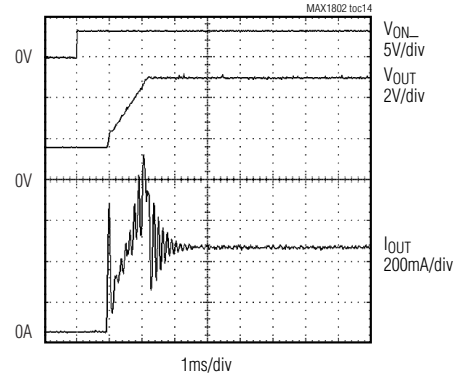
MAIN OUTPUT STARTUP RESPONSE



CORE OUTPUT STARTUP RESPONSE



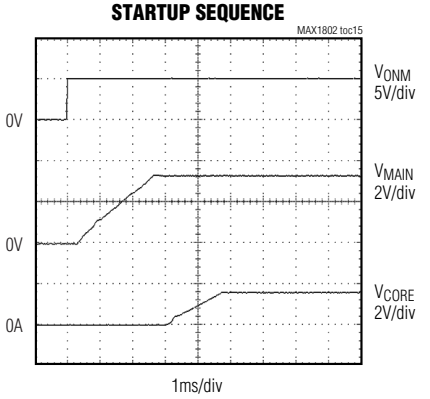
AUXILIARY CONTROLLER STARTUP RESPONSE



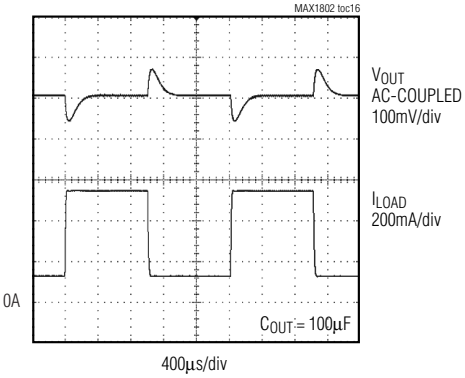
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{VDDM} = 6V, V_{VDDC} = 3.3V, V_{ONM} = 3V, V_{ONC} = V_{ON1} = V_{DCON2} = V_{DCON3} = 0, T_A = +25°C, unless otherwise noted.)

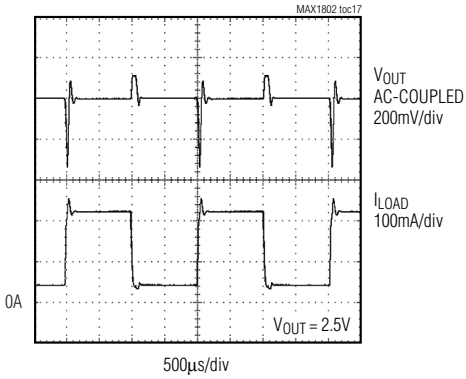
STARTUP SEQUENCE



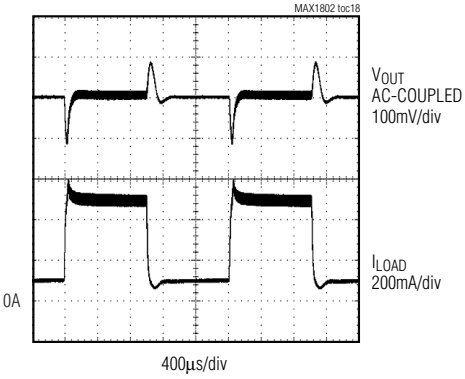
MAIN OUTPUT LOAD-TRANSIENT RESPONSE



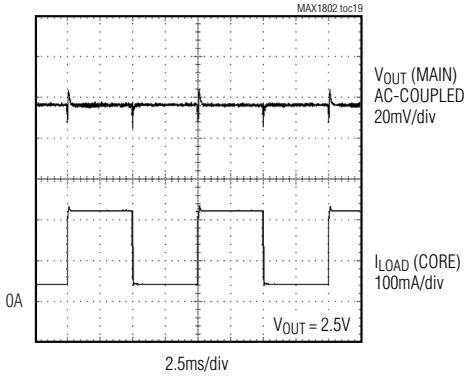
CORE OUTPUT LOAD-TRANSIENT RESPONSE



AUXILIARY OUTPUT LOAD-TRANSIENT RESPONSE



MAIN TRANSIENT RESPONSE SUBJECT TO CORE TRANSIENT



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Pin Description

PIN	NAME	FUNCTION
1	FBM	Main DC-DC Converter Feedback Input. Connect a feedback resistive voltage-divider from the output to FBM to set the main output voltage. Regulation voltage is V_{REF} (1.25V).
2	COMPM	Compensation for Main Controller. Output of main transconductance error amplifier. Connect a series resistor and capacitor to GND to compensate the main control loop (see *Compensation Design*).
3	ONM	Main Converter Enable Input. High level turns on the main converter and VL regulator. Connect ONM to VDDM to automatically start the converter. When the main converter is off, all other outputs are disabled.
4	VH	Internal Bias Voltage. VH provides bias to the main controller. Bypass VH to VDDM with a 0.1µF or greater ceramic capacitor.
5	VDDM	Battery Input. VDDM supplies power to the IC and also serves as a high-side current-sense input for the main DC-DC controller. Connect VDDM as close as possible to the source of the external P-channel switching MOSFET for the main controller.
6	DHM	External P-Channel MOSFET Gate-Drive Output for Main Controller. DHM swings between VDDM and PGNDM with 400mA (typ) drive current. Connect DHM to the gate of the external P-channel switching MOSFET for the main controller.
7	LXM	Main DC-DC Controller Current-Sense Input. Connect LXM to the drains of the external P- and N-channel switching MOSFETs for the main converter. LXM serves as the current-sense input for both P- and N-channel switching MOSFETs. Connect LXM as close as possible to the drain of the external P-channel switching MOSFET for the main controller.
8	DLM	External N-Channel MOSFET Gate-Drive Output for Main Controller. DLM swings between VDDM and PGNDM with 400mA (typ) drive current. Connect DLM to the gate of the external N-channel switching MOSFET for the main controller.
9	PGNDM	Power Ground for Main DC-DC Controller. PGNDM also serves as a low-side current-sense input for the main DC-DC controller. Connect PGNDM as close as possible to the source of the external N-channel switching MOSFET for the main controller.
10	OSC	Oscillator Control. Connect a timing capacitor from OSC to GND and a timing resistor from OSC to VL to set the switching frequency between 100kHz and 1MHz (see *Setting the Switching Frequency*).
11	DCON1	Maximum Duty Cycle Control Input for Auxiliary Controller 1. Connect DCON1 to VL to set the default maximum duty cycle. Connect a resistive voltage-divider from REF to DCON1 to set the maximum duty cycle between 40% and 90%. Pull DCON1 below 300mV to turn the controller off.
12	DL1	External MOSFET Gate Drive Output for Auxiliary Controller 1. DL1 swings between VDDC and PGND with 400mA (typ) drive current. Connect DL1 to the gate of the external switching N-channel MOSFET for auxiliary controller 1.
13	ON1	Enable Input for Auxiliary Controller 1. Connect ON1 to VL to automatically start auxiliary controller 1.
14	COMP1	Compensation for Auxiliary Controller 1. Output of auxiliary controller 1 transconductance error amplifier. Connect a series resistor and capacitor from COMP1 to GND to compensate the auxiliary controller 1 control loop (see *Compensation Design*).
15	FB1	Feedback Input for Auxiliary Controller 1. Connect a feedback resistive voltage-divider from the output of auxiliary controller 1 to FB1 to set the output voltage. Regulation voltage is V_{REF} (1.25V).
16	FB2	Feedback Input for Auxiliary Controller 2. Connect a feedback resistive voltage-divider from the output of auxiliary controller 2 to FB2 to set the output voltage. Regulation voltage is V_{REF} (1.25V).

Pin Description (continued)

PIN	NAME	FUNCTION
17	COMP2	Compensation for Auxiliary Controller 2. Output of auxiliary controller 2 transconductance error amplifier. Connect a series resistor and capacitor from COMP2 to GND to compensate the auxiliary controller 2 control loop (see *Compensation Design*).
18	DCON2	Maximum Duty Cycle Control Input for Auxiliary Controller 2. Connect DCON2 to VL to set the default maximum duty cycle. Connect a resistive voltage-divider from REF to DCON2 to set the maximum duty cycle between 40% and 90%. Pull DCON2 below 300mV to turn the controller off.
19	DL2	External MOSFET Gate Drive Output for Auxiliary Controller 2. DL2 swings between VDDC and PGND with 400mA (typ) drive current. Connect DL2 to the gate of the external switching N-channel MOSFET for auxiliary controller 2.
20	DL3	External MOSFET Gate Drive Output for Auxiliary Controller 3. DL3 swings between VDDC and PGND with 400mA (typ) drive current. Connect DL3 to the gate of the external switching N-channel MOSFET for auxiliary controller 3.
21	COMP3	Compensation for Auxiliary Controller 3. Output of auxiliary controller 3 transconductance error amplifier. Connect a series resistor and capacitor from COMP3 to GND to compensate the auxiliary controller 3 control loop (see *Compensation Design*).
22	FB3	Feedback Input for Auxiliary Controller 3. Connect a feedback resistive voltage-divider from the output of auxiliary controller 3 to FB3 to set the output voltage. Regulation voltage is V_{REF} (1.25V).
23	DCON3	Maximum Duty Cycle Control Input for Auxiliary Controller 3. Connect DCON3 to VL to set the default maximum duty cycle. Connect a resistive voltage-divider from REF to DCON3 to set the maximum duty cycle between 40% and 90%. Pull DCON3 below 300mV to turn the controller off.
24	ONC	Core Converter Enable Input. High level turns on the core converter. Connect ONC to VL to automatically start the core converter.
25	PGND	Power Ground. Sources of internal N-channel MOSFET power switches. Connect PGND to GND as close to the IC as possible.
26	LXC	Core Power Switching Node. Drains of the internal P- and N-channel MOSFET switches for the core converter.
27	VDDC	Core DC-DC Converter Power Input. VDDC is connected to the source of the internal P-channel MOSFET power switch for the core converter. VDDC is limited to 5.5V. For battery voltages greater than 5.5V, connect VDDC to the main output. Bypass VDDC to PGND with a 1µF or greater ceramic capacitor.
28	VL	Internal Low-Voltage Bypass. The internal circuitry is powered from VL. An internal linear regulator powers VL from VDDM when VDDC is less than 2.4V. When VDDC is greater than 2.4V, an internal switch connects VL to VDDC. Bypass VL to GND with a 1.0µF or greater ceramic capacitor.
29	COMPC	Compensation for Core Converter. Output of core transconductance error amplifier. Connect a series resistor and capacitor to GND to compensate the core control loop (see *Compensation Design*).
30	FBC	Core DC-DC Converter Feedback Input. Connect a feedback resistive voltage-divider from the core output to FBC to set the output voltage. Regulation voltage is V_{REF} (1.25V).
31	REF	1.25V Reference Output. Bypass REF to GND with a 0.1µF or greater ceramic capacitor.
32	GND	Analog Ground

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Detailed Description

The MAX1802 typical application circuit is shown in Figure 1. It features two step-down DC-DC converters (main and core), three auxiliary step-up DC-DC controllers, and control capability for multiple external MAX1801 slave DC-DC controllers. Together, these provide a complete high-efficiency power-supply solution for digital still cameras. Figures 2 and 3 show the MAX1802 functional block diagrams.

Master-Slave Configuration

The MAX1802 supports MAX1801 "slave" controllers that obtain input power, a voltage reference, and an oscillator signal directly from the MAX1802 "master" DC-DC converter. The master-slave configuration reduces system cost by eliminating redundant circuitry and controlling the harmonic content of noise with synchronized converter switching.

Main DC-DC Converter

The MAX1802 main step-down DC-DC converter generates a 2.7V to 5.5V output voltage from a 2.5V to 11V battery input voltage. When the battery voltage is lower than the main regulation voltage, the regulator goes into dropout and the P-channel switch remains on. In this condition, the output voltage is slightly lower than the input voltage. The converter drives an external P-channel MOSFET power switch and an external N-channel MOSFET synchronous rectifier. The converter operates in a low-noise, constant-frequency PWM current mode to regulate the voltage across the load. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered.

The external P-channel MOSFET switch turns on during the first part of each cycle, allowing current to ramp up in the inductor and store energy in a magnetic field while supplying current to the load. During the second part of each cycle, the P-channel MOSFET turns off and the voltage across the inductor reverses, forcing current through the external N-channel synchronous rectifier to the output filter capacitor and load. As the energy stored in the inductor is depleted, the current ramps down. The synchronous rectifier turns off when the inductor current approaches zero or at the beginning of a new cycle, at which time the P-channel switch turns on again.

The current-mode PWM converter uses the voltage at COMPM to program the inductor current and regulate the output voltage. The converter detects inductor current by sensing the voltage across the source and drain of the external P-channel MOSFET. The MAX1802 main output switches to Idle Mode at light loads to improve efficiency by leaving the P-channel switch on until the voltage across the MOSFET reaches the 20mV Idle Mode threshold. The Idle Mode current is 20mV divided by the MOSFET on-resistance. By forcing the inductor current above the Idle Mode threshold, more energy is supplied to the output capacitor than is required by the load. The switch and synchronous rectifiers then remain off until the output capacitor discharges to the regulation voltage. This causes the converter to operate at a lower effective switching frequency at light loads, thus improving efficiency.

An internal comparator turns off the N-channel synchronous rectifier as the inductor current drops near zero, by measuring the voltage across the MOSFET. If the N-channel MOSFET on-resistance is low (less than that of the P-channel switch), it may cause the MOSFET to turn off prematurely, degrading efficiency. This is especially critical for high input voltage applications, such as with 2 series Li+ cells. In this case, use an N-channel MOSFET with greater on-resistance than the P-channel switch, and/or place a Schottky recitifier across the N-channel MOSFET gate-source.

The voltage at COMPM is typically clamped to $V_{COMPM(MAX)}$ = 2.14V, thereby limiting the inductor current. The peak inductor current (I_{LIM}) and the maximum average output current ($I_{OUT(MAX)}$) are determined by the following equations:

$$I_{LIM} = \frac{V_{COMPM(MAX)} - V_{REF}\left(1 + \frac{V_{OUT} A_{VSWM}}{V_{IN}}\right)}{A_{VCSM} R_{DSP}}$$

$$I_{OUT(MAX)} = I_{LIM} - \left[\frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) V_{OUT}}{2 f_{OSC} L}\right]$$

where A_{VSWM} is the main slope compensation gain (0.20V/V), A_{VCSM} is the voltage gain of the main current-sense amplifier (9.3V/V), R_{DSP} is the on-resistance of the external P-channel MOSFET switch, and L is the inductor value. Note that the current limit increases as the input/output voltage ratio increases.

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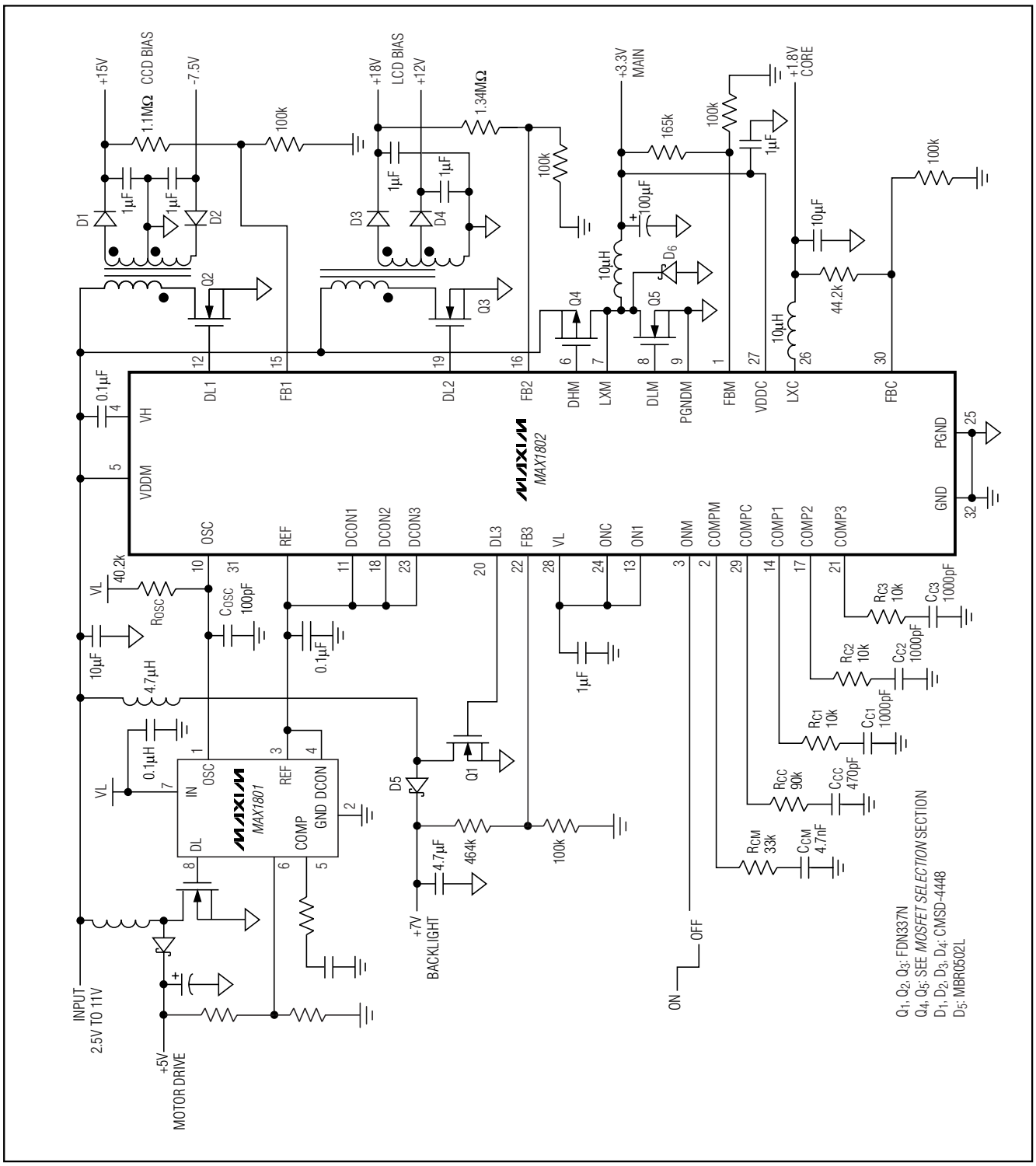

Figure 1. Typical Application Circuit

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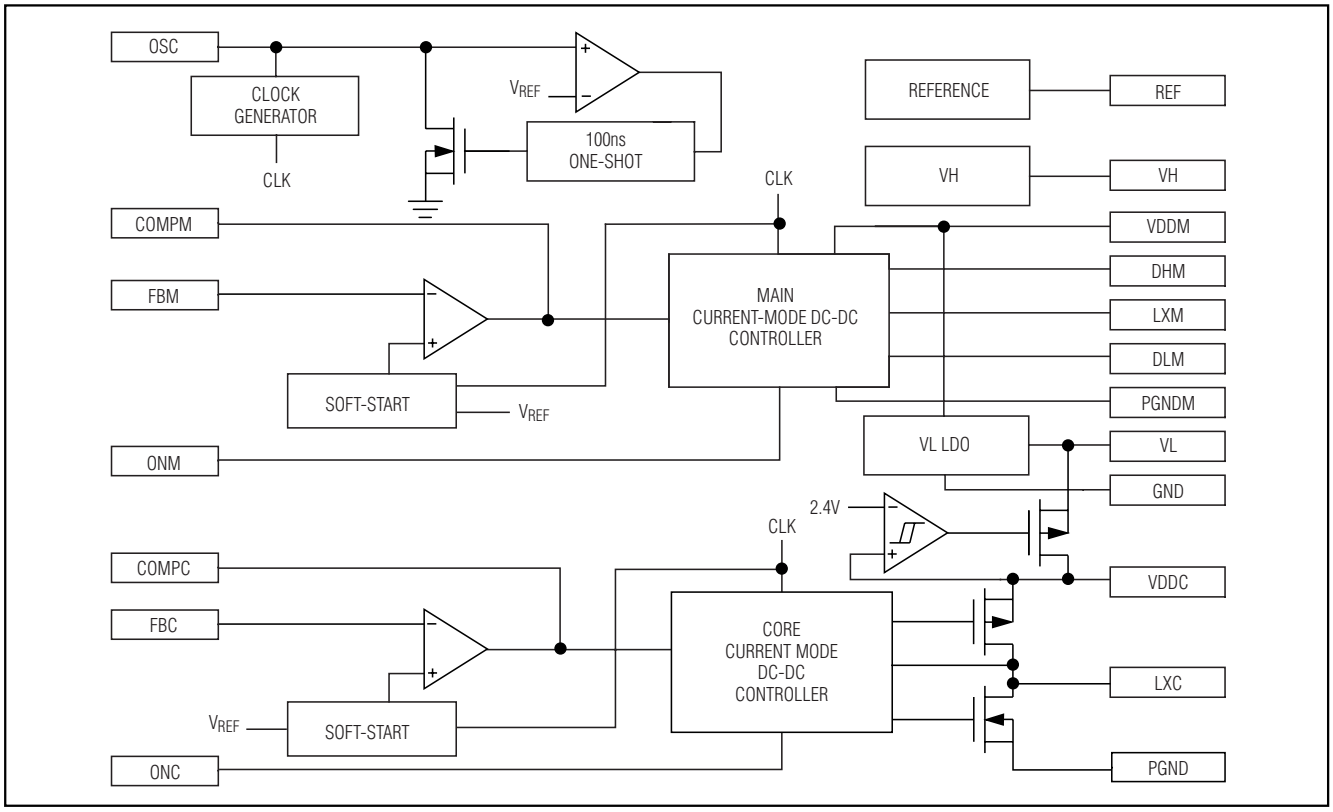

Figure 2. Simplified Block Diagram, Including Main and Core

Core DC-DC Converter

The MAX1802 core step-down DC-DC converter generates a 1.25V to 5.5V output voltage from the main controller output. The core converter has the same low-noise, constant-frequency PWM current-mode architecture as the main controller. However, it uses an internal P-channel MOSFET power switch and N-channel MOSFET synchronous rectifier to maximize efficiency and reduce circuit size and external component count. The core converter internally monitors the inductor current for current-mode regulation of the output voltage, as well as overload protection, automatic Idle Mode switchover, and turning off the synchronous rectifier when the inductor current approaches zero. By switching to Idle Mode at light loads and turning the synchronous rectifier off at zero current, light-load efficiency is improved. The core converter is inactive until the main output has started.

The voltage at COMPC is typically clamped to $V_{COMPC(MAX)}$ = 2.14V, thereby limiting the inductor current. The peak inductor current limit (I_{LIM}) and the maximum average output current ($I_{OUT(MAX)}$) are determined by the following equations:

$$I_{LIM} = \frac{V_{COMPC(MAX)} - V_{REF}\left(1 + \frac{V_{OUT} A_{VSWC}}{V_{IN}}\right)}{R_{CSC}}$$

$$I_{OUT(MAX)} = I_{LIM} - \left[\frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) V_{OUT}}{2 f_{OSC} L}\right]$$

where A_{VSWC} is the core slope compensation gain (0.20V/V), R_{CSC} is the transresistance of the core current-sense amplifier (1V/A), and L is the inductor value. Note that the current limit increases as the input/output ratio increases.

Auxiliary DC-DC Controllers

The MAX1802's three auxiliary controllers operate in a low-noise, fixed-frequency, PWM mode with output power limited by the external components. The con-

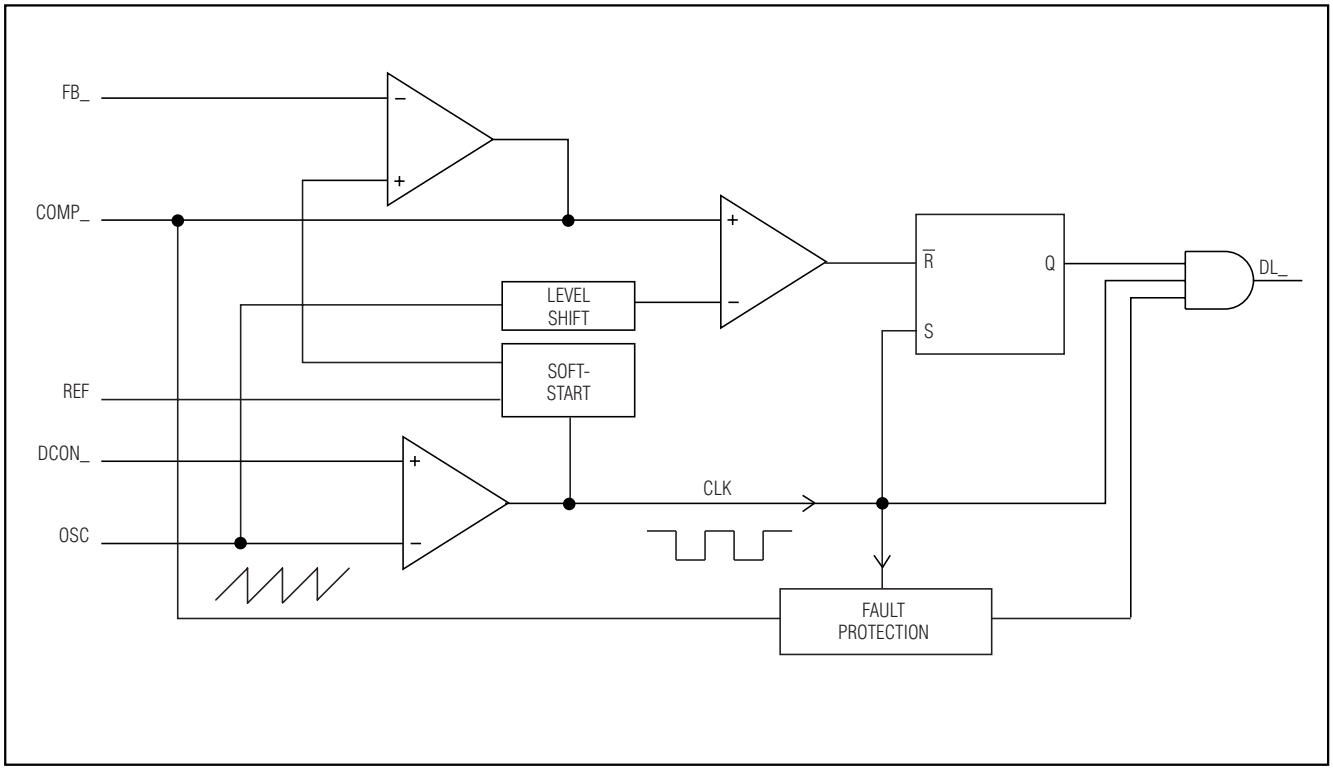

Figure 3. Auxiliary Controller Block Diagram

trollers regulate their output voltages by modulating the pulse width of the drive signal for an external N-channel MOSFET switch. The auxiliary controllers are inactive until the main output has started.

Figure 3 shows a block diagram for a MAX1802 auxiliary PWM controller. The sawtooth oscillator signal at OSC governs the internal timing. At the beginning of each cycle, DL_ goes high to turn on the external MOSFET switch. The MOSFET switch turns off when the internally level-shifted sawtooth rises above COMP_ or when the maximum duty cycle is exceeded. The switch remains off until the beginning of the next cycle. An internal transconductance amplifier establishes an integrated error voltage at COMP_, thereby increasing the loop gain for improved regulation accuracy.

Power-Up Sequence

The MAX1802 is in the shutdown state with all circuitry off when the ONM input is low (<1.3V). When ONM goes high, an internal linear regulator generates 3V at the VL output from the VDDM input to power internal circuitry. As VL rises above the 2.4V undervoltage lockout threshold, the internal reference and oscillator begin to function and the main DC-DC converter begins soft-start operation. The main DC-DC output reaches full regulation voltage after 1024 soft-start oscillator cycles. Once the main DC-DC converter completes soft-start, the core DC-DC converter and the auxiliary DC-DC controllers are enabled.

As the voltage at VDDC rises above 2.4V, the internal linear regulator turns off and an internal 3Ω switch connects VL directly to VDDC, which is typically connected to the output of the main DC-DC converter.

The core DC-DC converter and the auxiliary DC-DC controllers have independent on-off control and soft-start. The main DC-DC converter shuts down with a low input at ONM. The core DC-DC converter shuts down with a low input at ONC. Turn auxiliary DC-DC converter 1 off by driving either ON1 or DCON1 to GND. Turn off auxiliary controller 2 or 3 by driving DCON2 or DCON3 to GND.

Reference

The MAX1802 has an internal 1.248V, 1% reference. Connect a 0.1µF bypass capacitor from REF to GND within 0.2in (5mm) of the REF pin. REF can source up to 200µA of external load current, and it is enabled whenever ONM is high and VL is above the undervolt-

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age lockout threshold. The internal core converter, auxiliary controllers, and MAX1801 slave controllers each sink up to 30µA REF current during startup. If multiple MAX1801 controllers are turned on simultaneously, ensure that the master voltage reference can provide sufficient current, or buffer the reference with an appropriate unity-gain amplifier.

Oscillator

The oscillator uses a comparator, a 100ns one-shot, and an internal N-channel MOSFET switch in conjunction with an external timing resistor and capacitor to generate the oscillator signal at OSC (Figure 4). The capacitor voltage exponentially approaches VL from zero with a time constant given by the $R_{OSC}C_{OSC}$ product when the switch is open, and the comparator output becomes high when the capacitor voltage reaches V_{REF} (1.25V). At that time, the one-shot activates the internal MOSFET switch to discharge the capacitor within a 100ns interval, and the cycle repeats. Note that the oscillation frequency changes as VL changes during startup. The oscillation frequency is constant while the VL voltage is constant.

Maximum Duty Cycle

The MAX1802's three auxiliary controllers use the sawtooth oscillator signal generated at OSC, the voltage at DCON_, and an internal comparator to limit their maximum duty cycles (see *Setting the Maximum Duty Cycle*). Limiting the duty cycle can prevent saturation in some magnetic components. A low maximum duty cycle can also force the converter to operate in discontinuous current mode, simplifying design stability at the cost of a slight reduction in efficiency.

Soft-Start

All the MAX1802 converters feature a soft-start function that limits inrush current and prevents excessive battery loading at startup by ramping the output voltage to the regulation voltage. This is achieved by increasing the internal reference inputs to the controller transconductance amplifiers from 0 to the 1.25V reference voltage over 1024 oscillator cycles when initial power is applied or when the controller is enabled.

Overload Protection

The MAX1802's three auxiliary controllers have fault protection that prevents damage to transformer-coupled or SEPIC circuits due to an output overload condition. When the output voltage drops out of regulation for 1024 oscillator clock periods, the auxiliary controller is disabled to prevent excessive output current. Restart the controller by cycling the voltage at ON_ or DCON_ to GND and back to the on state. For a step-up application, short-circuit current is not limited, due to the DC current path through the inductor and output rectifier to the short circuit. If short-circuit protection is required in a step-up configuration, use a protection device such as a fuse to limit short-circuit current.

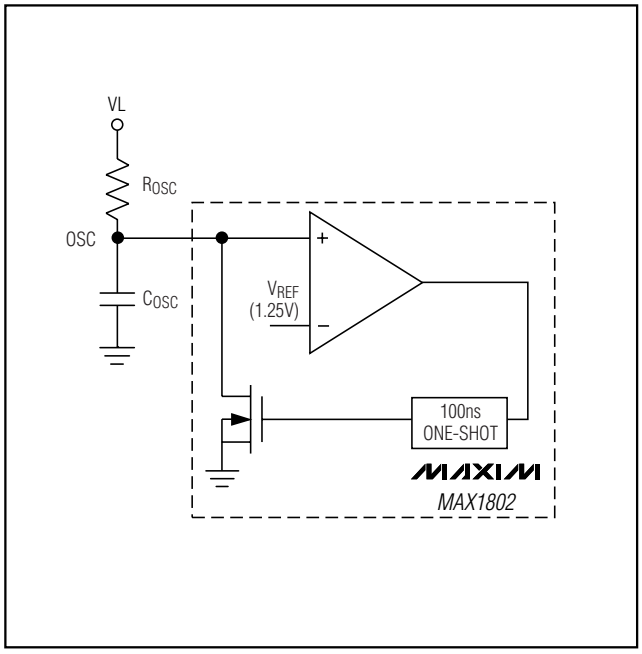

Figure 4. Oscillator

Design Procedure

Setting the Switching Frequency

Choose a switching frequency to optimize external component size or circuit efficiency for the particular MAX1802 application. Switching frequencies between 400kHz and 500kHz offer a good balance between component size and circuit efficiency. Higher frequencies allow smaller components, and lower frequencies improve efficiency.

The switching frequency is set with an external timing resistor (R_{OSC}) and capacitor (C_{OSC}). At the beginning of a cycle, the timing capacitor charges through the resistor until it reaches V_{REF}. The charge time t_1 is:

$$t_1 = -R_{OSC}(C_{OSC}+10pF) \ln [1 - (V_{REF} / V_{VL})]$$

Once the voltage at OSC reaches V_{REF}, it discharges through an internal switch over time t_2 = 200ns. The oscillator frequency is $f_{OSC} = 1 / (t_1 + t_2)$. Set f_{OSC} in the range $100kHz \le f_{OSC} \le 1MHz$. Choose C_{OSC} between 47pF and 470pF. Determine R_{OSC} from the relation:

$$R_{OSC} = (200ns - 1/f_{OSC}) / (C_{OSC} + 10pF) \times \ln (1 - V_{REF} / V_{VL})$$

See the *Typical Operating Characteristics* for f_{OSC} vs. R_{OSC} using different values of C_{OSC}. Due to duty cycle limitation in the main controller, keep $f_{OSC} \le V_{MAIN} / (V_{VDDM(MAX)} \times 500ns)$.

Setting the Output Voltages

Set the MAX1802 output voltage of each converter by connecting a resistive voltage-divider from the output voltage to the corresponding FB_ input. The FB_ input bias current is <100nA, so choose R_L (the low-side FB_-to-GND resistor) to be 100kΩ. Choose R_H (the high-side output-to-FB_ resistor) according to the relation:

$$R_H = R_L \left[\frac{V_{OUT}}{1.248} - 1 \right]$$

Setting the Maximum Duty Cycle

The oscillator signal at OSC and the voltage at DCON_ are used to generate the internal clock signals for the three MAX1802 auxiliary controllers (CLK in Figure 3). The internal clock's falling edge occurs when V_{OSC} exceeds $V_{DCON\_}$ (set by a resistive divider). The internal clock's rising edge occurs when V_{OSC} falls below 0.25V (Figure 5).

The adjustable maximum duty cycle range is 40% to 90% (see Maximum Duty Cycle vs. $V_{DCON\_}$ in the *Typical Operating Characteristics*). The maximum duty cycle defaults to 76% at 100kHz if $V_{DCON\_}$ is at or above the voltage at V_{REF} (1.25V) (see Default Maximum Duty Cycle vs. Frequency in the *Typical Operating Characteristics*). The controller shuts down if $V_{DCON\_}$ is <0.3V.

Inductor Selection

Main and Core Step-Down Converters

MAX1802 main and core step-down converters offer best efficiency when the inductor current is continuous. For most designs, a reasonable inductor value (L_{IDEAL}) can be derived from the following equation, which sets continuous peak-to-peak inductor current at 1/3 the DC inductor current:

$$L_{IDEAL} = \left(\frac{3(V_{IN} - V_{DSP}) D(1-D)}{I_{OUT} f_{OSC}} \right)$$

where D, the duty cycle, is given by:

$$D = \frac{V_{OUT} + V_{DSN}}{V_{IN} - V_{DSP} + V_{DSN}}$$

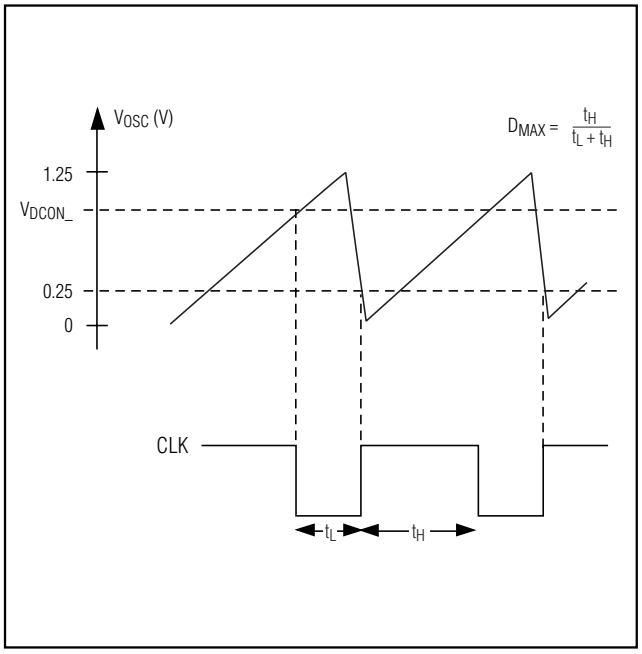

Figure 5. Auxiliary Controller Internal Clock Signal Generation

In these equations, V_{DSP} is the voltage drop across the P-channel MOSFET switch, and V_{DSN} is the voltage drop across the N-channel MOSFET synchronous rectifier. Given L_{IDEAL}, the consistent peak-to-peak inductor current is 0.33 I_{OUT}. The maximum inductor current is 1.17 I_{OUT}.

Inductance values smaller than L_{IDEAL} can be used; however, the maximum inductor current will rise as L is reduced, and a larger output capacitance will be required to maintain the same output ripple. For stable operation, the minimum inductance is limited by the internal slope compensation. The minimum inductor values for main and core are given by:

$$L_{MIN(MAIN)} = \left(1 - \frac{0.5}{D_{MAX}} \right) \frac{V_{OUT} R_{DSP}}{0.013 f_{OSC}}$$

and

$$L_{MIN(CORE)} = \left(1 - \frac{0.5}{D_{MAX}} \right) \frac{V_{OUT}}{0.13 f_{OSC}}$$

where R_{DSP} is the on-resistance of the P-channel MOSFET switch, and $D_{MAX} = V_{OUT} / V_{IN}$.

Auxiliary Step-Up Controllers

The three MAX1802 auxiliary step-up controllers offer best efficiency when the inductor current is continuous.

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Use discontinuous current when the step-up ratio (V_{OUT} / V_{IN}) is greater than 1 / (1 - D_{MAX}).

Continuous Inductor Current

A reasonable inductor value (L_{IDEAL}) can be derived from the following equation, which sets continuous peak-to-peak inductor current at 1/3 the DC inductor current:

$$L_{IDEAL} = \frac{3\left(V_{IN(MAX)} - V_{DSN}\right) D(1-D)}{I_{OUT}\, f_{OSC}}$$

where D, the duty cycle, is given by:

$$D \approx 1 - \frac{V_{IN}}{V_{OUT} + V_D}$$

In these equations, V_{DSN} is the voltage drop across the N-channel MOSFET switch, and V_D is the forward voltage drop across the rectifier. Given L_{IDEAL}, the consistent peak-to-peak inductor current is 0.33 I_{OUT} / (1 - D). The maximum inductor current is 1.17 I_{OUT} / (1 - D).

Inductance values smaller than L_{IDEAL} can be used; however, the maximum inductor current will rise as L is reduced, and a larger output capacitance will be required to maintain the same output ripple.

The inductor current will become discontinuous if I_{OUT} decreases by more than a factor of six from the value used to determine L_{IDEAL}.

Discontinuous Inductor Current

In the discontinuous mode, each MAX1802 auxiliary controller regulates the output voltage by adjusting the duty cycle to allow adequate power transfer to the load. To ensure regulation under worst-case load conditions (maximum I_{OUT}), choose:

$$L = \frac{V_{OUT}\, D_{MAX}}{2\, I_{OUT}\, f_{OSC}}$$

The peak inductor current is V_{IN} D_{MAX} / (L f_{OSC}).

The inductor's saturation current rating should meet or exceed the calculated peak inductor current.

Input and Output Filter Capacitors

The input capacitor (C_{IN}) reduces the current peaks drawn from the battery or input power source. The impedance of the input capacitor at the switching frequency should be less than that of the input source so that high-frequency switching currents do not pass through the input source.

The output capacitor is required to keep the output voltage ripple small and to ensure regulation control-loop stability. The output capacitor must have low impedance at the switching frequency. Tantalum and ceramic capacitors are good choices. Tantalum capacitors typically have high capacitance and medium-to-low equivalent series resistance (ESR) so that ESR dominates the impedance at the switching frequency. In turn, the output ripple is approximately:

$$V_{RIPPLE} \approx I_{L(p-p)}\, ESR$$

where $I_{L(p-p)}$ is the peak-to-peak inductor current.

Ceramic capacitors typically have lower ESR than tantalum capacitors, but with relatively small capacitance that dominates the impedance at the switching frequency. In turn, the output ripple is approximately:

$$V_{RIPPLE} \approx I_{L(p-p)}\, Z_C$$

where $I_{L(p-p)}$ is the peak-to-peak inductor current, and $Z_C \approx 1 / (2\, \pi\, f_{OSC}\, C_{OUT})$.

See the *Compensation Design* section for a discussion of the influence of output capacitance and ESR on regulation control-loop stability.

The capacitor voltage rating must exceed the maximum applied capacitor voltage. For most tantalum capacitors, manufacturers suggest derating the capacitor by applying no more than 70% of the rated voltage to the capacitor. Ceramic capacitors are typically used up to the voltage rating of the capacitor. Consult the manufacturer's specifications for proper capacitor derating.

MOSFET Selection

The MAX1802 main converter and auxiliary controllers drive external logic-level P- and/or N-channel MOSFETs as the circuit switching elements. The key selection parameters are:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Total gate charge (Q_g)
- Reverse transfer capacitance (C_{RSS})

Because the main converter's external MOSFETs are used for current sense, they directly determine the output current capability and efficiency of the main converter. It is important to select the appropriate external MOSFETs for the main converter. The P-channel on-resistance (R_{DSP}) at minimum input voltage (V_{VDDM}) must be low enough so that the converter can produce the desired output current as determined by the $I_{OUT(MAX)}$ equation in the *Main DC-DC Converter* section. The N-channel on-resistance (R_{DSN}) determines

the N-channel turn-off current (equal to 17mV/R_{DSN}). Choose R_{DSN} value between R_{DSP} and $3R_{DSP}$ to keep the N-channel turn-off current low for optimal efficiency. If a lower R_{DSN} is used, connect a Schottky diode from PGNDM to LXM for better efficiency (see *Diode Selection*).

For the main converter, the external gate drive swings between the voltage at VDDM and GND. For the auxiliary controllers, the external gate drive swings between the voltage at VDDC and GND. Use a MOSFET whose on-resistance is specified at or below the minimum gate drive voltage swing, and make sure that the maximum voltage swing does not exceed the maximum gate-source voltage specification of the MOSFET. The gate charge, Q_g, includes all capacitance associated with gate charging and helps to predict the transition time required to drive the MOSFET between on and off states. The power dissipated in the MOSFET is due to $R_{DS(ON)}$ and transition losses. The $R_{DS(ON)}$ loss is:

$$P_1 \approx D\ I_L^2\ R_{DS(ON)}$$

where D is the duty cycle, I_L is the average inductor current, and $R_{DS(ON)}$ is the on-resistance of the MOSFET. The transition loss is approximately:

$$P_2 \approx \frac{V_{SWING}\ I_L\ f_{OSC}\ t_T}{3}$$

where V_{SWING} is V_{OUT} for the auxiliary controllers or $V_{IN(MAX)}$ for the main and core converters, I_L is the average inductor current, f_{OSC} is the converter switching frequency, and t_T is the transition time. The transition time is approximately Q_g / I_G, where Q_g is the total gate charge, and I_G is the gate drive current (0.4A typ).

The total power dissipation in the MOSFET is $P_{MOSFET} = P_1 + P_2$.

Diode Selection

The main and core converters use synchronous rectifiers and thus do not require a diode. However, if the external N-channel synchronous rectifier has low on-resistance (less than the P-channel on-resistance), the high N-channel turn-off current results in lower efficiency. In that case, connect a Schottky diode, rated for maximum output current, from PGNDM to LXM to improve efficiency.

The auxiliary controllers require external rectifiers. For low-output-voltage applications, use a Schottky diode to rectify the output voltage because of the diode's low forward voltage and fast recovery time. Schottky diodes exhibit significant leakage current at high reverse voltages and high temperatures. Thus, for high-voltage, high-temperature applications, use ultra-fast junction rectifiers.

Compensation Design

Each DC-DC converter has an internal transconductance error amplifier whose output is used to compensate the control loop. Typically, a series resistor and capacitor are inserted from COMP_ to GND to form a pole-zero pair. The external inductor, the output capacitor, the compensation resistor and capacitor, and for the main converter, the external P-channel MOSFET, govern control-loop stability. The inductor and output capacitor are usually chosen in consideration of performance, size, and cost, but the compensation resistor and capacitor are chosen to optimize control-loop stability. The component values in the circuit of Figure 1 yield stable operation over a broad range of input/output voltages and converter switching frequencies. Follow the procedures below for optimal compensation.

In the following descriptions, Bode plots are used to graphically describe the loop response of the converters over frequency. The Bode plot shows loop gain and phase vs. frequency. A single pole results in a -20dB per decade slope and a -90° phase shift, and a single zero results in a +20dB per decade slope and a +90° phase shift. The stability of the system can be determined by the phase margin (how far from 0° the loop phase is when the response drops to 0dB) and gain margin (how far below 0dB the gain is when the phase reaches 0°). The system is stable for phase margins >30°, and a phase margin of 45° is preferred. The gain margin should be at least 10dB.

Main Converter

The main converter uses current mode to regulate the output voltage by forcing the required current through the inductor. Since the P-channel MOSFET operates with constant drain-source on-resistance (R_{DSP}), the voltage across the MOSFET is proportional to the inductor current. The converter current-sense amplifier measures the "on" MOSFET drain-source voltage to determine the inductor current for regulation. The gain through the current-sense amplifier (measured across the MOSFET) is A_{VCSM} = 9.3V/V. The voltage-divider attenuates the loop gain by $A_{VDV} = V_{REF} / V_{OUT}$, and the gain DC voltage of the error amplifier is A_{VEA} = 2000V/V. The controller forces the peak inductor current (I_L) such that:

$$I_L\ R_{DSP}\ A_{VCSM} = V_{OUT}\ A_{VDV}\ A_{VEA}$$

or

$$I_L = V_{OUT}\ A_{VDV}\ A_{VEA} / (A_{VCSM}\ R_{DSP})$$

Digital Camera Step-Down Power Supply

and the output voltage is I_{OUT} R_{LOAD}, which is equal to I_L R_{LOAD}. Thus, the total DC loop gain is:

$$A_{VDC} = R_{LOAD}\, A_{VDV}\, A_{VEA} / (A_{VCSM}\, R_{DSP})$$

or

$$A_{VDC} = 215\, V_{REF}\, R_{LOAD} / (V_{OUT}\, R_{DS(ON)})$$

Because of the current-mode control, there is a single pole in the loop response due to the output capacitor. This pole is at the frequency (in Hz):

$$P_O = 1 / (2\pi\, R_{LOAD}\, C_{OUT})$$

Note that as the load resistance increases, the pole moves to a lower frequency. However, the DC loop gain increases by the same amount since they are both dependent on R_{LOAD}. Thus, the crossover frequency (frequency at which the loop gain drops to 0dB), which is the product of the pole and the gain, remains at the same frequency.

The compensation network creates a pole and zero at the frequencies (in Hz):

$$P_C = G_{EA} / (4000\pi\, C_C) = 1 / (4x10^7\, \pi\, C_C)$$

and

$$Z_C = 1 / (2\pi\, R_C\, C_C)$$

and the ESR of the output filter capacitor causes a zero in the loop response at the frequency (in Hz):

$$Z_O = 1 / (2\pi\, C_{OUT}\, ESR)$$

The DC gain and the poles and zeros are shown in the Bode plot of Figure 6.

To achieve a stable circuit with the Bode plot of Figure 6, use the following procedure:

1) Determine the desired crossover frequency, either 1/3 of the zero due to the output capacitor ESR:

$$f_C = Z_O / 3 = \frac{1}{6\pi C_{OUT} ESR}$$

or 1/5 of the switching frequency:

$$f_C = \frac{f_{SW}}{5}$$

whichever is lower.

2) Determine the pole frequency due to the output capacitor and the load resistor:

$$P_O = \frac{1}{2\pi R_{LOAD(MIN)} C_{OUT}}$$

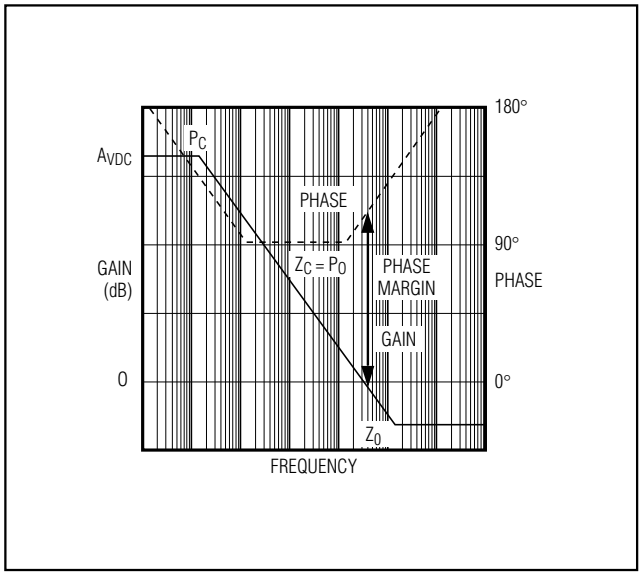

Figure 6. Current-Mode Step-Down Converter Bode Plot

or

$$P_O = \frac{I_{LOAD(MAX)}}{2\pi V_{OUT} C_{OUT}}$$

3) Determine the compensation resistor required to set the desired crossover frequency:

$$R_C = \frac{20M\Omega f_C}{A_{VDC} P_O}$$

or, by simplifying and using the typical V_{REF} = 1.25V:

$$R_C = 468k\Omega/V\ V_{OUT}\, C_{OUT}\, R_{DSP}\, f_C$$

4) Determine the compensation capacitor to set the proper error-amplifier pole and zero determined from the above equations:

$$C_C = \frac{1}{2\pi R_C P_O}$$

Core Converter

Compensating the core converter is similar to the compensation of the main converter described above. The only difference is that the current is measured internally, and the gain (transresistance) of the current-sense amplifier is R_{CSC} = 1.0V/A. The DC loop gain is:

$$A_{VDC} = 2000\, V_{REF}\, R_{LOAD} / V_{OUT}$$

To achieve a stable circuit for the core converter, use the following procedure:

1) Determine the desired crossover frequency, either 1/3 of the zero due to the output capacitor ESR:

$$f_C = \frac{Z_O}{3} = \frac{1}{6\pi C_{OUT} ESR}$$

or 1/5 of the switching frequency:

$$f_C = \frac{f_{SW}}{5}$$

whichever is lower.

2) Determine the pole frequency due to the output capacitor and the load resistor:

$$P_O = \frac{1}{2\pi R_{LOAD(MIN)} C_{OUT}}$$

or

$$P_O = \frac{I_{LOAD(MAX)}}{2\pi V_{OUT} C_{OUT}}$$

3) Determine the compensation resistor required to set the desired crossover frequency:

$$R_C = \frac{20M\Omega f_C}{A_{VDC} P_O}$$

or, by simplifying and using the typical V_{REF} = 1.25V:

$$R_C = 50k\Omega/V\ V_{OUT}\ C_{OUT}\ f_C$$

4) Determine the compensation capacitor to set the proper error-amplifier pole and zero determined from the above equations:

$$C_C = \frac{1}{2\pi R_C P_O}$$

Auxiliary Controllers

The auxiliary controllers use voltage mode to regulate their output voltages. The following explains how to compensate the control system for optimal performance. The compensation differs depending on whether the inductor current is continuous or discontinuous.

Discontinuous Inductor Current

For discontinuous inductor current, the PWM controller has a single pole. The pole frequency and DC gain of the PWM controller are dependent on the operating duty cycle, which is:

$$D = (2\ L\ f_{OSC} / R_E)^{1/2}$$

where R_E is the equivalent load resistance, or:

$$R_E = V_{IN}2\ \ R_{LOAD} / (V_{OUT} (V_{OUT} - V_{IN}))$$

The frequency of single pole due to the PWM converter is:

$$P_O = (2\ V_{OUT} - V_{IN}) / (2\pi\ (V_{OUT} - V_{IN})\ R_{LOAD}\ C_{OUT})$$

and the DC gain of the PWM controller is:

$$A_{VO} = 2\ V_{OUT}\ (V_{OUT} - V_{IN})\ R_{LOAD} / ((2\ V_{OUT} - V_{IN})\ D)$$

Note that, as in the current-mode, step-down cases above, as R_{LOAD} is increased, the pole frequency decreases and the DC gain increases proportionally. Since the crossover frequency is the product of the pole frequency and the DC gain, it remains independent of the load.

As in the cases of the main and core converters, the gain through the voltage-divider is $A_{VDV} = V_{REF} / V_{OUT}$, and the DC gain of the error amplifier is A_{VEA} = 2000V/V. Thus, the DC loop gain is $A_{VDC} = A_{VDV}\ A_{VEA}\ A_{VO}$.

The compensation resistor-capacitor pair at COMP cause a pole and zero at frequencies (in Hz):

$$P_C = G_{EA} / (4000\pi\ C_C) = 1 / (4x10^7\ \pi\ C_C)$$

$$Z_C = 1 / (2\pi\ R_C\ C_C)$$

and the ESR of the output filter capacitor causes a zero in the loop response at the frequency (in Hz): $Z_O = 1 / (2\pi\ C_{OUT}\ ESR)$.

The DC gain and the poles and zeros are shown in the Bode plot of Figure 7. To achieve a stable circuit with the Bode plot of Figure 7, follow the procedure below:

1) Choose the R_C that is equivalent to the inverse of the transconductance of the error amplifier, $1 / R_C = G_{EA}$ = 100µs, or R_C = 10kΩ. This sets the high-frequency voltage gain of the error amplifier to 0dB.

2) Determine the maximum output pole frequency:

$$P_{O(MAX)} = \frac{2V_{OUT} - V_{IN}}{2\pi(V_{OUT} - V_{IN}) R_{LOAD(MIN)} C_{OUT}}$$

where $R_{LOAD(MIN)} = V_{OUT} / I_{OUT(MAX)}$.

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3) Place the compensation zero at the same frequency as the maximum output pole frequency (in Hz):

$$Z_C = \frac{1}{2\pi R_C C_C} = \frac{2V_{OUT} - V_{IN}}{2\pi (V_{OUT} - V_{IN}) R_{LOAD(MIN)} C_{OUT}}$$

Solving for CC:

$$C_C = C_{OUT} V_{OUT} \left[\frac{V_{OUT} - V_{IN}}{R_C I_{OUT(MAX)} (2V_{OUT} - V_{IN})} \right]$$

Use values of C_C <10nF. If the above calculation determines that the capacitor should be >10nF, use C_C = 10nF, skip step 4, and go to step 5.

4) Determine the crossover frequency (in Hz):

$$f_C = \frac{V_{REF}}{\pi D C_{OUT}}$$

and to maintain at least 10dB gain margin, make sure that the crossover frequency is ≤1/3 of the ESR zero frequency, or $3f_C \le Z_O$, or $ESR \le D / 6 V_{REF}$.

If this is not the case, go to step 5 to reduce the error-amplifier high-frequency gain to decrease the crossover frequency.

5) The high-frequency gain may be reduced, thus reducing the crossover frequency, as long as the zero due to the compensation network remains at or below the crossover frequency. In this case:

$$ESR \le \frac{D}{G_{EA} R_C 6 V_{REF}}$$

and

$$f_C = \frac{G_{EA} R_C V_{REF}}{\pi D C_{OUT}} \ge \frac{1}{2\pi R_C C_C}$$

Choose C_{OUT}, R_C, and C_C to satisfy both equations simultaneously.

Continuous Inductor Current

For continuous inductor current, there are two conditions that change, requiring different compensation. The response of the control loop includes a right-half-plane zero and a complex pole pair due to the inductor and output capacitor. For stable operation, the controller-loop gain must drop below unity (0dB) at a much lower frequency than the right-half-plane zero frequency. The zero arising from the ESR of the output capacitor is typically used to compensate the control circuit by increasing the phase near the crossover frequency, increasing the phase margin. If a low-value, low-ESR output capacitor (such as a ceramic capacitor) is used, the ESR-related zero occurs at too high a frequency and does not increase the phase margin. In this case, use a lower value inductor so that it operates with discontinuous current (see the *Discontinuous Inductor Current* section).

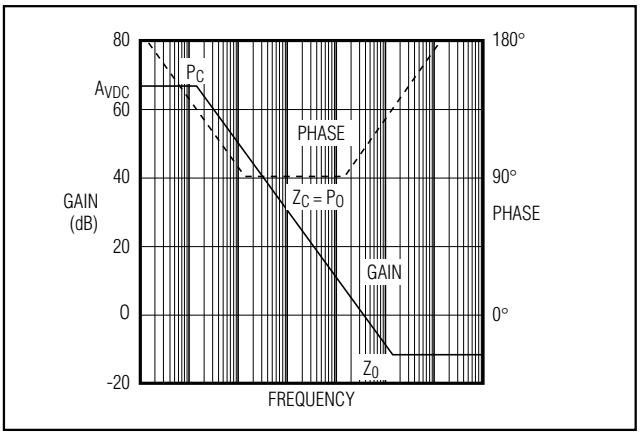

Figure 7. Discontinuous-Current, Voltage-Mode, Step-Up Controller Bode Plot

For continuous inductor current, the gain of the voltage divider is $A_{VDV} = V_{REF} / V_{OUT}$, and the DC gain of the error amplifier is A_{VEA} = 2000. The gain through the PWM controller in continuous current is:

$$A_{VO} = \frac{V_{OUT}^2}{V_{IN} V_{REF}}$$

Thus, the total DC loop gain is: $A_{VDC} = 2000 V_{OUT} / V_{IN}$.

The complex pole pair due to the inductor and output capacitor occurs at the frequency (in Hz):

$$P_O = \frac{V_{OUT}}{2\pi V_{IN} \sqrt{LC_{OUT}}}$$

The pole and zero due to the compensation network at COMP occur at the frequencies (in Hz):

$$P_C = \frac{G_{EA}}{(4000\pi C_C)} = \frac{1}{4 \times 10^7 \pi C_C}$$

$$Z_C = \frac{1}{2\pi R_C C_C}$$

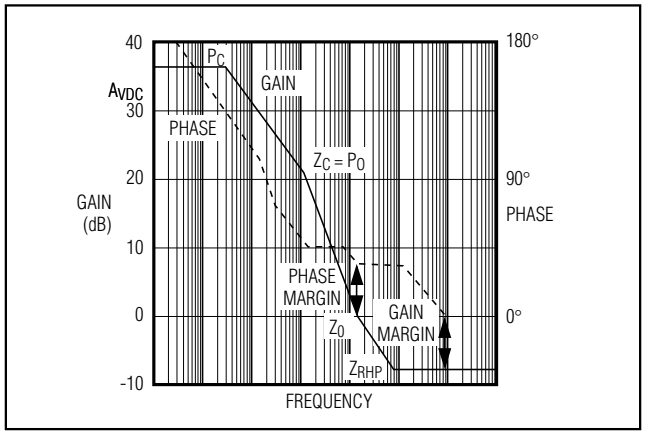

Figure 8. Continuous-Current, Voltage-Mode, Step-Up Converter Bode Plot

The frequency (in Hz) of the zero due to the ESR of the output capacitor is:

$$Z_O = \frac{1}{2\pi C_{OUT} ESR}$$

and the right-half-plane zero frequency (in Hz) is:

$$Z_{RHP} = \frac{(1-D)^2 R_{LOAD}}{2\pi L}$$

Figure 8 shows the Bode plot of the loop gain of this control circuit.

To configure the compensation network for a stable control loop, set the crossover frequency at that of the zero due to the output capacitor ESR. Use the following procedure:

1) Determine the frequency of the right-half-plane zero:

$$Z_{RHP} = \frac{(1-D)^2 R_{LOAD}}{2\pi L}$$

2) Find the DC loop gain:

$$A_{VDC} = \frac{2000 V_{OUT}}{V_{IN}}$$

3) Determine the frequency of the complex pole pair due to the inductor and output capacitor:

$$f_O = \frac{V_{OUT}}{2\pi V_{IN}\sqrt{LC_{OUT}}}$$

4) Since response is 2nd order (-40dB per decade) between the complex pole pair and the ESR zero, determine the desired amplitude at the complex pole pair to force the crossover frequency equal to the ESR zero frequency. Thus:

$$A(P_O) = (Z_O/P_O)^2 = \frac{L V_{IN}^2}{C_{OUT} ESR^2 V_{OUT}^2}$$

5) Determine the desired compensation pole. Since the response between the compensation pole and the complex pole pair is 1st order (-20dB per decade), the ratio of the frequencies is equal to the ratio of the amplitudes at those frequencies. Thus:

$$\frac{P_O}{P_C} = \frac{A_{DC}}{A(P_O)}$$

Solving this equation for C_C:

$$C_C = \frac{V_{OUT}(C_{OUT})^{3/2} ESR^2}{20M\Omega\, V_{IN}\, (L)^{1/2}}$$

6) Determine R_C for the compensation zero frequency as equal to the complex pole-pair frequency: $Z_C = P_O$.

Solving for R_C:

$$R_C = \frac{V_{IN}\sqrt{LC_{OUT}}}{V_{OUT} C_C}$$

Applications Information

Using the MAX1801 with the MAX1802 Step-Down Master

The MAX1801 is a slave DC-DC controller that can be used with the MAX1802 to generate additional output voltages. The MAX1801 does not generate its own reference or oscillator. Instead it uses the reference and oscillator from the MAX1802 step-down master converter controller (Figure 1). MAX1801 controller operation and design is similar to that of the MAX1802 auxiliary controllers. For more details, refer to the MAX1801 data sheet.

Using an Auxiliary Controller in an SEPIC Configuration

Where the battery voltage may be above or below the required output voltage, neither a step-up nor a step-down converter is suitable; instead, use a step-up/step-down converter. One type of step-up/step-down

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converter is the SEPIC, shown in Figure 9. Inductors L1 and L2 can be separate inductors or can be wound on a single core and coupled like a transformer. Typically, using a coupled inductor will improve efficiency since some power is transferred through the coupling, so less power passes through the coupling capacitor (C2). Likewise, C2 should have low ESR to improve efficiency. The ripple current rating must be greater than the larger of the input and output currents. The MOSFET (Q1) drain-source voltage rating and the rectifier (D1) reverse-voltage rating must exceed the sum of the input and output voltages. Other types of step-up/step-down circuits are a flyback converter and a step-up converter followed by a linear regulator.

Using an Auxiliary Controller for a Multi-Output Flyback Circuit

Some applications require multiple voltages from a single converter that features a flyback transformer. Figure 10 shows a MAX1802 auxiliary controller in a two-output flyback configuration. The controller drives an external MOSFET that switches the transformer primary, and the two secondaries generate the outputs. Only a single positive output voltage can be regulated using the feedback resistive voltage-divider, so the other voltages are set by the turns ratio of the transformer secondaries. The regulation of the other secondary voltages degrades due to transformer leakage inductance and winding resistance. Voltage regulation is best when the load current is limited to a small range. Consult the transformer manufacturer for the proper design for a given application.

Using a Charge Pump for Negative Output Voltages

Negative output voltages can be produced without a transformer using a charge-pump circuit with an auxiliary controller as shown in Figure 11. When MOSFET Q1 turns off, the voltage at its drain rises to supply current to V_{OUT+}. At the same time, C1 charges to the voltage at V_{OUT+} through D1. When the MOSFET turns on, C1 discharges through D3, thereby charging C3 to V_{OUT-} minus the drop across D3 to create roughly the same voltage as V_{OUT+} at V_{OUT-} but with inverted polarity. If different magnitudes are required for the positive and negative voltages, a linear regulator can be used at one of the outputs to achieve the desired voltage.

Designing a PC Board

A good PC board layout is important to achieve optimal performance from the MAX1802. Good design reduces excessive conducted and/or radiated noise, both of which are undesirable.

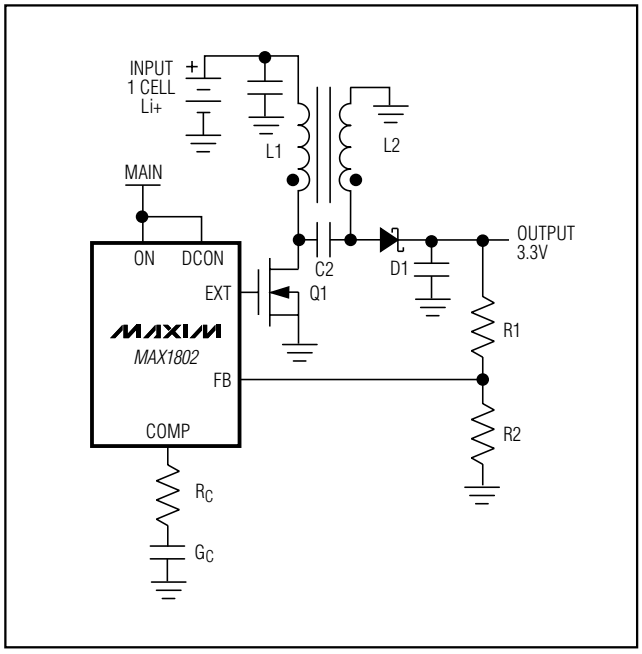


Figure 9. Auxiliary Controller, SEPIC Configuration

Conductors carrying discontinuous currents should be kept as short as possible. Conductors carrying high currents should be made as wide as possible. A separate low-noise ground plane containing the reference and signal grounds should only connect to the power-ground plane at one point to minimize the effects of power-ground currents.

Keep the voltage feedback network very close to the IC, preferably within 0.2in (5mm) of the FB_ pin. Nodes with high dv/dt (switching nodes) should be kept as small as possible and should stay away from high-impedance nodes such as FB_ and COMP_.

Refer to the MAX1802EVKIT evaluation kit manual for a full PC board example.

Chip Information

TRANSISTOR COUNT: 7740

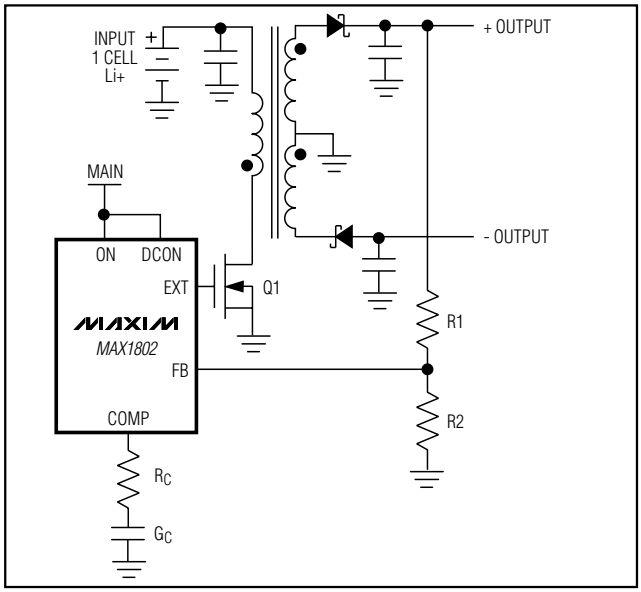


Figure 10. Auxiliary Controller, Flyback Configuration

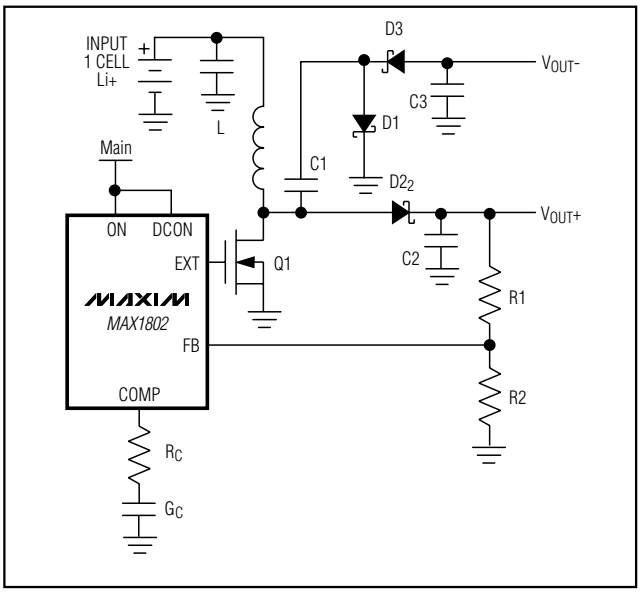
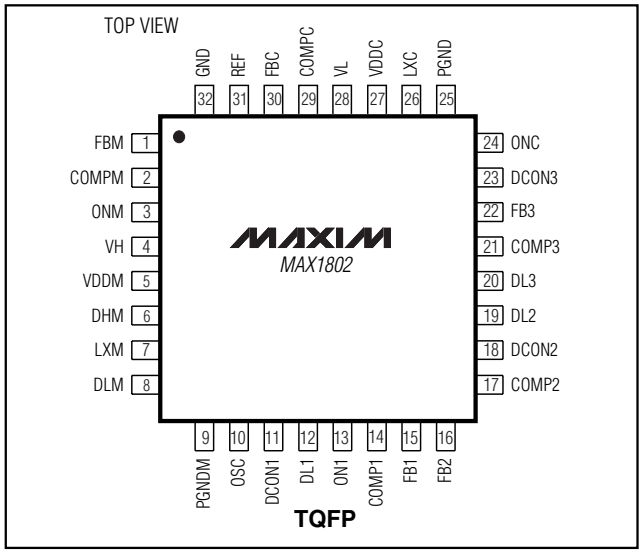


Figure 11. Auxiliary Controller, Charge-Pump Configuration

Pin Configuration



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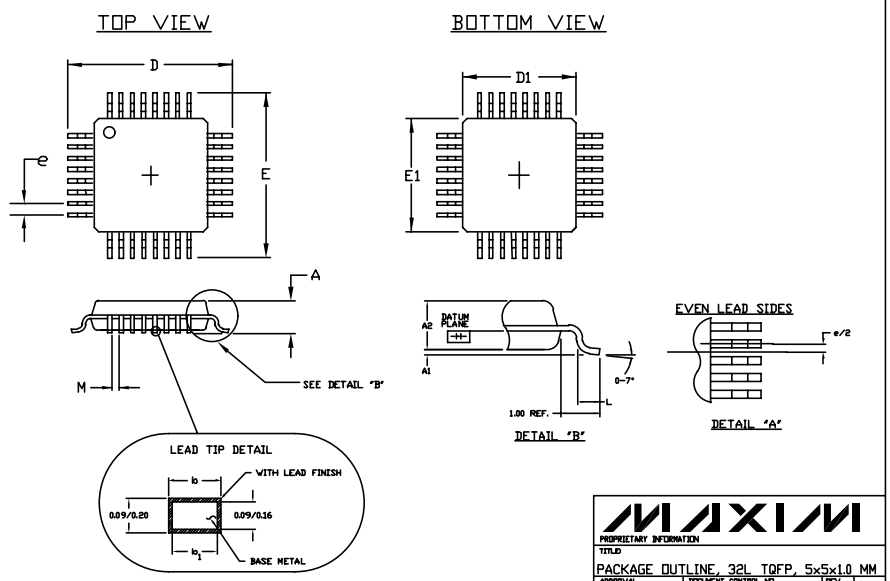
Package Information

32L TQFP, 5x5x01.0.EPS



PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0110	A	1/2

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

	JEDEC VARIATIONS	
	DIMENSIONS IN MILLIMETERS	
	AA	
	5x5x1.0 MM	
	MIN.	MAX.
A	---	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	7.00 BSC.	
D_1	5.00 BSC.	
E	7.00 BSC.	
E_1	5.00 BSC.	
L	0.45	0.75
M	0.15	---
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0 MM

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