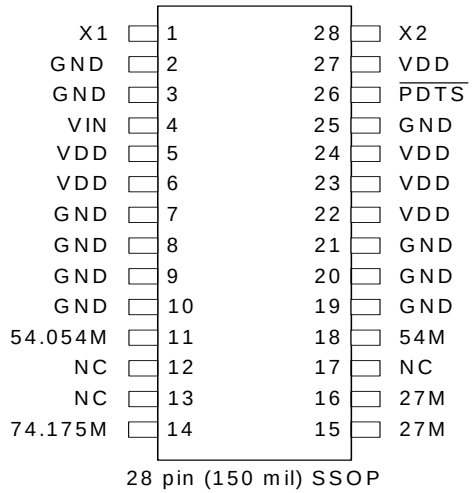
Pin Assignment



28 pin (150 mil) SSOP

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI	Input	Crystal connection. Connect to a 27 MHz fundamental mode pullable crystal.
2	GND	Power	Connect to ground.
3	GND	Power	Connect to ground.
4	VIN	Input	VCXO Voltage input. Zero to 3.3 V analog control voltage for VCXO.
5, 6, 22, 23, 24, 27	VDD	Power	Connect to +3.3 V.
7, 8, 9, 10, 19, 20, 21	GND	Power	Connect to ground.
11	54.054M	Output	54.054 MHz clock output. Weak internal pull-down when tri-state.
12, 13, 17	NC	-	No connect. Do not connect anything to these pins.
14	74.175M	Output	74.175 MHz clock output. Weak internal pull-down when tri-state.
15, 16	27M	Output	27 MHz reference clock output. Weak internal pull-down when tri-state.
18	54M	Output	54 MHz clock output. Weak internal pull-down when tri-state.
25	GND	Power	Connect to ground.
26	$\overline{\text{PDTS}}$	Input	Powers down entire chip. Tri-states CLK outputs when low. Internal pull-up.
28	X2	Input	Crystal connection. Connect to a 27 MHz fundamental mode pullable crystal.

External Components

The ICS477-05 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01µF must be connected between VDD and GND, as close to these pins as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Quartz Crystal

The ICS477-05 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The ICS477-05 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the ICS477-05 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the ICS477-05. There should be no via’s between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

See application note MAN05 for complete crystal specifications.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, CL.

To determine the value of the crystal capacitors:

1. Connect VDD of the ICS477-05 to 3.3 V. Connect pin 4 of the ICS477-05 to the second power supply. Adjust the voltage on pin 3 to 0V. Measure and record the frequency of the 27 MHz output.

2. Adjust the voltage on pin 4 to 3.3 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$Error = 10^6 x\left[\frac{(f_{3.0V} - f_{target}) + (f_{0V} - f_{target})}{f_{target}}\right] - error_{xtal}$$

Where:

f_{target} = nominal crystal frequency

$error_{xtal}$ =actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than ±25 ppm, no adjustment is needed. If the centering error is more than 25 ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be

considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact ICS for details.) If the centering error is more than 25 ppm positive, add identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

External Capacitor =

2 x (centering error)/(trim sensitivity)

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (typically less than ±25 ppm).

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pins as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS477-05. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS477-05. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Supply Current	IDD	No load		48		mA
Power Down Current	IDDPD	No load		0.5		mA
Input High Voltage	V_{IH}	$\overline{PDTS}$ pin	2			V
Input Low Voltage	V_{IL}	$\overline{PDTS}$ pin			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}	CLK output		±80		mA
Input Capacitance, inputs	C_{IN}			5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
Internal Pull-up Resistor	R_{PUP}	$\overline{PDTS}$ pin		360		kΩ
Internal Pull-down Resistor	R_{PD}	CLK outputs		510		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

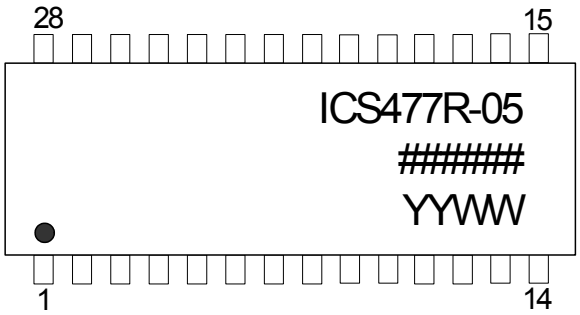
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{in}	Crystal input, Note 2		27		MHz
Crystal Pullability	F_P	0V≤ VIN ≤ 3.3 V	±100			ppm
VCXO Gain	K_0	VIN = VDD/2 ± 1 V		150		ppm/V
Output Rise Time	t_{OR}	20% to 80%, Note 1		1.2		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1.0		ns
Clock Stabilization Time after Power-up					10	ms
Cycle Jitter (short term jitter)	t_{ja}			±200		ps

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Long Term Jitter		54.054M, 54M clocks		1.0		ns
		74.175M clock		1.3		ns
		27M reference clock		300		ps
Output Enable Time		$\overline{\text{PDTS}}$ high to output locked to ±1%		250		µs
Output Disable Time		$\overline{\text{PDTS}}$ low to tri-state		20		ns

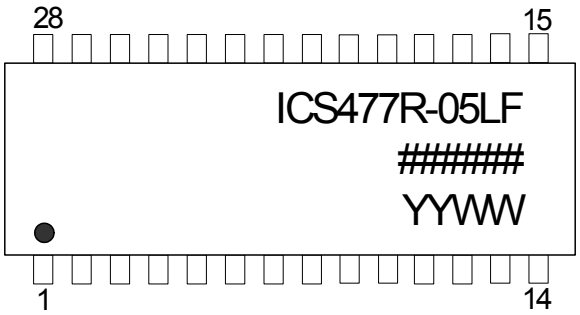
Note 1: Measured with a 15 pF load.

Note 2:With an ICS approved crystal.

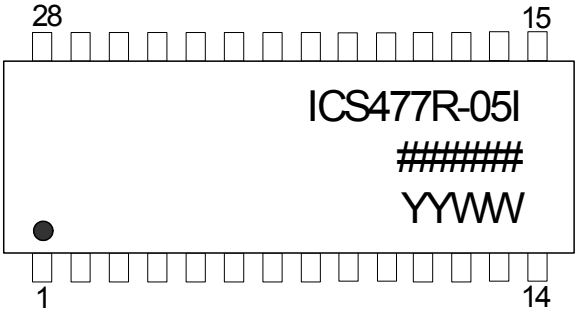
Marking Diagram



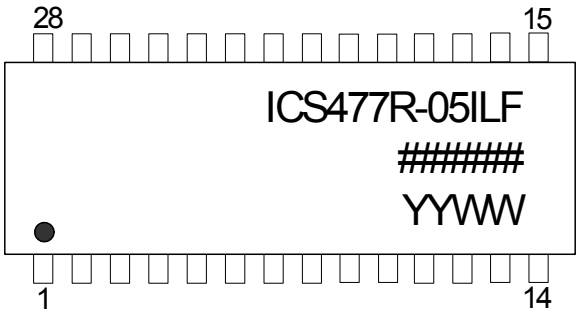
Marking Diagram (Pb free)



Marking Diagram (industrial)



Marking Diagram (Pb free, industrial)

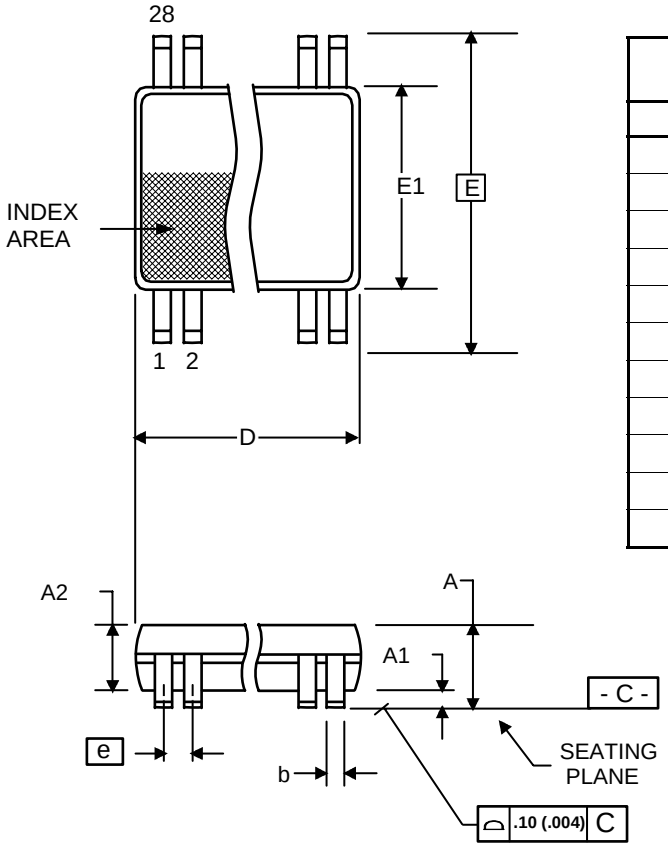


Notes:

1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week.
3. “LF” designates Pb (lead) free.
4. “I” designates industrial temperature grade.

Package Outline and Package Dimensions (28-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	0.008	0.012
C	0.18	0.25	.007	.010
D	9.80	10.00	.386	.394
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
477R-05	ICS477R-05 (top line) YYWW (3rd line)	Tubes	28-pin SSOP	0 to +70° C
477R-05T		Tape and Reel	28-pin SSOP	0 to +70° C
477R-05I	ICS477R-05I (top line) YYWW (3rd line)	Tubes	28-pin SSOP	-40 to +85° C
477R-05IT		Tape and Reel	28-pin SSOP	-40 to +85° C
477R-05LF	ICS477R-05LF (top line) YYWW (3rd line)	Tubes	28-pin SSOP	0 to +70° C
477R-05LFT		Tape and Reel	28-pin SSOP	0 to +70° C
477R-05ILF	ICS477R-05ILF (top line) YYWW (3rd line)	Tubes	28-pin SSOP	-40 to +85° C
477R-05ILFT		Tape and Reel	28-pin SSOP	-40 to +85° C

"LF" denotes Pb (lead) free package.

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