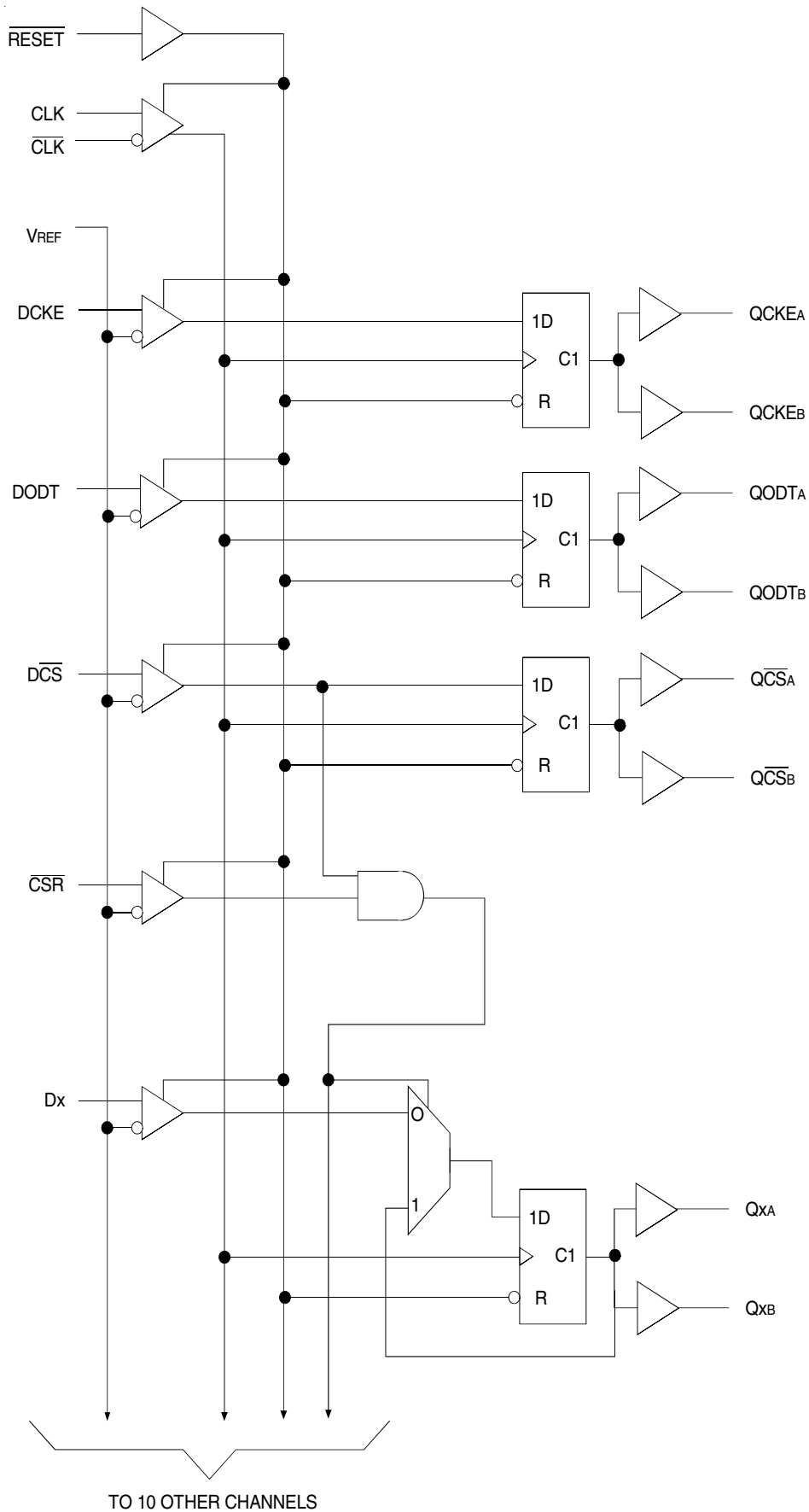


FUNCTIONAL BLOCK DIAGRAM (1:2)



TO 10 OTHER CHANNELS

PIN CONFIGURATION (TYPE A)

6	QCKEB	Q2B	Q3B	QODTB	Q5B	Q6B	C0	$\overline{\text{QCSB}}$	ZOL	Q8B	Q9B	Q10B	Q11B	Q12B	Q13B	Q14B
5	QCKEA	Q2A	Q3A	QODTA	Q5A	Q6A	C1	$\overline{\text{QCSA}}$	ZOH	Q8A	Q9A	Q10A	Q11A	Q12A	Q13A	Q14A
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	NC	NC	NC	NC	NC	NC	$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	NC	NC	NC	NC	NC	NC	NC
1	DCKE	D2	D3	DODT	D5	D6	NC	CLK	$\overline{\text{CLK}}$	D8	D9	D10	D11	D12	D13	D14
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

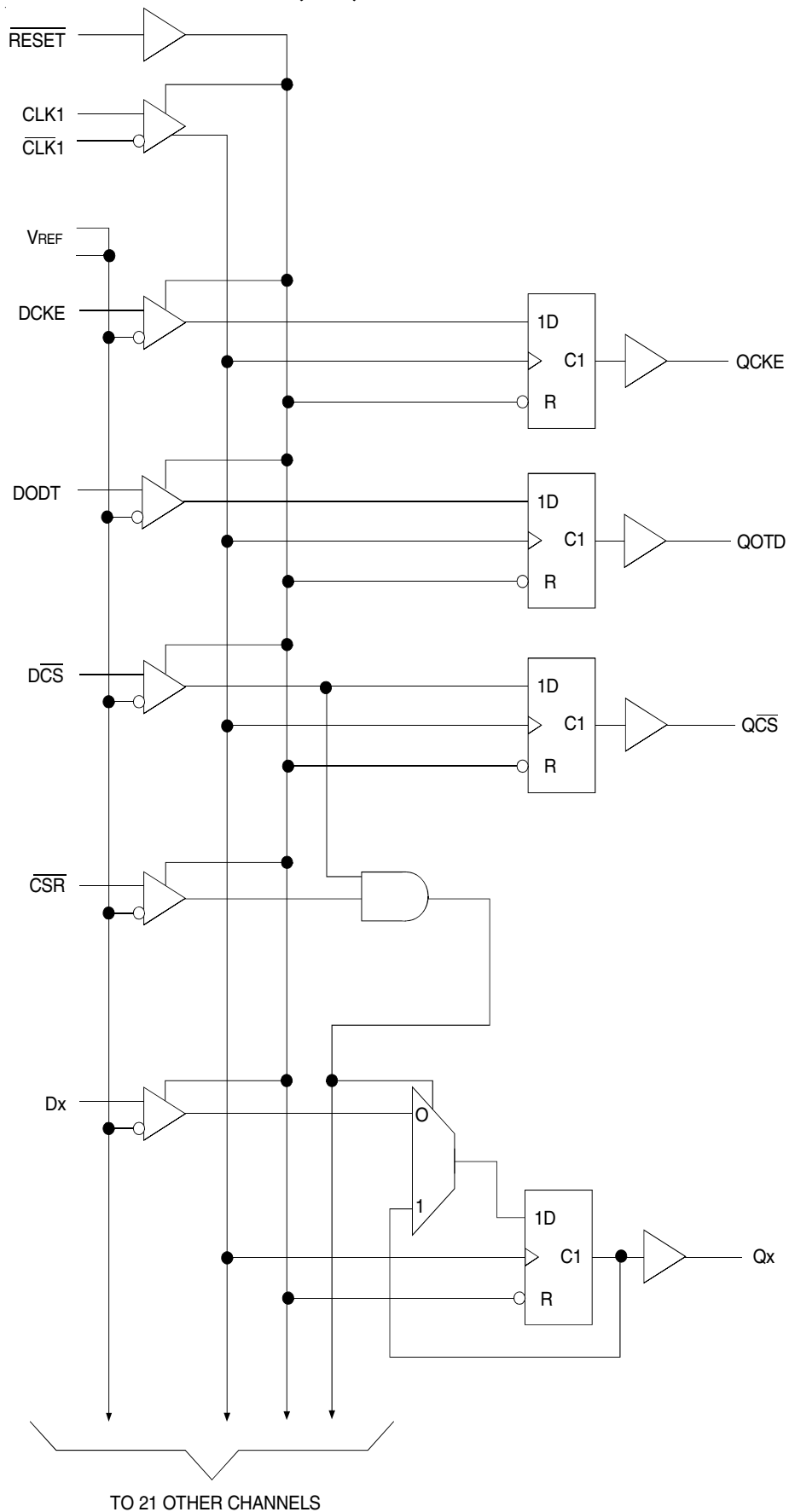
96-PIN LFBGA
1:2 REGISTER (TYPE A, FRONTSIDE)
TOP VIEW

PIN CONFIGURATION (TYPE B)

6	Q1B	Q2B	Q3B	Q4B	Q5B	Q6B	C0	$\overline{\text{QCSB}}$	ZOL	Q8B	Q9B	Q10B	QODTB	Q12B	Q13B	QCKEB
5	Q1A	Q2A	Q3A	Q4A	Q5A	Q6A	C1	$\overline{\text{QCSA}}$	ZOH	Q8A	Q9A	Q10A	QODTA	Q12A	Q13A	QCKEA
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	NC	NC	NC	NC	NC	NC	$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	NC	NC	NC	NC	NC	NC	NC
1	D1	D2	D3	D4	D5	D6	NC	CLK	$\overline{\text{CLK}}$	D8	D9	D10	DODT	D12	D13	DCKE
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

96-PIN LFBGA
1:2 REGISTER (TYPE B, BACKSIDE)
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM (1:1)



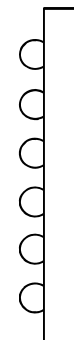
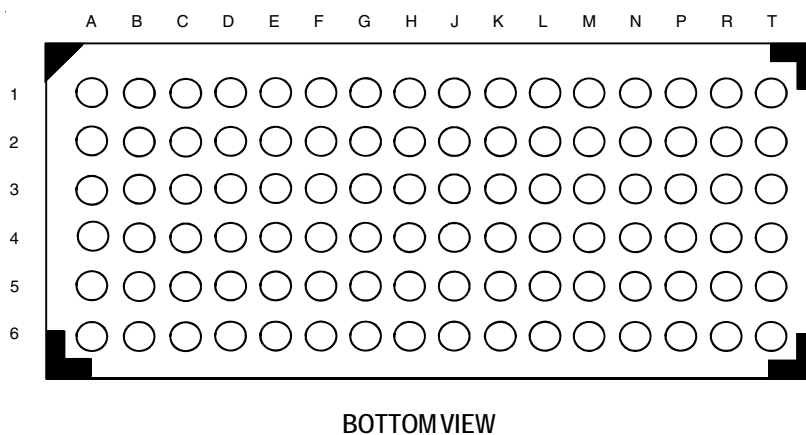
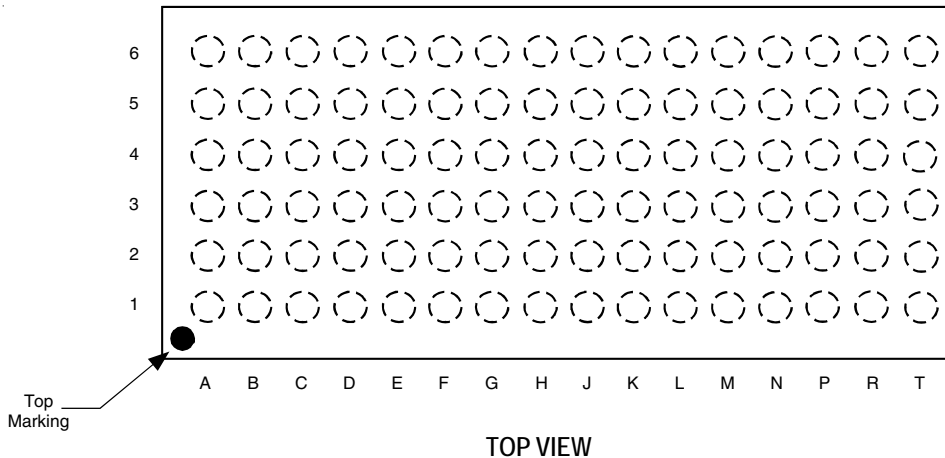
PIN CONFIGURATION

6	NC	Q15	Q16	NC	Q17	Q18	C0	NC	ZoL	Q19	Q20	Q21	Q22	Q23	Q24	Q25
5	QCKE	Q2	Q3	QODT	Q5	Q6	C1	$\overline{\text{QCS}}$	ZoH	Q8	Q9	Q10	Q11	Q12	Q13	Q14
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	NC	D15	D16	NC	D17	D18	$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	D19	D20	D21	D22	D23	D24	D25
1	DCKE	D2	D3	DODT	D5	D6	NC	CLK	$\overline{\text{CLK}}$	D8	D9	D10	D11	D12	D13	D14
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

*Rows 3 and 4 are reserved for VDD and GND.

96-PIN LFBGA 1:1 REGISTER TOP VIEW

96 BALL LFBGA PACKAGE ATTRIBUTES



FUNCTION TABLE (EACH FLIP-FLOP) (1)

Inputs					Qx Outputs	QCSx Output	QODTx, QCKEx Outputs
RESE \bar{T}	D \bar{C} S	C \bar{S} R	CLK	CL \bar{K}			
H	L	L	↑	↓	L	L	L
H	L	L	↑	↓	H	L	H
H	L	L	L or H	L or H	X	Q ₀ ⁽²⁾	Q ₀ ⁽²⁾
H	L	H	↑	↓	L	L	L
H	L	H	↑	↓	H	L	H
H	L	H	L or H	L or H	X	Q ₀ ⁽²⁾	Q ₀ ⁽²⁾
H	H	L	↑	↓	L	L	H
H	H	L	↑	↓	H	H	H
H	H	L	L or H	L or H	X	Q ₀ ⁽²⁾	Q ₀ ⁽²⁾
H	H	H	↑	↓	L	Q ₀ ⁽²⁾	H
H	H	H	↑	↓	H	Q ₀ ⁽²⁾	H
H	H	H	L or H	L or H	X	Q ₀ ⁽²⁾	Q ₀ ⁽²⁾
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW to HIGH
↓ = HIGH to LOW
- Output level before the indicated steady-state conditions were established.

MODE SELECT

C ₀	C ₁	Device Mode
0	0	1:1 25-bit to 25-bit
0	1	1:2 14-bit to 28-bit, Front (Type A)
1	0	Reserved
1	1	1:2 14-bit to 28-bit, Back (Type B)

OUTPUT CONTROL (SSTU32864G)

Z _{OH}	Z _{OL}	Output Slew Rate
0	0	Standard
0	1	Highest
1	0	Low
1	1	High

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V _{DD}	Supply Voltage Range	-0.5 to 2.5	V
V _I ^(2,3)	Input Voltage Range	-0.5 to 2.5	V
V _O ^(2,3)	Output Voltage Range	-0.5 to V _{DD} +0.5	V
I _{IK}	Input Clamp Current	±50	mA
	V _I < 0 V _I > V _{DD}		
I _{OK}	Output Clamp Current	±50	mA
	V _O < 0 V _O > V _{DD}		
I _O	Continuous Output Current, V _O = 0 to V _{DD}	±50	mA
V _{DD}	Continuous Current through each V _{DD} or GND	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
- This value is limited to 2.5V maximum.

TERMINAL FUNCTIONS (ALL PINS)

Terminal Name	Electrical Characteristics	Description
GND	Ground Input	Ground
V _{DD}	1.8V nominal	Power Supply Voltage
V _{REF}	0.9V nominal	Input Reference Voltage
Z _{OH} ⁽¹⁾	LVC MOS	Output Slew Rate Control
Z _{OL} ⁽¹⁾	LVC MOS	Output Slew Rate Control
CLK	Differential Input	Positive Master Clock Input
$\overline{\text{CLK}}$	Differential Input	Negative Master Clock Input
C x	LVC MOS Input	Configuration Control Inputs
$\overline{\text{RESET}}$	LVC MOS Input	Asynchronous Reset Input. Resets registers and disables V _{REF} data and clock differential-input receivers.
$\overline{\text{CSR}}$, $\overline{\text{DCS}}$	SSTL_18 Input	Chip Select Inputs. Disables outputs Dx switching when both inputs are HIGH.
Dx	SSTL_18 Input	Data Input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$.
DODT	SSTL_18 Input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
DCKE	SSTL_18 Input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
Qx	1.8V CMOS	Data Outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
$\overline{\text{QCSx}}$	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
OODTx	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls
OCKEx	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ controls

NOTE:

- The signals will be left unconnected for the SSTU32864/A/C/D.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$ (1,2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
VDD	Supply Voltage		1.7	—	1.9	V
VREF	Reference Voltage		$0.49 * V_{DD}$	$0.5 * V_{DD}$	$0.51 * V_{DD}$	V
VTT	Termination Voltage		$V_{REF} - 40\text{mV}$	V_{REF}	$V_{REF} + 40\text{mV}$	V
VI	Input Voltage		0	—	VDD	V
VIH	AC High-Level Input Voltage	Data Inputs	$V_{REF} + 250\text{mV}$	—	—	V
VIL	AC Low-Level Input Voltage	Data Inputs	—	—	$V_{REF} - 250\text{mV}$	V
VIH	DC High-Level Input Voltage	Data Inputs	$V_{REF} + 125\text{mV}$	—	—	V
VIL	DC Low-Level Input Voltage	Data Inputs	—	—	$V_{REF} - 125\text{mV}$	V
VIH	High-Level Input Voltage	$\overline{\text{RESET}}$, Cx	$0.65 * V_{DD}$	—	—	V
VIL	Low-Level Input Voltage	$\overline{\text{RESET}}$, Cx	—	—	$0.35 * V_{DD}$	V
VICR	Common Mode Input Voltage	CLK, $\overline{\text{CLK}}$	0.675	—	1.125	V
VID	Differential Input Voltage	CLK, $\overline{\text{CLK}}$	600	—	—	mV
IOH	High-Level Output Current		—	—	-8	mA
IOL	Low-Level Output Current		—	—	8	
TA	Operating Free-Air Temperature		0	—	70	$^\circ\text{C}$

NOTES:

1. The $\overline{\text{RESET}}$ and Cx inputs of the device must be held at valid levels (not floating) to ensure proper device operation.
2. The differential inputs must not be floating unless $\overline{\text{RESET}}$ is LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VOH		$V_{DD} = 1.7\text{V}$ to 1.9V , $I_{OH} = -6\text{mA}$	1.2	—	—	V
VOL		$V_{DD} = 1.7\text{V}$ to 1.9V , $I_{OL} = 6\text{mA}$	—	—	0.5	V
II	All Inputs	$V_i = V_{DD}$ or GND	-5	—	5	μA
IDD	Static Standby	$I_O = 0$, $V_{DD} = 1.9\text{V}$, $\overline{\text{RESET}} = \text{GND}$	—	—	100	μA
	Static Operating	$I_O = 0$, $V_{DD} = 1.9\text{V}$, $\overline{\text{RESET}} = V_{DD}$, $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$	—	—	40	mA
IDDD	Dynamic Operating (Clock Only)	$I_O = 0$, $V_{DD} = 1.8\text{V}$, $\overline{\text{RESET}} = V_{DD}$, $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$, CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle.	—	—	—	$\mu\text{A}/\text{Clock MHz}$
	Dynamic Operating (Per Each Data Input)	$I_O = 0$, $V_{DD} = 1.8\text{V}$, $\overline{\text{RESET}} = V_{DD}$, $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$, CLK and $\overline{\text{CLK}}$ Switching at 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.				$\mu\text{A}/\text{Clock MHz/Data Input}$
CI	Data Inputs	$V_i = V_{REF} \pm 250\text{mV}$	2.5	—	3.5	pF
	CLK and $\overline{\text{CLK}}$	$V_{ICR} = 0.9\text{V}$, $V_{ID} = 600\text{mV}$	2	—	3	
	$\overline{\text{RESET}}$	$V_i = V_{DD}$ or GND	2	—	4	

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

Symbol	Parameter	V _{DD} = 1.8V ± 0.1V		Unit	
		Min.	Max.		
f _{clock} ⁽¹⁾	Clock Frequency	—	340	MHz	
t _w	Pulse Duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW	1	—	ns	
t _{ACT} ⁽²⁾	Differential Inputs Active Time	—	10	ns	
t _{INACT} ⁽³⁾	Differential Inputs Inactive Time	—	15	ns	
t _{SU}	Setup Time	DCS before CLK \uparrow , CLK \downarrow , $\overline{\text{CSR}}$ HIGH	0.7	—	ns
		DCS before CLK \uparrow , CLK \downarrow , $\overline{\text{CSR}}$ LOW	0.5	—	
		DODT, $\overline{\text{CSR}}$, Data, and DCKE before CLK \uparrow , CLK \downarrow	0.5	—	
t _H	Hold Time	Data, DCS, $\overline{\text{CSR}}$, DCKE, and DODT after CLK \uparrow , CLK \downarrow	0.5	—	ns

NOTES:

- 270MHz max clock frequency for parts assembled and tested prior to WW37.
- Data and V_{REF} inputs must be low a minimum time of t_{ACT} max, after $\overline{\text{RESET}}$ is taken HIGH.
- Data, V_{REF}, and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} max, after $\overline{\text{RESET}}$ is taken LOW.

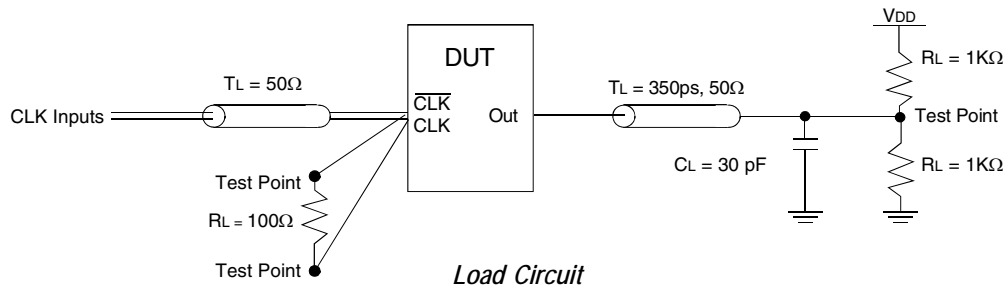
SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED) ⁽¹⁾

Symbol	Parameter	V _{DD} = 1.8V ± 0.1V		Unit
		Min	Max.	
f _{MAX}		340	—	MHz
t _{PDM} ⁽²⁾	CLK and $\overline{\text{CLK}}$ to Q	1.41	2.15	ns
t _{PDMSS} ^(2,3)	CLK and $\overline{\text{CLK}}$ to Q (simultaneous switching)	—	2.35	ns
t _{RPHL}	$\overline{\text{RESET}}$ to Q	—	3	ns
dV/dt _r	Output slew rate from 20% to 80%	1	4	V/ns
dV/dt _f	Output slew rate from 20% to 80%	1	4	V/ns
dV/dt _Δ ⁽⁴⁾	Output slew rate from 20% to 80%	—	1	V/ns

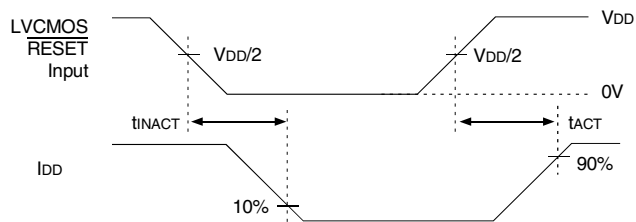
NOTES:

- See TEST CIRCUITS AND WAVEFORMS.
- Includes 350ps of test load transmission line delay.
- This parameter is not production tested.
- Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

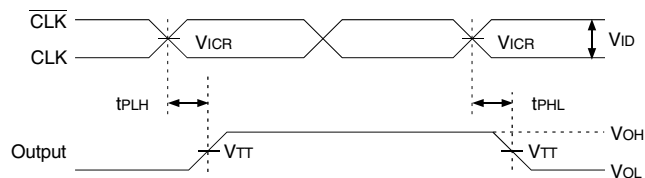
TEST CIRCUITS AND WAVEFORMS ($V_{DD} = 1.8V \pm 0.1V$)



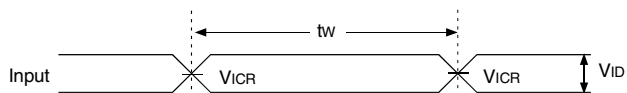
Load Circuit



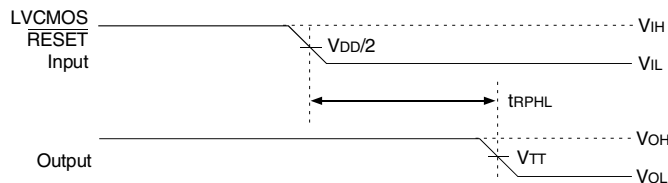
Voltage and Current Waveforms
Inputs Active and Inactive Times



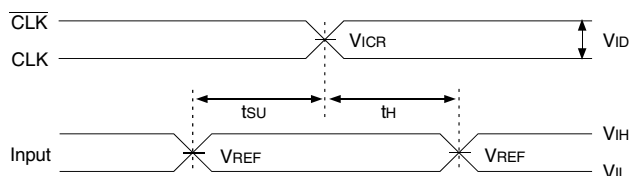
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times

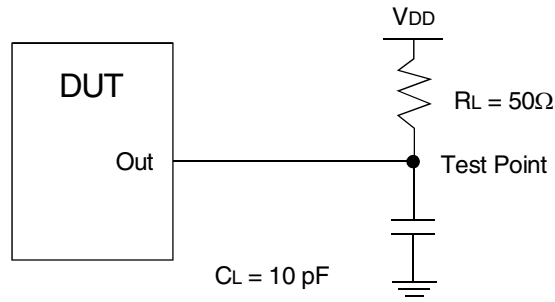


Voltage Waveforms - Setup and Hold Times

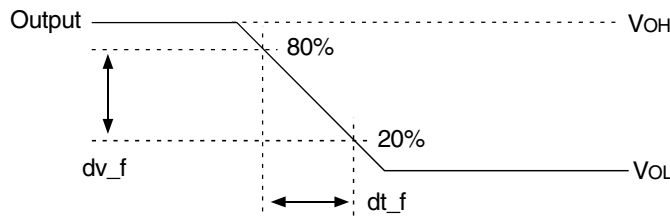
NOTES:

1. CL includes probe and jig capacitance.
2. IDD tested with clock and data inputs held at VDD or GND, and Io = 0mA
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. VTT = VREF = VDD/2
6. VIH = VREF + 250mV (AC voltage levels) for differential inputs. VIH = VDD for LVC MOS input.
7. VIL = VREF - 250mV (AC voltage levels) for differential inputs. VIL = GND for LVC MOS input.
8. VID = 600mV.
9. tPLH and tPHL are the same as tPDM.

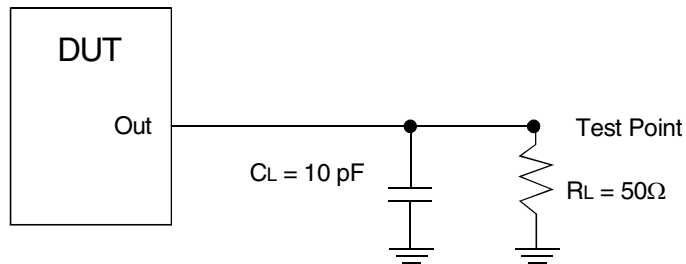
TEST CIRCUITS AND WAVEFORMS ($V_{DD} = 1.8V \pm 0.1V$)



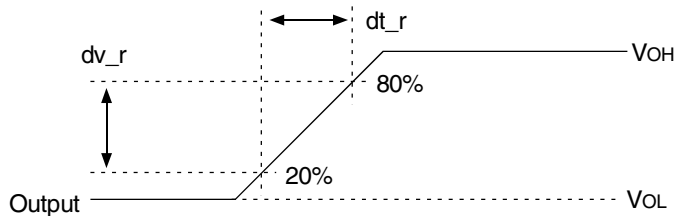
Load Circuit: High-to-Low Slew-Rate Adjustment



Voltage Waveforms: High-to-Low Slew-Rate Adjustment



Load Circuit: Low-to-High Slew-Rate Adjustment

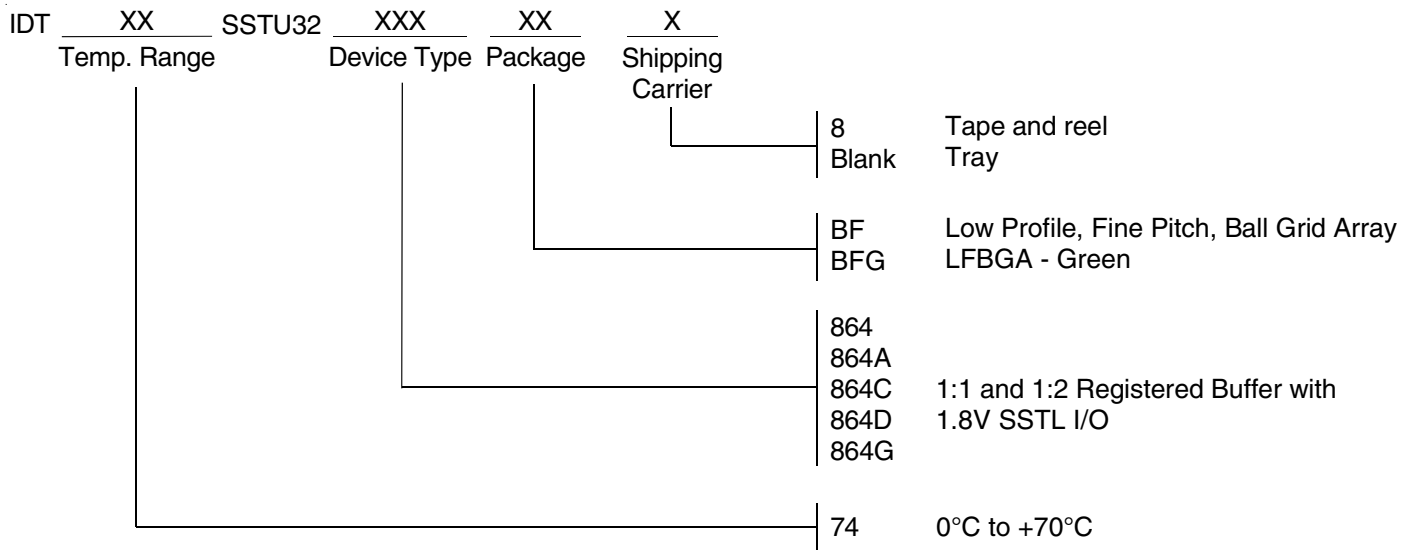


Voltage Waveforms: Low-to-High Slew-Rate Adjustment

NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{MHz}$, $Z_o = 50\Omega$, input slew rate = $1 \text{ V/ns} \pm 20\%$ (unless otherwise specified).

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