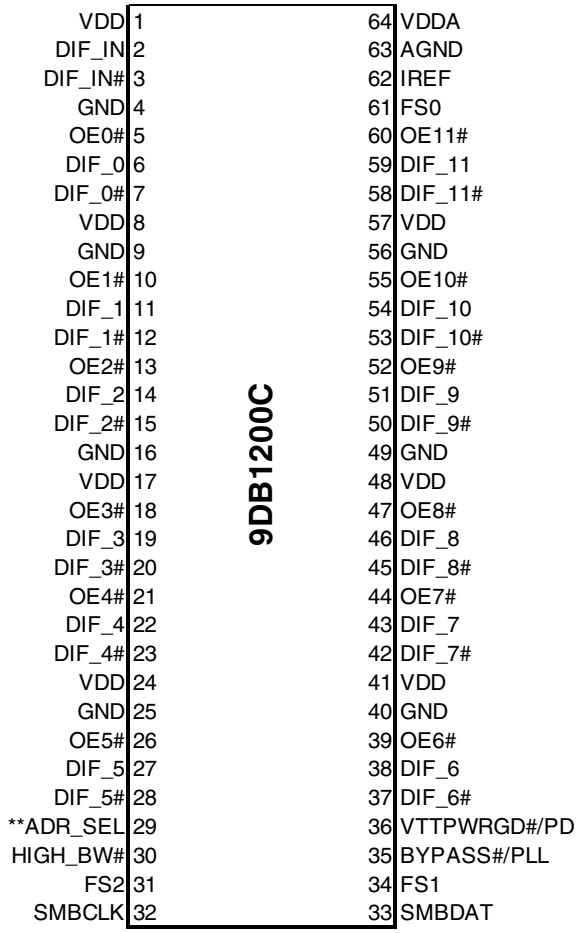
Pin Configuration



64-TSSOP

** Indicates 120K ohm Pulldown

Frequency Select Table

FS_L2 B0b2	FS_L1 B0b1	FS_L0 B0b0	Input MHz	DIF_x; MHz
0	0	0	266.66	266.66
0	0	1	133.33	133.33
0	1	0	200.00	200.00
0	1	1	166.66	166.66
1	0	0	333.33	333.33
1	0	1	100.00	100.00
1	1	0	400.00	400.00
1	1	1	Hi-Z	Hi-Z

1. FS_L(2:0) are 3.3V tolerant low-threshold inputs.

Please see VIL_FS and VIH_FS specifications in the Input/Supply/Common Output Parameters Table for correct values.

SMBus Address Selection (Pin 29)

ADR_SEL	Voltage	SMBus Adr (Wr/Rd)
Low	<0.8V	DC/DD
Mid	1.2<Vin<1.8V	D6/D7
High	Vin > 2.0V	D4/D5

Power Groups

Pin Number		Description
VDD	GND	
1	4	DIF_IN/DIF_IN#
8, 17, 24, 41, 48, 57	9, 16, 25, 40, 49, 56	DIF(11:0)
N/A	63	IREF
64	63	Analog VDD & GND for PLL core

Note: Please treat pin 1 as an analog VDD.

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDD	PWR	Power supply, nominal 3.3V
2	DIF_IN	IN	0.7 V Differential TRUE input
3	DIF_IN#	IN	0.7 V Differential Complementary Input
4	GND	PWR	Ground pin.
5	OE0#	IN	Active low input for enabling DIF pair 0. 1 =disable outputs, 0 = enable outputs
6	DIF_0	OUT	0.7V differential true clock output
7	DIF_0#	OUT	0.7V differential Complementary clock output
8	VDD	PWR	Power supply, nominal 3.3V
9	GND	PWR	Ground pin.
10	OE1#	IN	Active low input for enabling DIF pair 1. 1 =disable outputs, 0 = enable outputs
11	DIF_1	OUT	0.7V differential true clock output
12	DIF_1#	OUT	0.7V differential Complementary clock output
13	OE2#	IN	Active low input for enabling DIF pair 2. 1 =disable outputs, 0 = enable outputs
14	DIF_2	OUT	0.7V differential true clock output
15	DIF_2#	OUT	0.7V differential Complementary clock output
16	GND	PWR	Ground pin.
17	VDD	PWR	Power supply, nominal 3.3V
18	OE3#	IN	Active low input for enabling DIF pair 3. 1 =disable outputs, 0 = enable outputs
19	DIF_3	OUT	0.7V differential true clock output
20	DIF_3#	OUT	0.7V differential Complementary clock output
21	OE4#	IN	Active low input for enabling DIF pair 4 1 =disable outputs, 0 = enable outputs
22	DIF_4	OUT	0.7V differential true clock output
23	DIF_4#	OUT	0.7V differential Complementary clock output
24	VDD	PWR	Power supply, nominal 3.3V
25	GND	PWR	Ground pin.
26	OE5#	IN	Active low input for enabling DIF pair 5. 1 =disable outputs, 0 = enable outputs
27	DIF_5	OUT	0.7V differential true clock output
28	DIF_5#	OUT	0.7V differential Complementary clock output
29	**ADR_SEL	IN	This tri-level input selects one of 3 SMBus addresses. See the SMBus Address Select Table for the addresses.
30	HIGH_BW#	IN	3.3V input for selecting PLL Band Width 0 = High, 1= Low
31	FS2	IN	Frequency select pin.
32	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
33	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
34	FS1	IN	3.3V Frequency select latched input pin.
35	BYPASS#/PLL	IN	Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode
36	VTTPWRGD#/PD	IN	VTTPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.
37	DIF_6#	OUT	0.7V differential complement clock output
38	DIF_6	OUT	0.7V differential true clock output
39	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
40	GND	PWR	Ground pin.
41	VDD	PWR	Power supply, nominal 3.3V
42	DIF_7#	OUT	0.7V differential complement clock output
43	DIF_7	OUT	0.7V differential true clock output
44	OE7#	IN	Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs
45	DIF_8#	OUT	0.7V differential complement clock output
46	DIF_8	OUT	0.7V differential true clock output
47	OE8#	IN	Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs
48	VDD	PWR	Power supply, nominal 3.3V
49	GND	PWR	Ground pin.
50	DIF_9#	OUT	0.7V differential complement clock output
51	DIF_9	OUT	0.7V differential true clock output
52	OE9#	IN	Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs
53	DIF_10#	OUT	0.7V differential complement clock output
54	DIF_10	OUT	0.7V differential true clock output
55	OE10#	IN	Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs
56	GND	PWR	Ground pin.
57	VDD	PWR	Power supply, nominal 3.3V
58	DIF_11#	OUT	0.7V differential complement clock output
59	DIF_11	OUT	0.7V differential true clock output
60	OE11#	IN	Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs
61	FS0	IN	3.3V Frequency select latched input pin.
62	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
63	AGND	PWR	Analog Ground pin for Core PLL
64	VDDA	PWR	3.3V power for the PLL core.

Absolute Max

Symbol	Parameter	Min	Max	Units
VDDA	3.3V Core Supply Voltage		4.6	V
VDD	3.3V Logic Supply Voltage		4.6	V
V_{IL}	Input Low Voltage	GND-0.5		V
V_{IH}	Input High Voltage		V_{DD}+0.5V	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	GND - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			375	mA	1
Powerdown Current	$I_{DD3.3PD}$	all differential pairs tri-stated			24	mA	1
Input Frequency	F_{iPLL}	PLL Mode	100		400	MHz	1
	$F_{iBYPASS}$	Bypass Mode	33		400	MHz	1
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
PLL Jitter Peaking	j_{PEAK}	Peaking when HIGH_BW#=0		1.5	2	dB	1
		Peaking when HIGH_BW#=1		1.5	2	dB	1
PLL Bandwidth	BW	PLL Bandwidth when HIGH_BW#=0	2	3	4	MHz	1
		PLL Bandwidth when HIGH_BW#=1	0.7	1	1.4	MHz	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1.8	ms	1,2
Modulation Frequency	f_{MOD}	Triangular Modulation	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	cycles	1,3
Tdrive_PD	t_{DRVPD}	DIF output enable after PD de-assertion			300	us	1,3
Tfall	t_F	Fall time of OE#			5	ns	1
Trise	t_R	Rise time of OE#			5	ns	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3]Time from deassertion until outputs are >200 mV

Electrical Characteristics - Clock Input Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through Vswing min centered around differential zero

Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, R_{REF}=475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values			0	ppm	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50%	2.5		4.5	ps	1
	t_{pdPLL}	PLL Mode V_T = 50%	-250		250	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50%			50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode			50	ps	1,5
		BYPASS mode as additive jitter			50	ps	1,5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK509B accuracy requirements. The 9DB1200 itself does not contribute to ppm error.

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[4] Applies to Bypass Mode Only

[5] Measured from differential waveform

Electrical Characteristics - Phase Jitter

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNITS	NOTES
Jitter, Phase	tjphase	PCIe Gen 1 REFCLK phase jitter (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)		35	86	ps	1,2,3
		PCIe Gen 2 REFCLK phase jitter (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=12 ns) Lo-band content (10kHz to 1.5MHz)		1.1	3	ps rms	1,2
		PCIe Gen 2 REFCLK phase jitter (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=12 ns) Hi-band content (1.5MHz to Nyquist)		2.3	3.1	ps rms	1,2
		QPI specs REFCLK phase jitter		0.25	0.5	ps rms	2,4

Notes on Phase Jitter:

[1] See http://www.pcisig.com for complete specs. Guaranteed by design and characterization, not tested in production.

[2] Device driven by 932S421BGLF or equivalent

[3] BER of 1E-9

[4] Measured at 133MHz using CSI_133_MHZ_6_4BG_12UI template in Intel supplied Clock Jitter Tool.

DIF Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

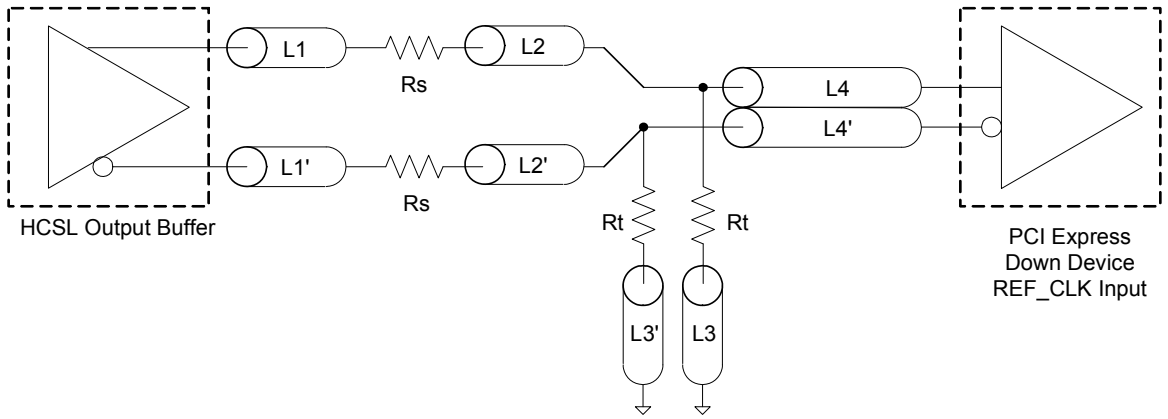
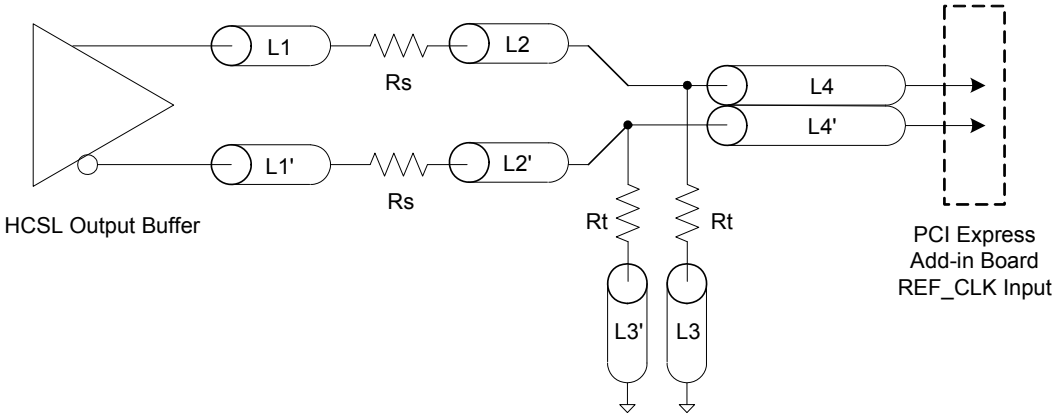


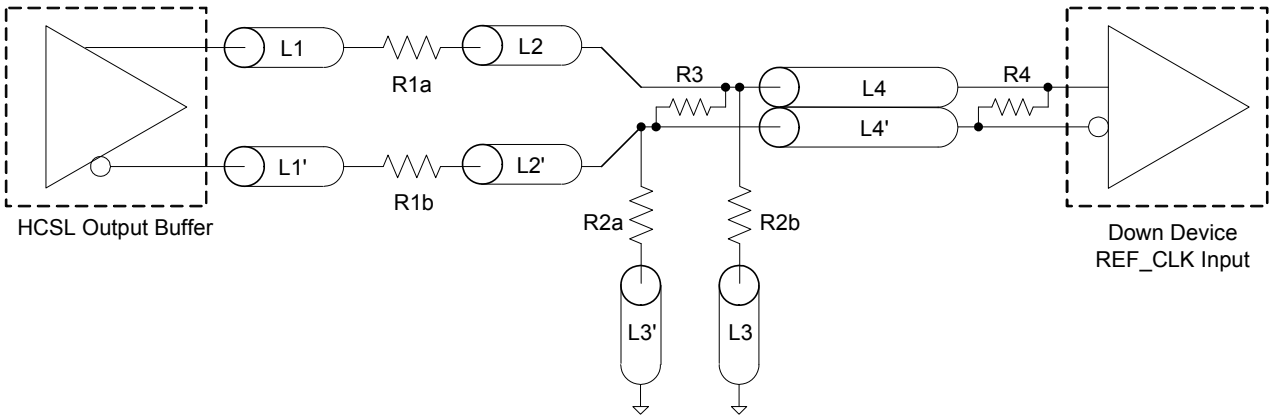
Figure 2: PCI Express Connector Routing



Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

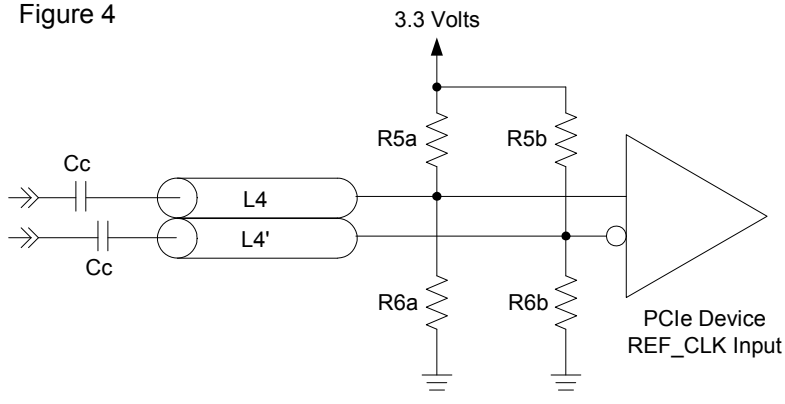
R1a = R1b = R1
R2a = R2b = R2

Figure 3



Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



General SMBus serial interface information for the 9DB1200C

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $DC_{(h)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $DC_{(h)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $DD_{(h)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(h)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $DC_{(h)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $DC_{(h)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $DD_{(h)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Note: Addresses show assumes pin 29 is low.

SMBus Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	HIGH_BW#	High or Low BW	RW	High BW	Low BW	Latch
Bit 6	-	BYPASS#/PLL	Bypass (non-PLL Mode) or PLL Mode	RW	Bypass	PLL	Latch
Bit 5	-	Reserved	Reserved	RW	Reserved		X
Bit 4	-	Reserved	Reserved	RW	Reserved		X
Bit 3	-	Reserved	Reserved	RW	Reserved		X
Bit 2	-	FS2	Frequency Select 2	RW	See FS Table		Latch
Bit 1	-	FS1	Frequency Select 1	RW			Latch
Bit 0	-	FS0	Frequency Select 0	RW			Latch

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	43,42	DIF_7	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 6	38,37	DIF_6	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 5	27,28	DIF_5	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 4	22,23	DIF_4	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 3	19,20	DIF_3	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 2	14,15	DIF_2	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 1	11,12	DIF_1	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 0	6,7	DIF_0	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	RW	Reserved		0
Bit 5	-	Reserved	Reserved	RW	Reserved		0
Bit 4	-	Reserved	Reserved	RW	Reserved		0
Bit 3	58,59	DIF_11	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 2	53,54	DIF_10	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 1	50,51	DIF_9	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 0	45,46	DIF_8	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1

SMBus Table: Output Enable Readback

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	43,42	OE7#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 6	38,37	OE6#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 5	27,28	OE5#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 4	22,23	OE4#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 3	19,20	OE3#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 2	14,15	OE2#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 1	11,12	OE1#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 0	6,7	OE0#	OE# Pin Readback	R	Enabled	Disabled	X

SMBus Table: Output Enable Readback

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	Reserved		0
Bit 6	-	Reserved	Reserved	R	Reserved		0
Bit 5	-	Reserved	Reserved	R	Reserved		0
Bit 4	-	Reserved	Reserved	R	Reserved		0
Bit 3	58,59	OE11#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	X
Bit 2	53,54	OE10#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	X
Bit 1	50,51	OE9#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	X
Bit 0	45,46	OE8#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	X

Note: For an output to be enabled, BOTH the Output Enable Bit and the OE# pin must be enabled. This means that the Output Enable Bit must be '1' and the corresponding OE# pin must be '0'.

SMBus Table: Vendor & Revision ID Register

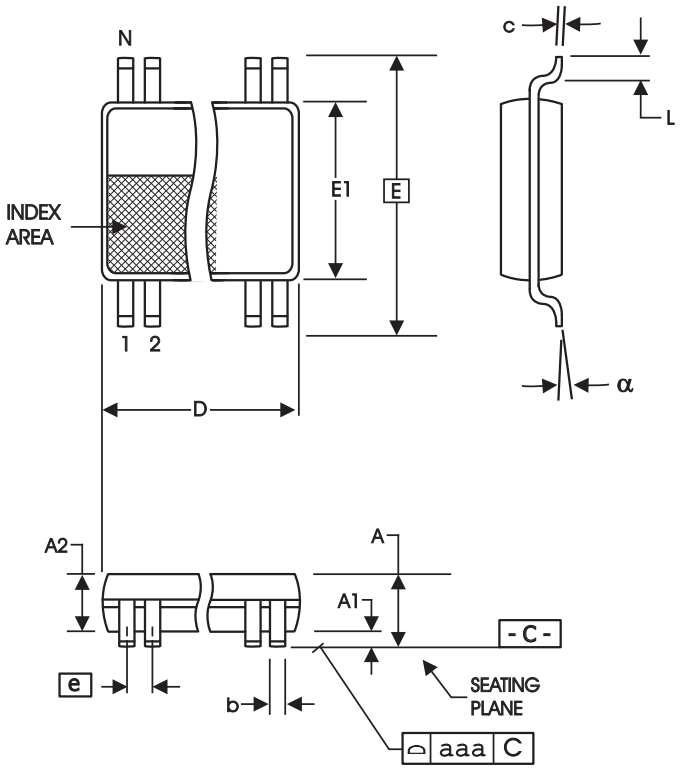
Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	1
Bit 0	-	VID0		R	-	-	0

SMBus Table: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)		RW	Device ID is 0C Hex		0
Bit 6	-	Device ID 6		RW			0
Bit 5	-	Device ID 5		RW			0
Bit 4	-	Device ID 4		RW			0
Bit 3	-	Device ID 3		RW			1
Bit 2	-	Device ID 2		RW			1
Bit 1	-	Device ID 1		RW			0
Bit 0	-	Device ID 0		RW			0

SMBus Table: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DB1200CGLF	Tubes	64-pin TSSOP	0 to +70°C
9DB1200CGLFT	Tape and Reel	64-pin TSSOP	0 to +70°C

"LF" after the package code denotes the Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Issue Date	Description	Page #
A	12/18/2007	1. Updated SMBus Serial Interface Information. 2. Release to Final.	10
B	4/7/2008	Added Input Clock Parameters	6
C	8/28/2008	1. Updated Phase Jitter Numbers 2. Added PLL BW and jitter peaking specs 3. Added input to output delay specs 5. Updated stabilization time to 1.8ms from 1.0ms	
D	9/15/2009	1. Corrected pin number references in SMBus Bytes 1 and 3 2. Added typical values to phase jitter table.	Various
E	11/4/2009	Changed CLK Stabilization spec from 1.0 to 1.8 ms	5
F	7/1/2010	Corrected power groups table for input clock,	2
G	8/15/2012	Updated Byte 5 VENDOR ID (bits 3 through 0) from 0001 to 0010	12

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(Rev.1.0 Mar 2020)

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