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REVISION HISTORY

4/2018—Rev. 0 to Rev. A

Change to Enhanced Product Features Section 1
Changes to Ordering Guide 15

9/2011—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5292-EP

V_{DD} = 21 V to 33 V, V_{SS} = 0 V; V_{DD} = 10.5 V to 16.5 V, V_{SS} = −10.5 V to −16.5 V; V_{LOGIC} = 2.7 V to 5.5 V, $V_A = V_{DD}$, $V_B = V_{SS}$, −55°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		10			Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC	−1		+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} =20 kΩ, $\|V_{DD} - V_{SS}\|$ = 26 V to 33 V	−2		+2	LSB
	R-INL	R_{AB} =20 kΩ, $\|V_{DD} - V_{SS}\|$ = 21 V to 26 V	−3		+3	LSB
Nominal Resistor Tolerance (R-Perf Mode)[3]	$\Delta R_{AB}/R_{AB}$	See Table 2	−1	±0.5	+1	%
Nominal Resistor Tolerance (Normal Mode)[4]	$\Delta R_{AB}/R_{AB}$			±7		%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale; see Figure 14		35		ppm/°C
Wiper Resistance	R_W	Code= zero scale		60	100	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity[5]	DNL		−1		+1	LSB
Integral Nonlinearity[5]	INL		−2.5		+2.5	LSB
Voltage Divider Temperature Coefficient[4]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale; see Figure 17		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−8		+1	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		10	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[6]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[4]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale		85		pF
Capacitance W[4]	C_W	f = 1 MHz, measured to GND, code = half scale		65		pF
Common-Mode Leakage Current[4]	I_{CM}	$V_A = V_B = V_W$	−120	±1	120	nA
DIGITAL INPUTS		JEDEC compliant				
Input Logic High[4]	V_{IH}	V_{LOGIC} = 2.7 V to 5.5 V	2.0			V
Input Logic Low[4]	V_{IL}	V_{LOGIC} = 2.7 V to 5.5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{LOGIC}			±1	μA
Input Capacitance[4]	C_{IL}			5		pF
DIGITAL OUTPUTS (SDO and RDY)						
Output High Voltage[4]	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}	V_{LOGIC} − 0.4			V
Output Low Voltage[4]	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}			GND + 0.4	V
Three-State Leakage Current			−1		+1	μA
Output Capacitance[4]	C_{OL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	9		33	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±9		±16.5	V
Positive Supply Current	I_{DD}	V_{DD}/V_{SS} = ±16.5 V		0.1	2	μA
Negative Supply Current	I_{SS}	V_{DD}/V_{SS} = ±16.5 V	−2	−0.1		μA
Logic Supply Range	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V, V_{IH} = 5 V or V_{IL} = GND		1	10	μA
OTP Store Current[4,7]	I_{LOGIC_PROG}	V_{IH} = 5 V or V_{IL} = GND		25		mA
OTP Read Current[4,8]	$I_{LOGIC\_FUSE\_READ}$	V_{IH} = 5 V or V_{IL} = GND		25		mA
Power Dissipation[9]	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND		8	110	μW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10%		0.103		%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[5, 10]						
Bandwidth	BW	−3 dB		520		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		−93		dB
V_W Settling Time	t_S	V_A = 30 V, V_B = 0 V, ±0.5 LSB error band, initial code = zero scale, board capacitance = 170 pF				
		Code = full-scale, normal mode		750		ns
		Code = full-scale, R-Perf mode		2.5		µs
		Code = half-scale, normal mode		2.5		µs
		Code = half-scale, R-Perf mode		5		µs
Resistor Noise Density	e_{N_WB}	Code = half-scale, T_A = 25°C, 0 kHz to 200 kHz		10		nV/√Hz

[1] Typical values represent average readings at 25°C, V_{DD} = 15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between R_{WB} at Code 0x00B and Code 0x3FF or between R_{WA} at Code 0x3F3 and Code 0x000. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode, with a wiper current of 1 mA for V_A < 12 V and 1.2 mA for V_A ≥ 12 V.
[3] Resistor performance mode. The terms resistor performance mode and R-Perf mode are used interchangeably.
[4] Guaranteed by design and characterization, not subject to production test.
[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[7] Different from operating current; supply current for fuse program lasts approximately 550 µs.
[8] Different from operating current; supply current for fuse read lasts approximately 550 µs.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$) + ($I_{LOGIC} \times V_{LOGIC}$).
[10] All dynamic characteristics use V_{DD} = 15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.

RESISTOR PERFORMANCE MODE CODE RANGE

Table 2.

Resistor Tolerance per Code	−55°C < T_A < +125°C							
	$\|V_{DD} - V_{SS}\|$ = 30 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 26 V to 30 V		$\|V_{DD} - V_{SS}\|$ = 22 V to 26 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 22 V	
	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}
1% R-Tolerance	From 0x1EF to 0x3FF	From 0x000 to 0x210	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	N/A	N/A
2% R-Tolerance	From 0x0C3 to 0x3FF	From 0x000 to 0x33C	From 0x0E6 to 0x3FF	From 0x000 to 0x319	From 0x131 to 0x3FF	From 0x000 to 0x2CE	From 0x131 to 0x3FF	From 0x000 to 0x2CE
3% R-Tolerance	From 0x073 to 0x3FF	From 0x000 to 0x38C	From 0x087 to 0x3FF	From 0x000 to 0x378	From 0x0AF to 0x3FF	From 0x000 to 0x350	From 0x0AF to 0x3FF	From 0x000 to 0x350

INTERFACE TIMING SPECIFICATIONS

V_{DD}/V_{SS} = ±15 V, V_{LOGIC} = 2.7 V to 5.5 V, −55°C < T_A < +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit[1]	Unit	Description
t_1[2]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	1	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	400[3]	ns min	Minimum $\overline{SYNC}$ high time
t_9	14	ns min	$\overline{SYNC}$ rising edge to next SCLK fall ignore
t_{10}[4]	1	ns min	RDY rising edge to $\overline{SYNC}$ falling edge
t_{11}[4]	40	ns max	$\overline{SYNC}$ rising edge to RDY fall time
t_{12}[4]	2.4	µs max	RDY low time, RDAC register write command execute time (R-Perf mode)
t_{12}[4]	410	ns max	RDY low time, RDAC register write command execute time (normal mode)
t_{12}[4]	8	ms max	RDY low time, memory program execute time
t_{12}[4]	1.5	ms min	Software/hardware reset
t_{13}[4]	450	ns max	RDY low time, RDAC register readback execute time
t_{13}[4]	1.3	ms max	RDY low time, memory readback execute time
t_{14}[4]	450	ns max	SCLK rising edge to SDO valid
t_{RESET}	20	ns min	Minimum $\overline{RESET}$ pulse width (asynchronous)
$t_{POWER-UP}$[5]	2	ms max	Power-on OTP restore time

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Maximum SCLK frequency is 50 MHz.
[3] Refer to t_{12} and t_{13} for RDAC register and memory commands operations.
[4] R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}, with a capacitance load of 168 pF.
[5] Maximum time after V_{LOGIC} is equal to 2.5 V.

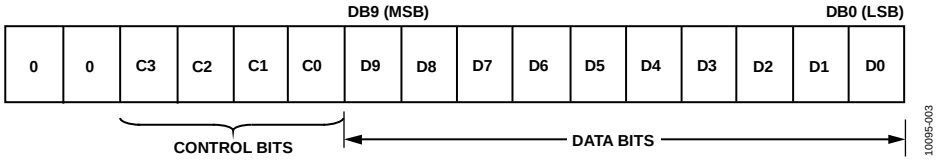

Figure 2. Shift Register Content

Timing Diagrams

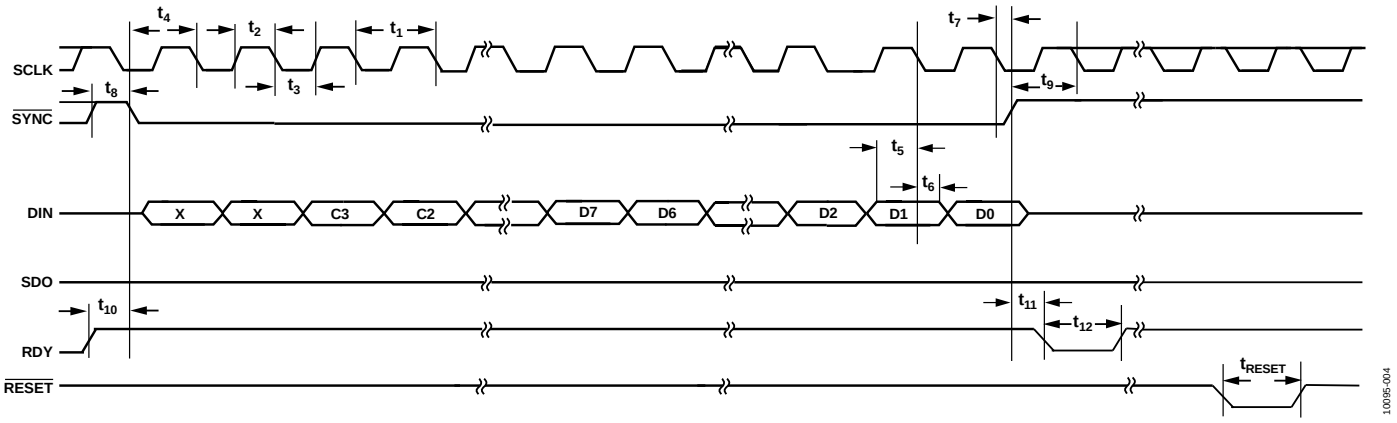

Figure 3. Write Timing Diagram, CPOL = 0, CPHA = 1

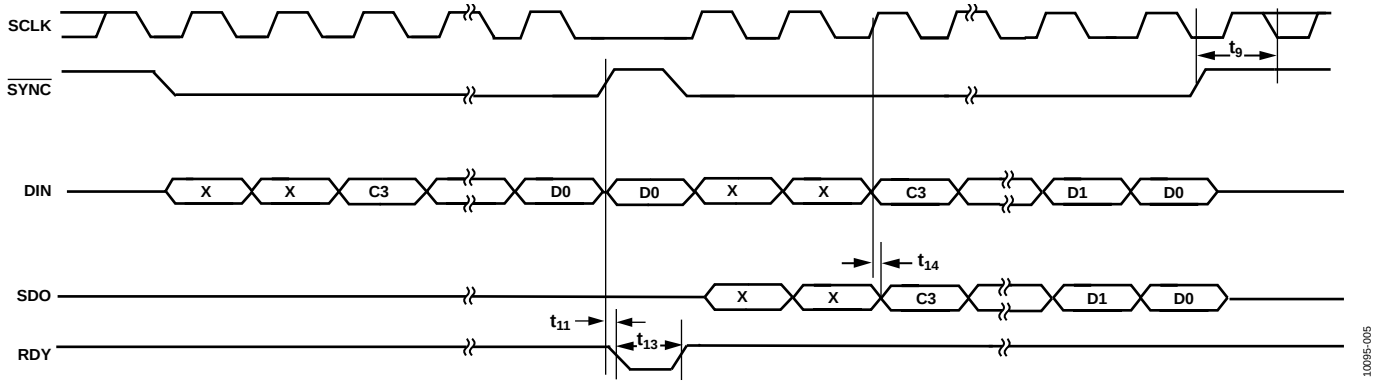

Figure 4. Read Timing Diagram, CPOL = 0, CPHA = 1

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +35 V
V_{SS} to GND	+0.3 V to −25 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{DD} to V_{SS}	35 V
V_A, V_B, V_W to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
Digital Input and Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
EXT_CAP Voltage to GND	−0.3 V to +7 V
I_A, I_B, I_W	
Continuous	±3 mA
Pulsed[1]	
Frequency > 10 kHz	±3/d[2]
Frequency ≤ 10 kHz	±3/√d[2]
Operating Temperature Range[3]	−55°C to +125°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Pulse duty factor.
[3] Includes programming of OTP memory.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead TSSOP	93[1]	20	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec to 1 m/sec air flow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

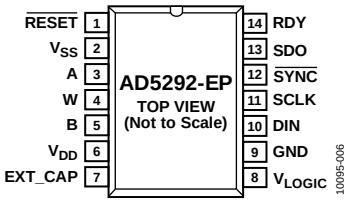

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Hardware Reset Pin. Refreshes the RDAC register with the contents of the 20-TP memory register. Factory default loads midscale until the first 20-TP wiper memory location is programmed. $\overline{\text{RESET}}$ is activated at the logic high transition. Tie $\overline{\text{RESET}}$ to V_{LOGIC} if not used.
2	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
3	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$.
4	W	Wiper Terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$.
5	B	Terminal B of RDAC. $V_{SS} \le V_B \le V_{DD}$.
6	V_{DD}	Positive Power Supply. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
7	EXT_CAP	External Capacitor. Connect a 1 µF capacitor to EXT_CAP. This capacitor must have a voltage rating of ≥7 V.
8	V_{LOGIC}	Logic Power Supply; 2.7 V to 5.5 V. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
9	GND	Ground Pin, Logic Ground Reference.
10	DIN	Serial Data Input. The AD5292-EP has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
11	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
12	$\overline{\text{SYNC}}$	Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the shift register and data is transferred in on the falling edges of the following clocks. The selected register is updated on the rising edge of $\overline{\text{SYNC}}$ following the 16th clock cycle. If $\overline{\text{SYNC}}$ is taken high before the 16th clock cycle, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC.
13	SDO	Serial Data Output. This open-drain output requires an external pull-up resistor. SDO can be used to clock data from the shift register in daisy-chain mode or in readback mode.
14	RDY	Ready Pin. This active-high open-drain output identifies the completion of a write or read operation to or from the RDAC register or memory.

TYPICAL PERFORMANCE CHARACTERISTICS

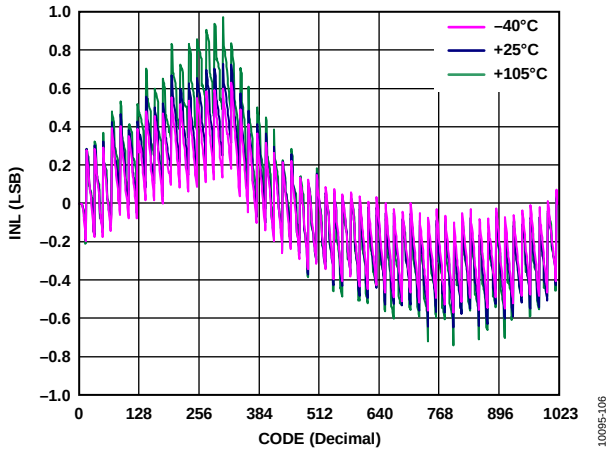

Figure 6. R-INL in R-Perf Mode vs. Code

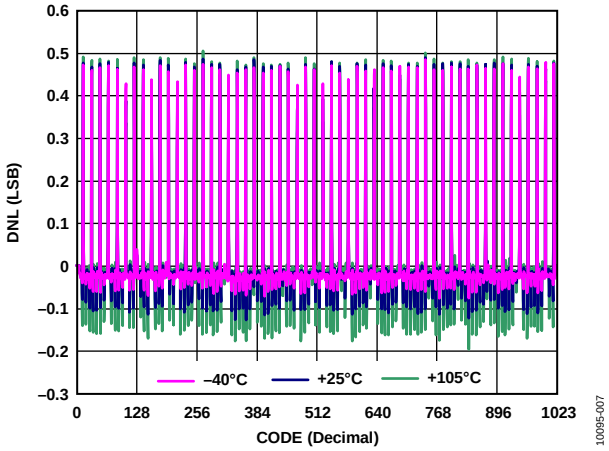

Figure 9. R-DNL in R-Perf Mode vs. Code

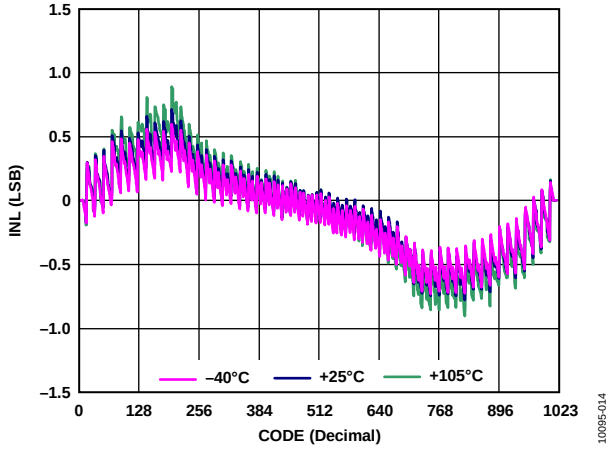

Figure 7. INL in R-Perf Mode vs. Code

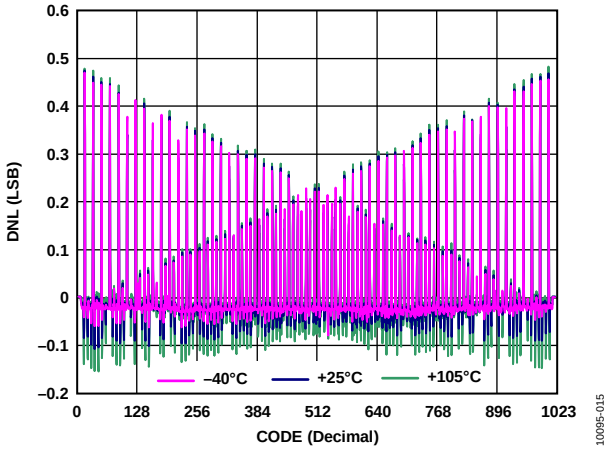

Figure 10. DNL in R-Perf Mode vs. Code

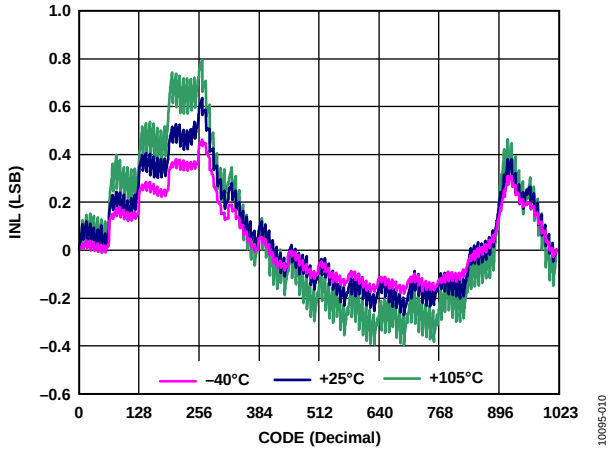

Figure 8. R-INL in Normal Mode vs. Code

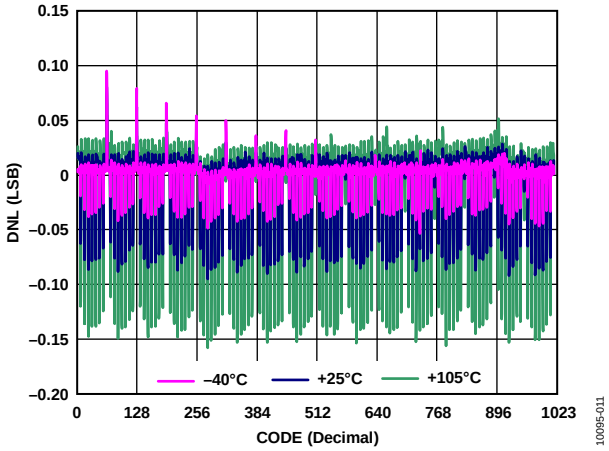

Figure 11. R-DNL in Normal Mode vs. Code

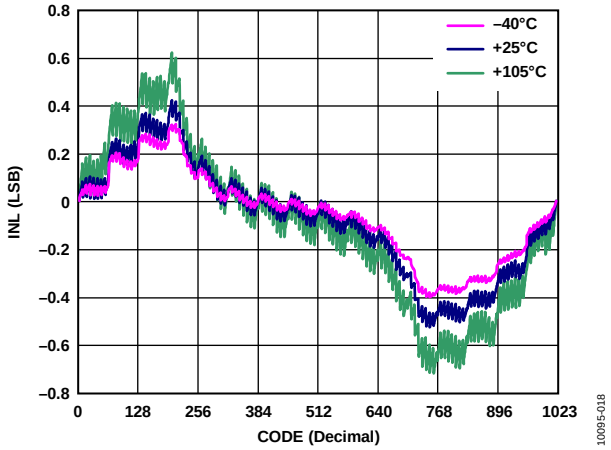

Figure 12. INL in Normal Mode vs. Code

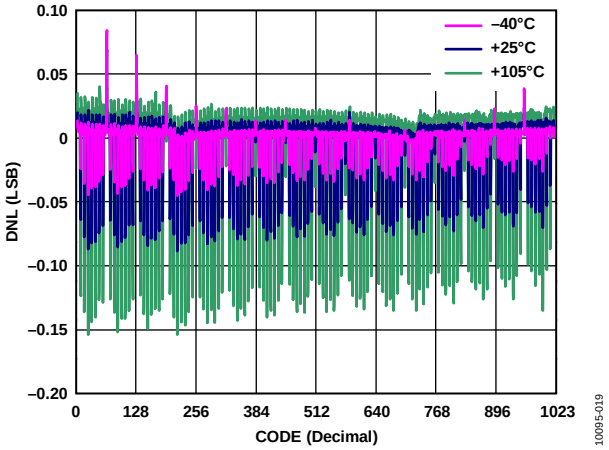

Figure 15. DNL in Normal Mode vs. Code

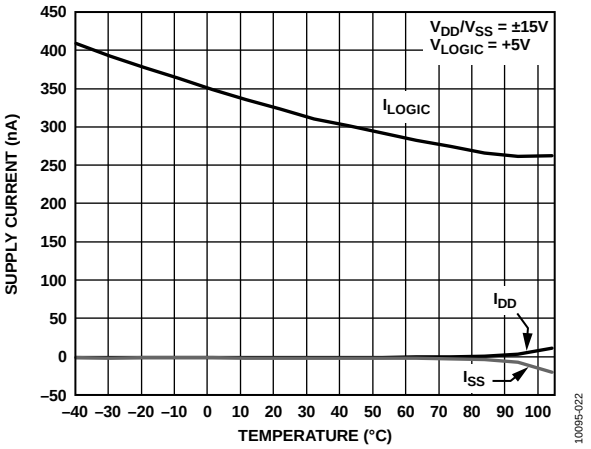

Figure 13. Supply Current (I_{DD}, I_{SS}, I_{LOGIC}) vs. Temperature

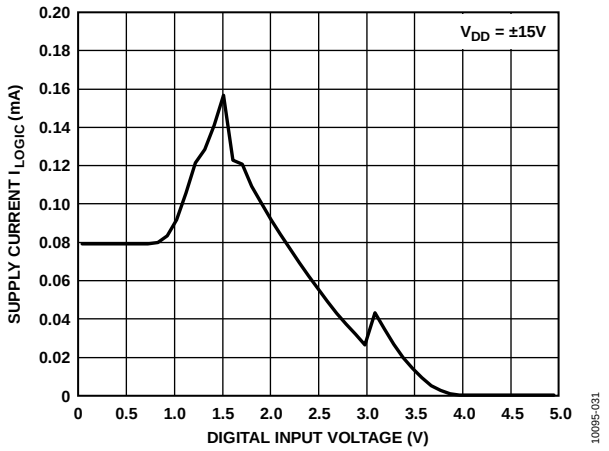

Figure 16. Supply Current I_{LOGIC} vs. Digital Input Voltage

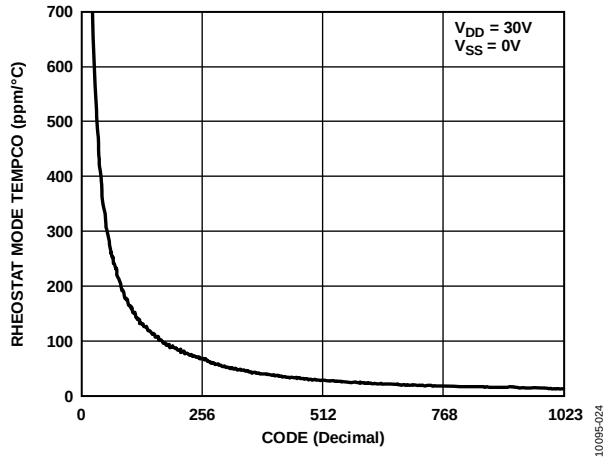

Figure 14. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

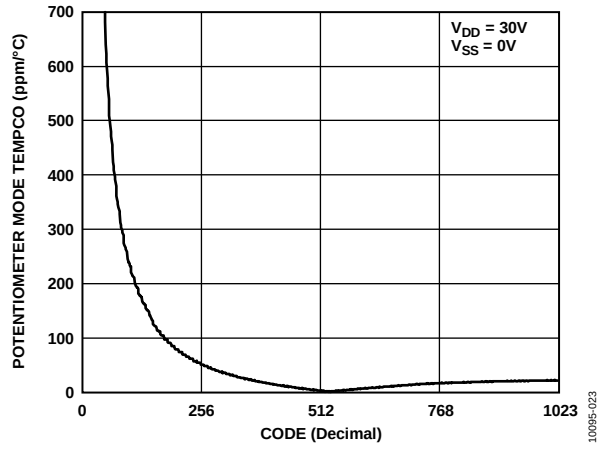

Figure 17. Potentiometer Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

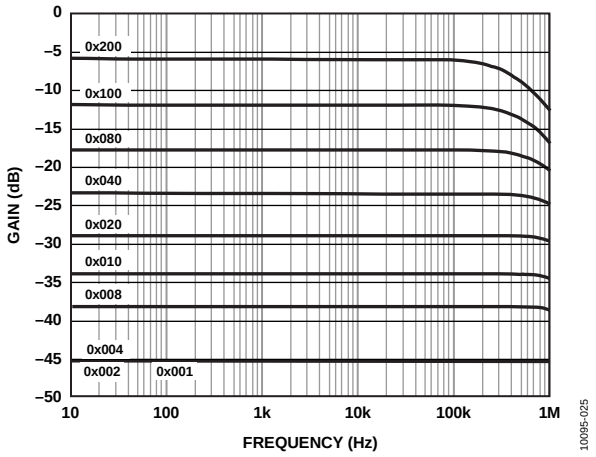

Figure 18. 20 kΩ Gain vs. Frequency vs. Code

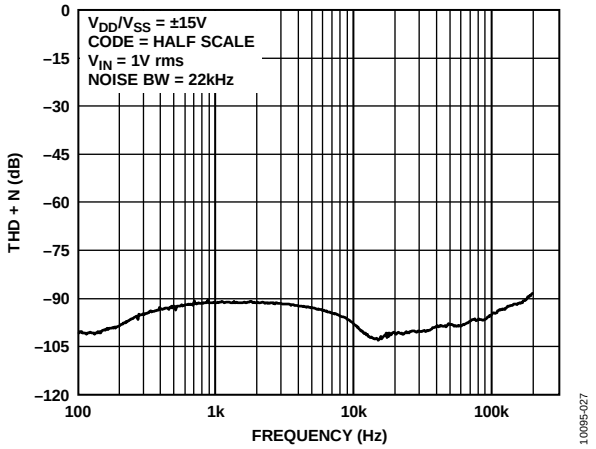

Figure 19. THD + Noise vs. Frequency

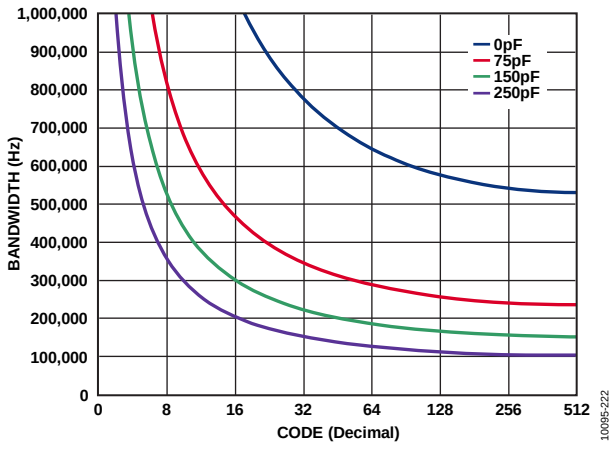

Figure 20. Bandwidth vs. Code vs. Net Capacitance

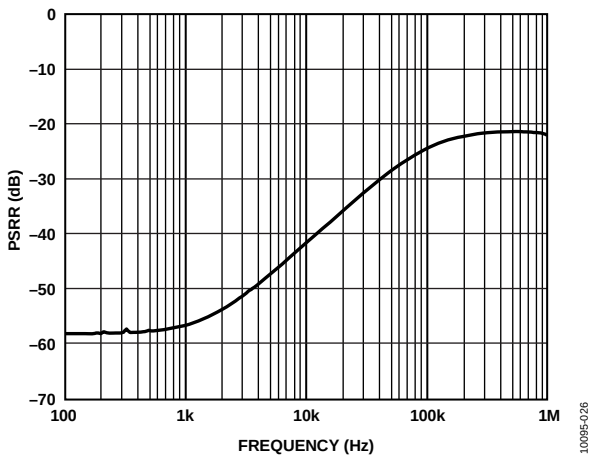

Figure 21. Power Supply Rejection Ratio vs. Frequency

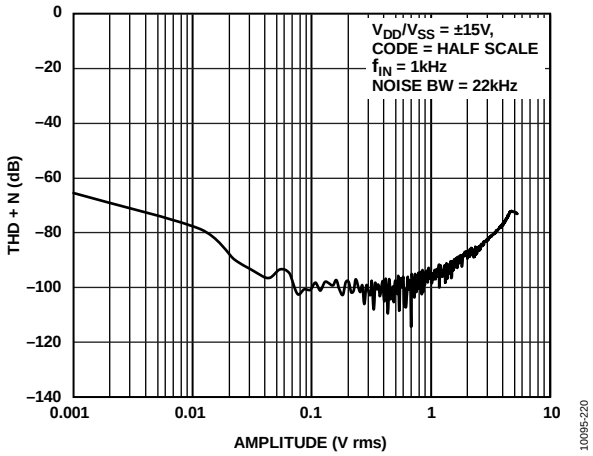

Figure 22. THD + Noise vs. Amplitude

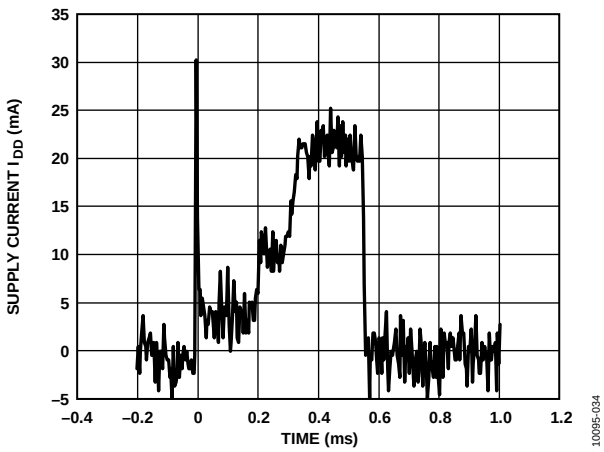

Figure 23. I_{DD} Waveform While Blowing/Reading Fuse

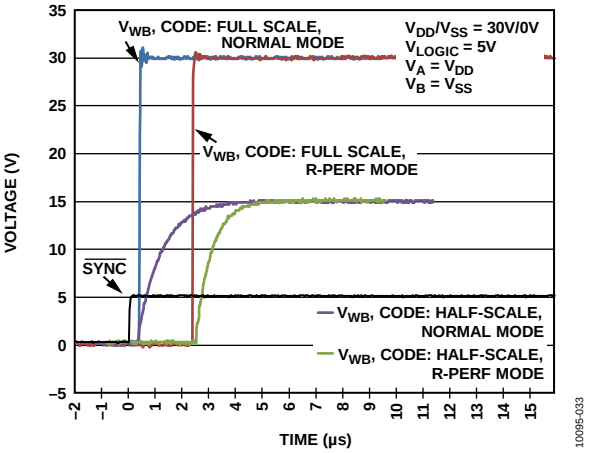

Figure 24. Large-Signal Settling Time from Code Zero Scale

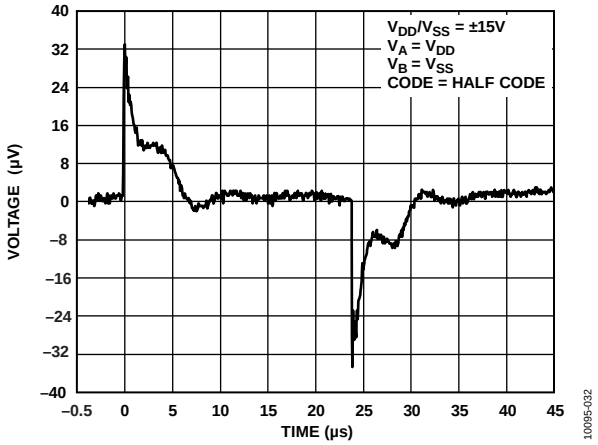

Figure 27. Digital Feedthrough

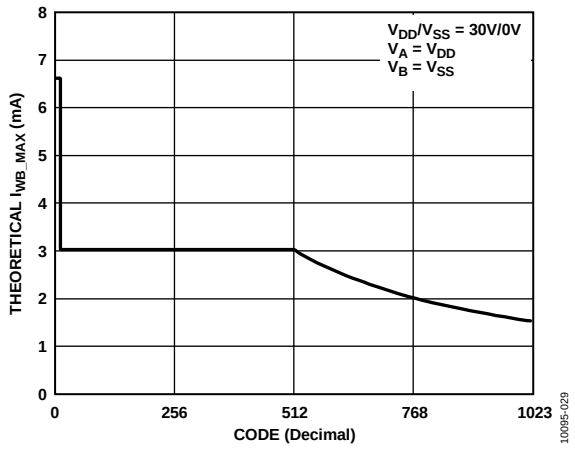

Figure 25. Theoretical Maximum Current vs. Code

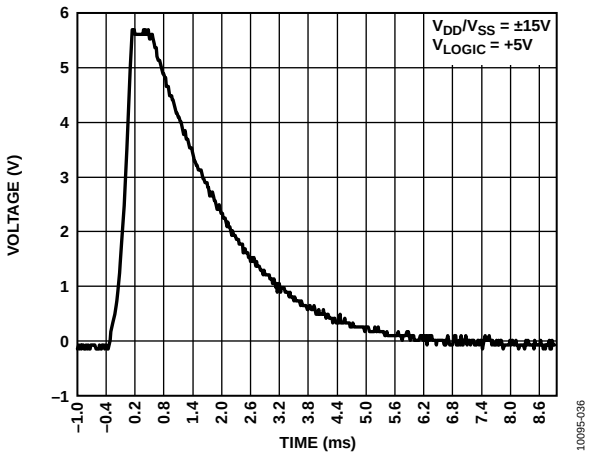

Figure 28. V_{EXT_CAP} Waveform While Reading Fuse Or Calibration

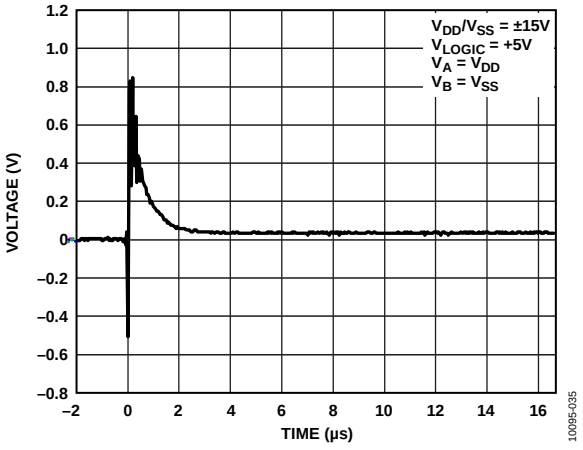

Figure 26. Maximum Transition Glitch

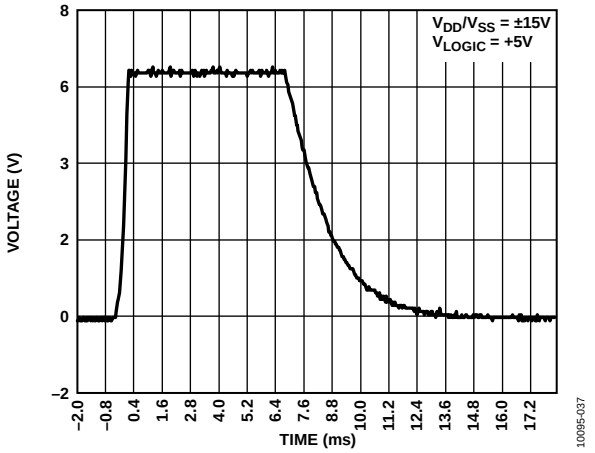

Figure 29. V_{EXT_CAP} Waveform While Writing Fuse

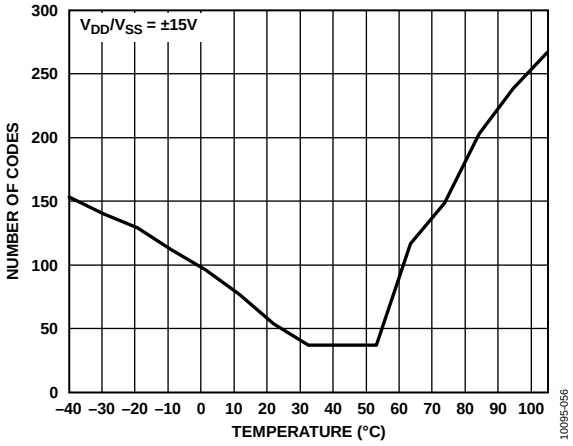

Figure 30. Code Range > 1% R-Tolerance Error vs. Temperature

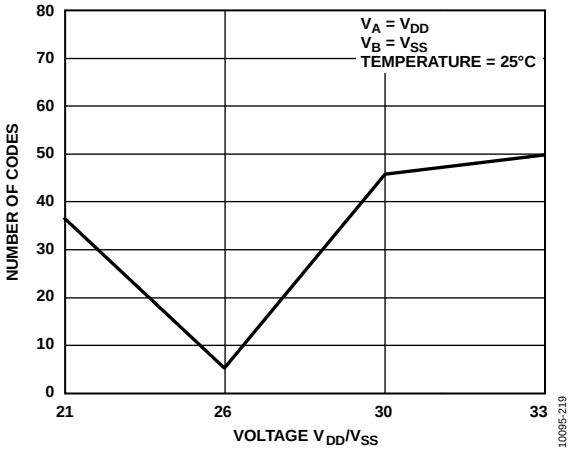

Figure 31. Code Range > 1% R-Tolerance Error vs. Voltage

TEST CIRCUITS

Figure 32 to Figure 37 define the test conditions used in the Specifications section.

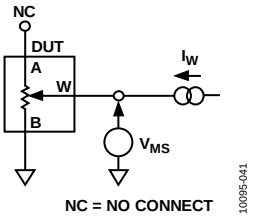

Figure 32. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

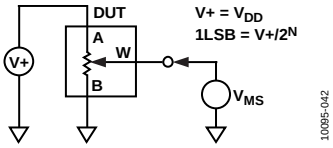

Figure 33. Potentiometer Divider Nonlinearity Error (INL, DNL)

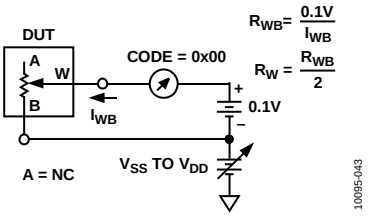

Figure 34. Wiper Resistance

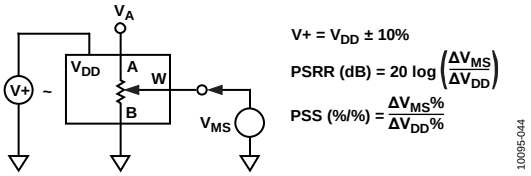

Figure 35. Power Supply Sensitivity (PSS, PSRR)

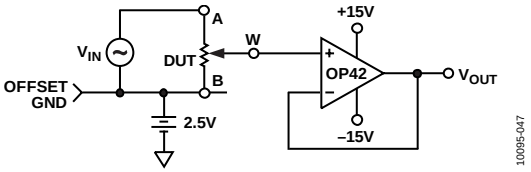

Figure 36. Gain vs. Frequency

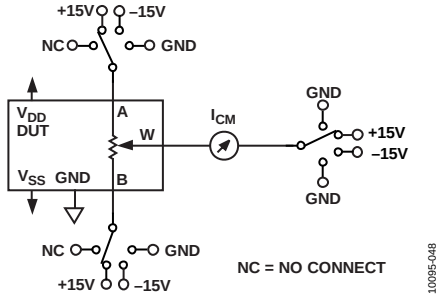

Figure 37. Common-Mode Leakage Current

OUTLINE DIMENSIONS

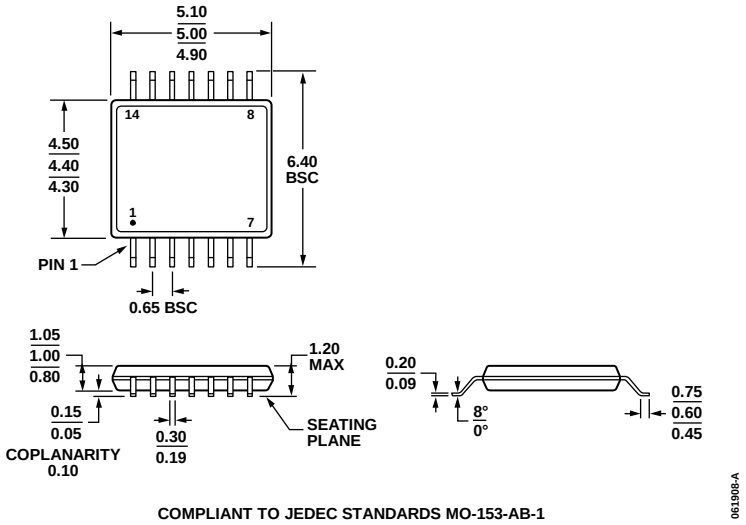

Figure 38. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Resolution	Memory	Temperature Range	Package Description	Package Option
AD5292SRU-20-EP	20	1024	20-TP	−55°C to +125°C	14-Lead TSSOP	RU-14
AD5292SRUZ-20-EP	20	1024	20-TP	−55°C to +125°C	14-Lead TSSOP	RU-14

[1] Z = RoHS Compliant Part.

NOTES

D10095-0-4/18(A)

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Analog Devices Inc.:

AD5292BRUZ-20 AD5292BRUZ-50 AD5292BRUZ-100-RL7 AD5292BRUZ-100 EVAL-AD5292EBZ AD5292BRUZ-50-RL7 AD5292BRUZ-20-RL7 AD5292SRUZ-20-EP EVAL-AD5292DBZ