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REVISION HISTORY

8/08—Rev. 0 to Rev A

Changes to Supply Current Parameter	4
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1/07—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$, all switch sections unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ ¹	Max	Unit
ANALOG SWITCH						
Analog Signal Range			0		V_{DD}	V
On Resistance	R_{ON}	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$ (see Figure 18) Wide bandwidth section ² Low distortion section ³		5.9	8.8	Ω
On Resistance Flatness	$R_{FLAT(ON)}$	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$ (see Figure 18) Wide bandwidth section ² Low distortion section ³		3.9	5.5	Ω
On Resistance Matching Between Channels ⁴	ΔR_{ON}	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$ Wide bandwidth section ² Low distortion section ³ (SPDT) Low distortion section ³ (4:1 multiplexers)		2.0	3.6	Ω
				0.74	1.6	Ω
					0.52	Ω
					0.1	Ω
					0.3	Ω
LEAKAGE CURRENTS						
Source Off Leakage	I_S (Off)	$V_{DD} = 3.6\text{ V}$, $V_S = 0\text{ V or }3.6\text{ V}$, $V_D = 3.6\text{ V or }0\text{ V}$ (see Figure 19)		± 10		nA
Channel On Leakage	I_D , I_S (On)	$V_{DD} = 3.6\text{ V}$, $V_S = V_D = 0\text{ V or }3.6\text{ V}$ (see Figure 20)		± 10		nA
DIGITAL INPUTS (IN1, IN2, IN3, S/D)						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}				0.8	V
Input High/Input Low Current ⁵	I_{INL} , I_{INH}	$V_{IN} = V_{INL}$ OR V_{INH}		± 0.005	± 0.1	μA
Digital Input Capacitance	C_{IN}			6		pF
DYNAMIC CHARACTERISTICS⁵						
t_{ON}	t_{ON}	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = V_{DD}/2$ or 0 V (see Figure 24)		20	32	ns
t_{OFF}	t_{OFF}	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = V_{DD}/2$ or 0 V (see Figure 24)		9	15	ns
Propagation Delay	t_D	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ Wide bandwidth section ² Low distortion section ³ (SPDT) Low distortion section ³ (4:1 multiplexers)		0.3	0.46	ns
				0.65	0.95	ns
				0.4	0.65	ns
Propagation Delay Skew	t_{SKEW}	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ Wide bandwidth section ² Low distortion section ³ (4:1 multiplexers)		20		ps
				40		ps
Break-Before-Make Time Delay	t_{BBM}	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = V_{DD}/2$ (see Figure 25)	5	11		ns
Charge Injection	Q_{INJ}	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ (see Figure 26) Wide bandwidth section ² Low distortion section ³		-0.57		pC
				6.2		pC
Off Isolation		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ (see Figure 21)		-74		dB
Channel-to-Channel Crosstalk		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ (see Figure 22)		-77		dB
Total Harmonic Distortion	THD + N	$R_L = 32\ \Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_S = 2\text{ V p-p}$ Wide bandwidth section ² Low distortion section ³		1.2		%
				0.65		%
-3 dB Bandwidth		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ (see Figure 23) Wide bandwidth section ² Low distortion section ³ (SPDT) Low distortion section ³ (4:1 multiplexers)		550		MHz
				230		MHz
				160		MHz
Differential Gain Error		CCIR330 test signal Wide bandwidth section ² Low distortion section ³ (SPDT) Low distortion section ³ (4:1 multiplexers)		0.07		%
				0.08		%
				0.18		%

ADG790

Parameter	Symbol	Test Conditions/Comments	Min	Typ ¹	Max	Unit
Differential Phase Error		CCIR330 test signal				
		Wide bandwidth section ²		0.13		Degrees
		Low distortion section ³ (SPDT)		0.08		Degrees
Power Supply Rejection Ratio	PSRR	Low distortion section ³ (4:1 multiplexers) f = 10 kHz, no decoupling capacitors		0.19		Degrees
Source Off Capacitance	C _S (Off)	Wide bandwidth section ²		3.5		pF
		Low distortion section ³		11		pF
Drain Off Capacitance	C _D (Off)	Wide bandwidth section ²		5.5		pF
		Low distortion section ³ (SPDT)		14		pF
Source/Drain On Capacitance	C _D , C _S (On)	Wide bandwidth section ²		8.5		pF
		Low distortion section ³ (SPDT)		19		pF
		Low distortion section ³ (4:1 multiplexers)		32		pF
POWER REQUIREMENTS						
Supply Voltage	V _{DD}		1.65		3.6	V
Supply Current	I _{DD}	V _{DD} = 3.6 V, digital inputs tied to 0 V or 3.6 V		0.1	1.5	μA

¹ All typical values are at T_A = 25°C, V_{DD} = 3.3 V.

² Refers to all switches connected to Pin D1, Pin D2, and Pin D3.

³ Refers to all switches connected to Pin D4 (SPDT), Pin D5, and Pin D6 (4:1 multiplexers).

⁴ Refers to the on resistance matching between the same channels (S_xA and S_xB, for example) from different multiplexers for the wide bandwidth section and the 4:1 multiplexers from the low distortion section. For the SPDT switch from the low distortion section, it refers to the matching between the S4A and S4B channels.

⁵ Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	-0.3 V to +4.6 V
Analog and Digital Pins ¹	-0.3 V to $V_{DD} + 0.3$ V or 10 mA, whichever occurs first
Peak Current, S Pin or D Pin	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S Pin or D Pin	30 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C
Junction Temperature	150°C
Thermal Impedance (θ_{JA}) ²	80°C/W
Reflow Soldering (Pb Free)	
Peak Temperature	260°C (+0°C/-5°C)
Time at Peak Temperature	As per JEDEC J-STD-20

¹ Overvoltages at INx, S pin or D pin are clamped by internal diodes. Limit current to the maximum ratings given.

² Measured with the device soldered on a 4-layer board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

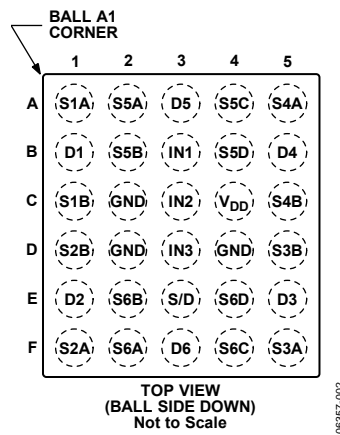


Figure 2. 30-Ball WLCSP (CB-30-1)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	S1A	Source Terminal for Mux 1 (Wide Bandwidth Section). Can be an input or an output.
A2	S5A	Source Terminal for Mux 5 (Low Distortion Section). Can be an input or an output.
A3	D5	Drain Terminal for Mux 5 (Low Distortion Section). Can be an input or an output.
A4	S5C	Source Terminal for Mux 5 (Low Distortion Section). Can be an input or an output.
A5	S4A	Source Terminal for Mux 4 (Low Distortion Section). Can be an input or an output.
B1	D1	Drain Terminal for Mux 1 (Wide Bandwidth Section). Can be an input or an output.
B2	S5B	Source Terminal for Mux 5 (Low Distortion Section). Can be an input or an output.
B3	IN1	Logic Control Input.
B4	S5D	Source Terminal for Mux 5 (Low Distortion Section). Can be an input or an output.
B5	D4	Drain Terminal for Mux 4 (Low Distortion Section). Can be an input or an output.
C1	S1B	Source Terminal for Mux 1 (Wide Bandwidth Section). Can be an input or an output.
C2	GND	Ground (0 V) Reference.
C3	IN2	Logic Control Input.
C4	V _{DD}	Most Positive Power Supply Terminal.
C5	S4B	Source Terminal for Mux 4 (Low Distortion Section). Can be an input or an output.
D1	S2B	Source Terminal for Mux 2 (Wide Bandwidth Section). Can be an input or an output.
D2	GND	Ground (0 V) Reference.
D3	IN3	Logic Control Input.
D4	GND	Ground (0 V) Reference.
D5	S3B	Source Terminal for Mux 3 (Wide Bandwidth Section). Can be an input or an output.
E1	D2	Drain Terminal for Mux 2 (Wide Bandwidth Section). Can be an input or an output.
E2	S6B	Source Terminal for Mux 6 (Low Distortion Section). Can be an input or an output.
E3	S/D	Shutdown Logic Control Input.
E4	S6D	Source Terminal for Mux 6 (Low Distortion Section). Can be an input or an output.
E5	D3	Drain Terminal for Mux 3 (Wide Bandwidth Section). Can be an input or an output.
F1	S2A	Source Terminal for Mux 2 (Wide Bandwidth Section). Can be an input or an output.
F2	S6A	Source Terminal for Mux 6 (Low Distortion Section). Can be an input or an output.
F3	D6	Drain Terminal for Mux 6 (Low Distortion Section). Can be an input or an output.
F4	S6C	Source Terminal for Mux 6 (Low Distortion Section). Can be an input or an output.
F5	S3A	Source Terminal for Mux 3 (Wide Bandwidth Section). Can be an input or an output.

TYPICAL PERFORMANCE CHARACTERISTICS

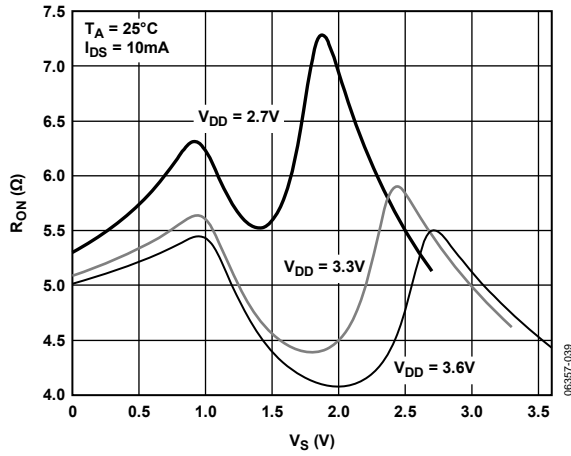


Figure 3. On Resistance vs. Source Voltage, Wide Bandwidth Section

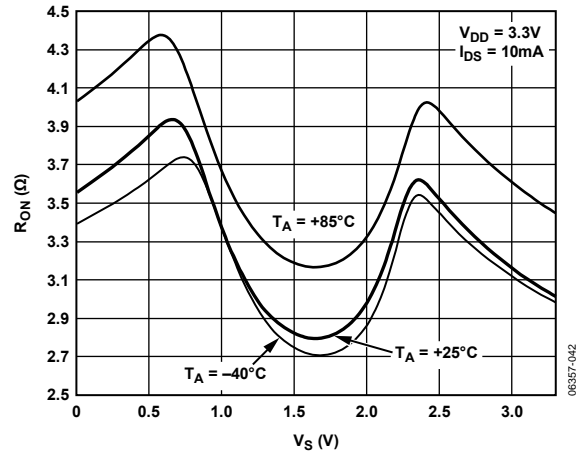


Figure 6. On Resistance vs. Temperature, Low Distortion Section

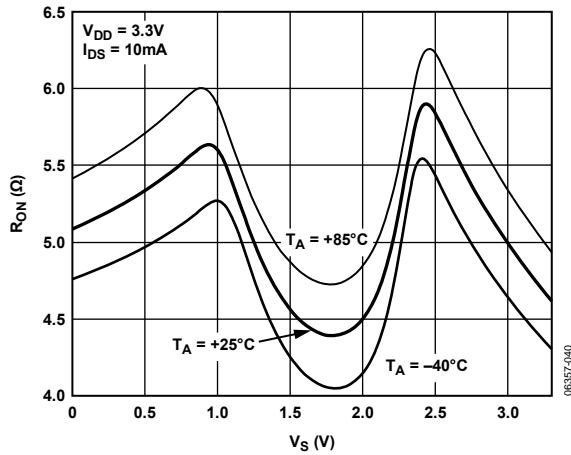


Figure 4. On Resistance vs. Temperature, Wide Bandwidth Section

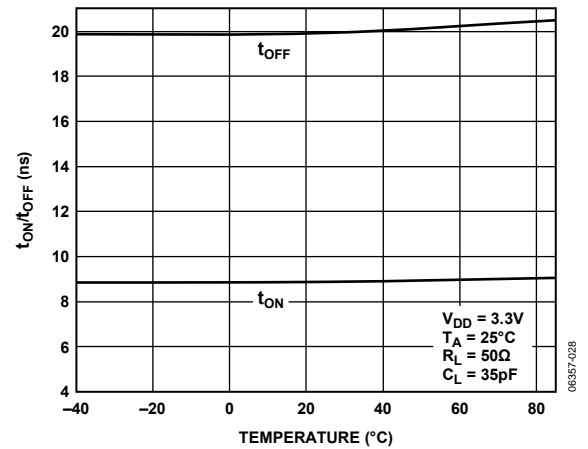


Figure 7. t_{ON}/t_{OFF} Times vs. Temperature

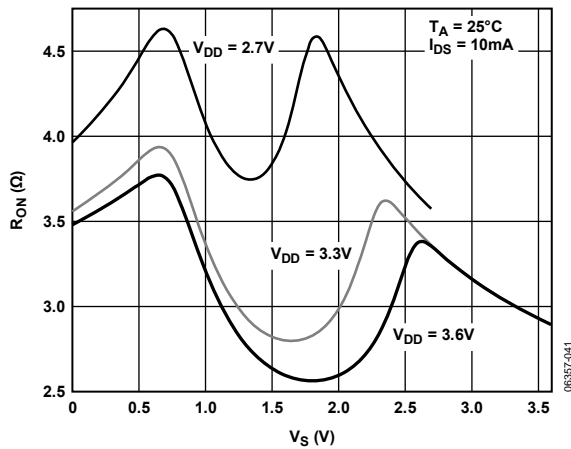


Figure 5. On Resistance vs. Source Voltage, Low Distortion Section

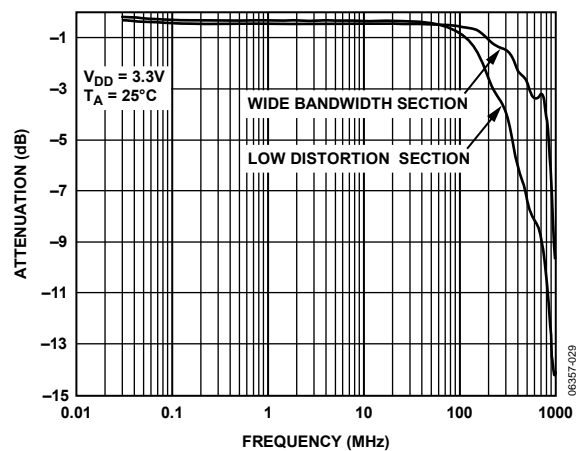


Figure 8. On Response vs. Frequency, Low Distortion Section (SPDT)

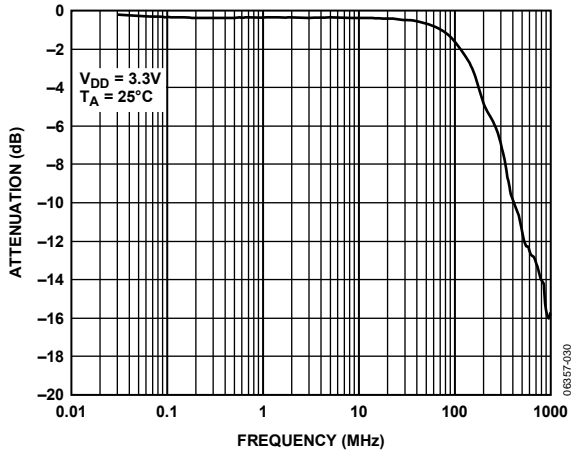


Figure 9. On Response vs. Frequency, Low Distortion Section (4:1 Multiplexers)

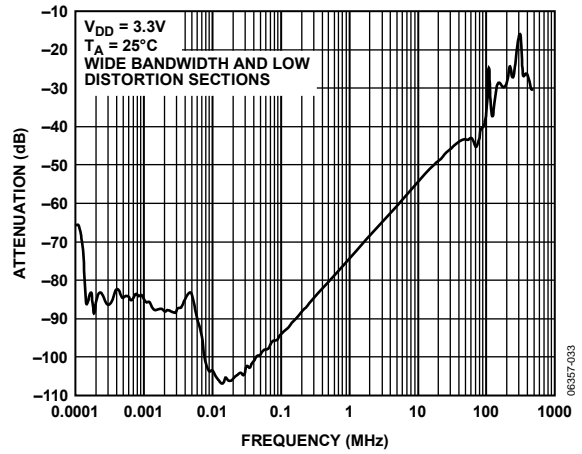


Figure 12. Off Isolation vs. Frequency

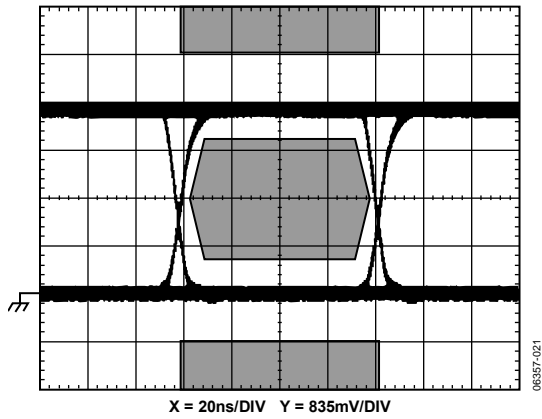


Figure 10. USB 1.1 Eye Diagram

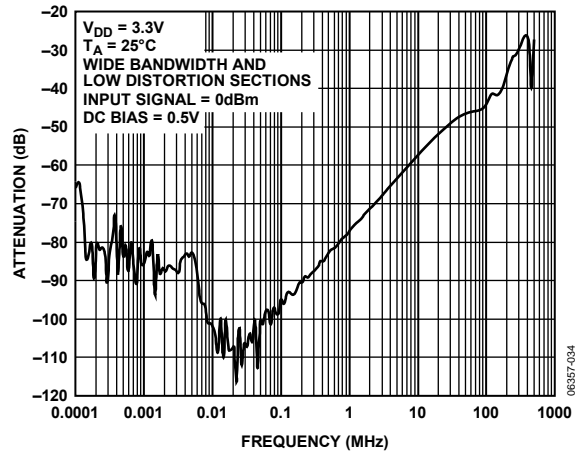


Figure 13. Crosstalk vs. Frequency

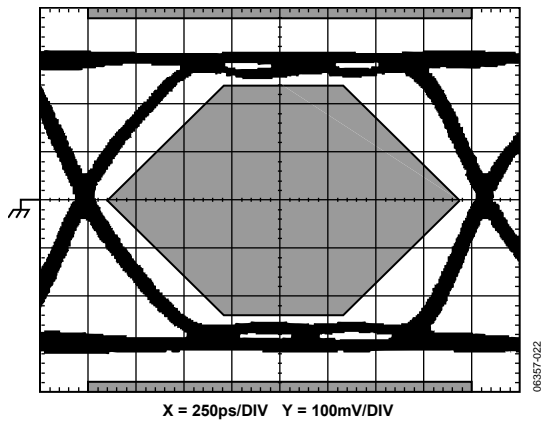


Figure 11. USB 2.0 Eye Diagram

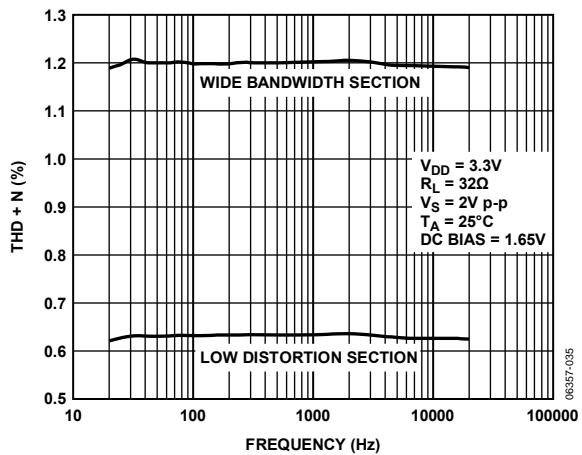


Figure 14. THD + N vs. Frequency

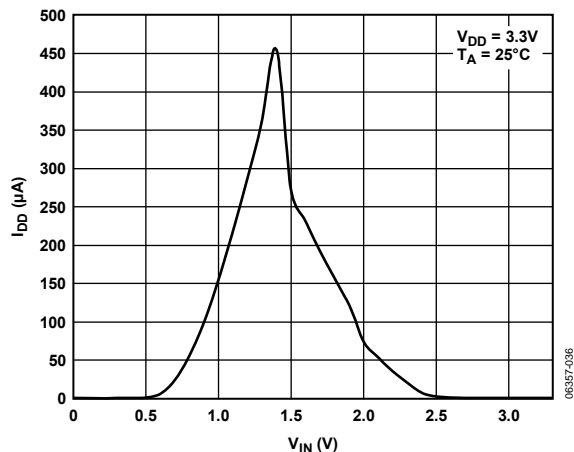


Figure 15. Supply Current vs. Input Logic Level

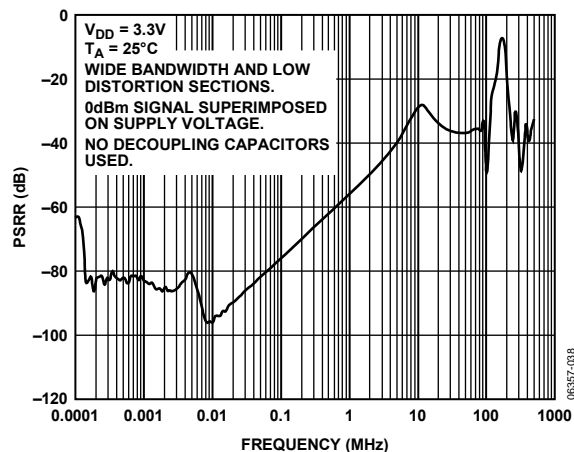


Figure 17. Power Supply Rejection Ratio vs. Frequency

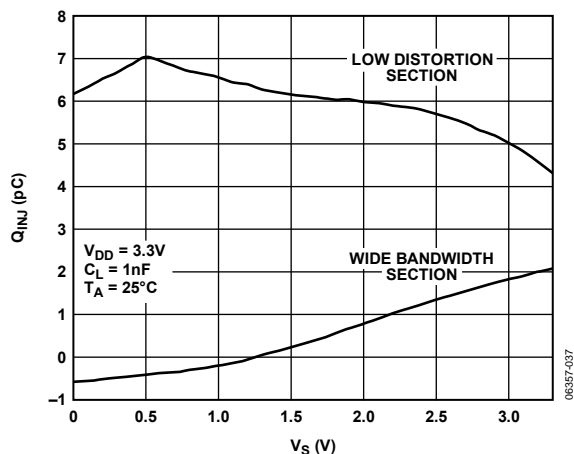


Figure 16. Charge Injection vs. Source Voltage

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (Vs)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}

On resistance match between any two channels.

I_S (Off)

Source leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

Off switch source capacitance. Measured with reference to ground.

C_D, C_S (On)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and the 10% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to the other.

t_D

Signal propagation delay through the switch measured between the 50% points of the input signal and its corresponding output signal.

t_{SKEW}

Difference in propagation delay between the selected inputs on the 4:1 multiplexers or any two SPDT switches from the wide bandwidth section.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

-3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitudes plus signal noise to the fundamental.

Differential Gain Error

The measure of how much color saturation shift occurs when the luminance level changes. Both attenuation and amplification can occur; therefore, the largest amplitude change between any two levels is specified and expressed in percent.

Differential Phase Error

The measure of how much hue shift occurs when the luminance level changes. It can be a negative or a positive value and is expressed in degrees of subcarrier phase.

TEST CIRCUITS

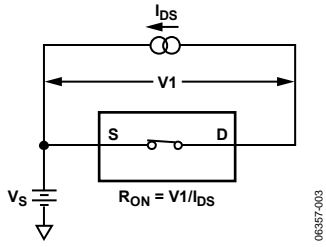


Figure 18. On Resistance

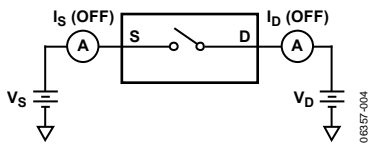


Figure 19. Off Leakage

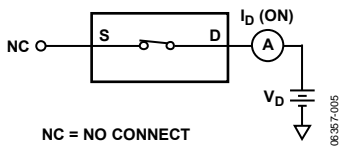
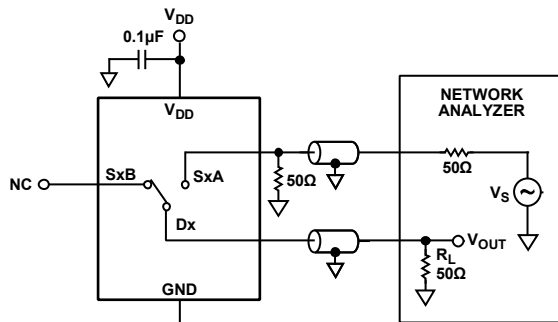


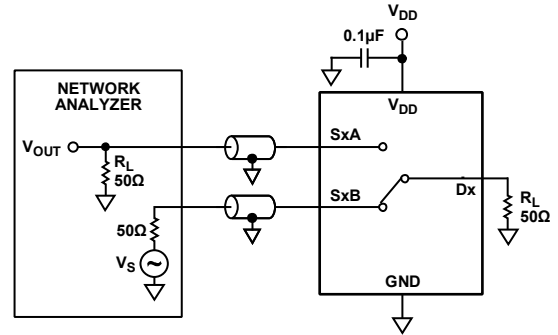
Figure 20. On Leakage



OFF ISOLATION = $20 \log \frac{V_{OUT}}{V_S}$

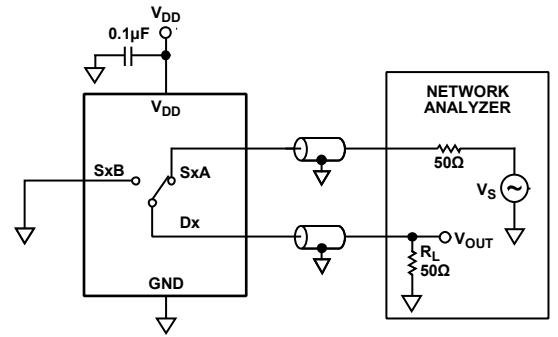
NC = NO CONNECT

Figure 21. Off Isolation



CHANNEL-TO-CHANNEL CROSSTALK = $20 \log \frac{V_{OUT}}{V_S}$

Figure 22. Channel-to-Channel Crosstalk



INSERTION LOSS = $20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$

Figure 23. -3 dB Bandwidth

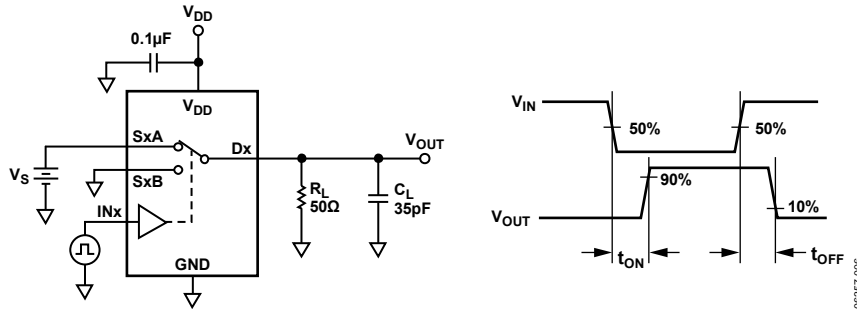


Figure 24. Switching Times (t_{ON} , t_{OFF})

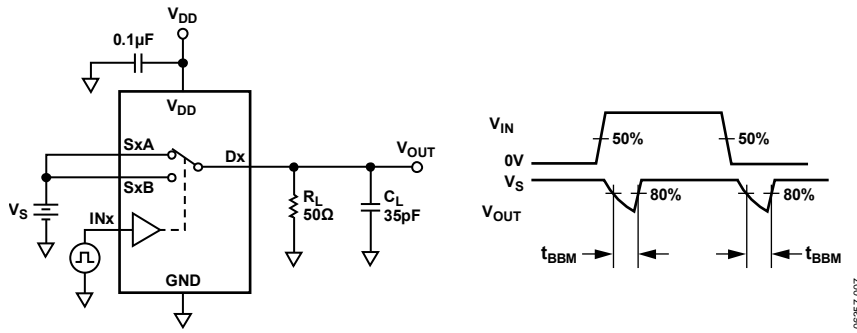


Figure 25. Break-Before-Make Time Delay (t_{BBM})

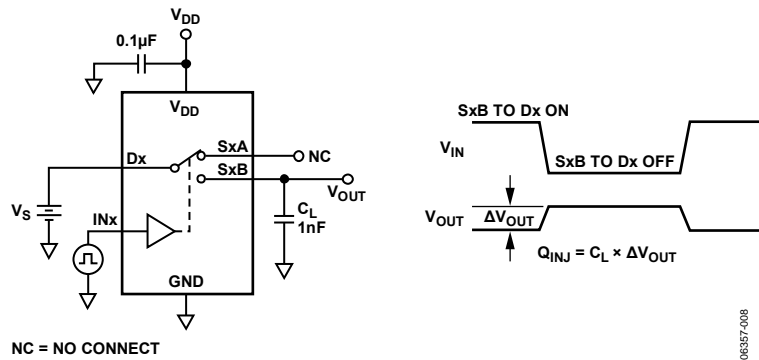


Figure 26. Charge Injection

THEORY OF OPERATION

The ADG790 is a single-chip, CMOS switching solution that comprises four SPDT switches and two 4:1 multiplexers. The internal architecture used by the device groups the switches into two sections, each optimized to provide the best performance in terms of bandwidth and distortion. The on-chip parallel interface controls the operation of all switches, allowing the user to control switches from both sections simultaneously.

WIDE BANDWIDTH SECTION

The wide bandwidth section contains three SPDT switch configurations S1A and S1B to D1, S2A and S2B to D2, and S3A and S3B to D3. Besides low on resistance and excellent flatness, these switches use a CMOS topology, which ensures the ability to switch signals up to the supply rails. Combined with the low switch capacitance, this provides the wide bandwidth required when switching high frequency signals. The three SPDT switches are also optimized to provide low propagation delay and excellent matching between the channels, making the ADG790 ideal for applications that use multiple signals, such as universal USB switches (full speed and high speed), or RGB video signals, such as VGA.

LOW DISTORTION SECTION

The low distortion section contains a single SPDT switch (S4A and S4B to D4) and two 4:1 multiplexers (S5A, S5B, S5C, and S5D to D5 and S6A, S6B, S6C, S6D and D6, respectively). The switches from this section also use a CMOS topology that

exhibits very low on resistance and flatness while maintaining a wide bandwidth that makes them suitable for a wide range of applications, including low distortion audio and standard definition video signals. The channels from the 4:1 multiplexers are matched to provide optimal performance when used with differential signals such as S-Video.

CONTROL INTERFACE

The operation of the ADG790 is controlled via a 4-wire parallel interface. The logic levels applied to the IN1, IN2, and IN3 pins control the operation of the switches from both the wide bandwidth and low distortion sections, as shown in Table 4. The shutdown pin (S/D) allows the user to disable all four SPDT switches and force the 4:1 multiplexers into the S5B and S6B positions, respectively. This function can be used to set up a low speed communication protocol between the circuitry from both sides of the device, which allows automatic configuration of the switching function.

For example, in modern handset applications, where a single connector is used as a multifunction communication port, the S5B to D5 and S6B to D6 configuration obtained by setting the S/D pin high can be used to detect the type of peripheral device connected to the handset. The ADG790 then automatically routes the required signals to the communication port connector.

Table 4. Truth Table

Logic Control Inputs				Switch Status						
S/D	IN1	IN2	IN3	S1A to D1 S2A to D2 S3A to D3 S5D to D5 S6D to D6	S1B to D1 S2B to D2 S3B to D3	S4A to D4	S4B to D4	S5A to D5 S6A to D6	S5B to D5 S6B to D6	S5C to D5 S6C to D6
1	X ¹	X ¹	X ¹	Off	Off	Off	Off	Off	On	Off
0	0	0	0	Off	On	Off	On	Off	Off	On
0	0	0	1	On	Off	On	Off	Off	Off	Off
0	0	1	0	Off	On	On	Off	Off	On	Off
0	0	1	1	Off	On	On	Off	Off	Off	On
0	1	0	0	Off	On	On	Off	On	Off	Off
0	1	0	1	On	Off	Off	On	Off	Off	Off
0	1	1	0	Off	On	Off	On	On	Off	Off
0	1	1	1	Off	On	Off	On	Off	On	Off

¹ X = logic state does not matter.

EVALUATION BOARD

The ADG790 evaluation board allows designers to evaluate the high performance of the device with minimum effort.

The EVAL-ADG790EBZ includes a PCB populated with the ADG790 that can be used to evaluate the performance of the device. The evaluation board interfaces to the USB port of a PC, allowing the user to easily program the ADG790 through the USB port using the software provided with the board. Schematics of the evaluation board are shown in Figure 27 and Figure 28. The software runs on any PC that has Microsoft® Windows® 2000 or Windows® XP installed.

USING THE ADG790 EVALUATION BOARD

The ADG790 evaluation board is a test system designed to simplify the evaluation of the device. Each input/output of the part comes with a standardized socket that allows connection to and from USB, CVBS, S-Video, and VGA signal sources. A data sheet for the ADG790 evaluation board with full information on setup and operation is also available.

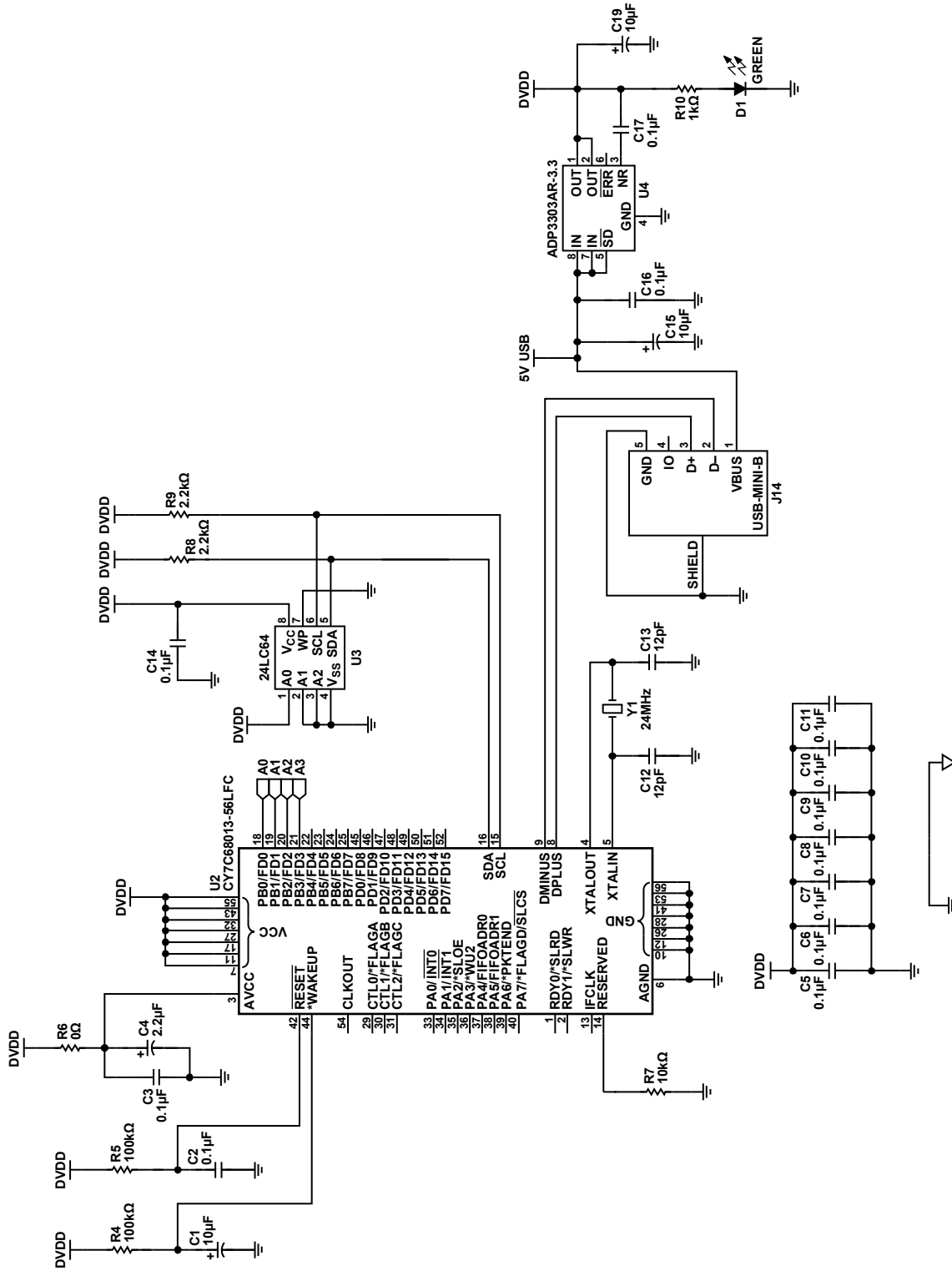


Figure 27. EVAL-ADG790 Schematic USB Controller Section

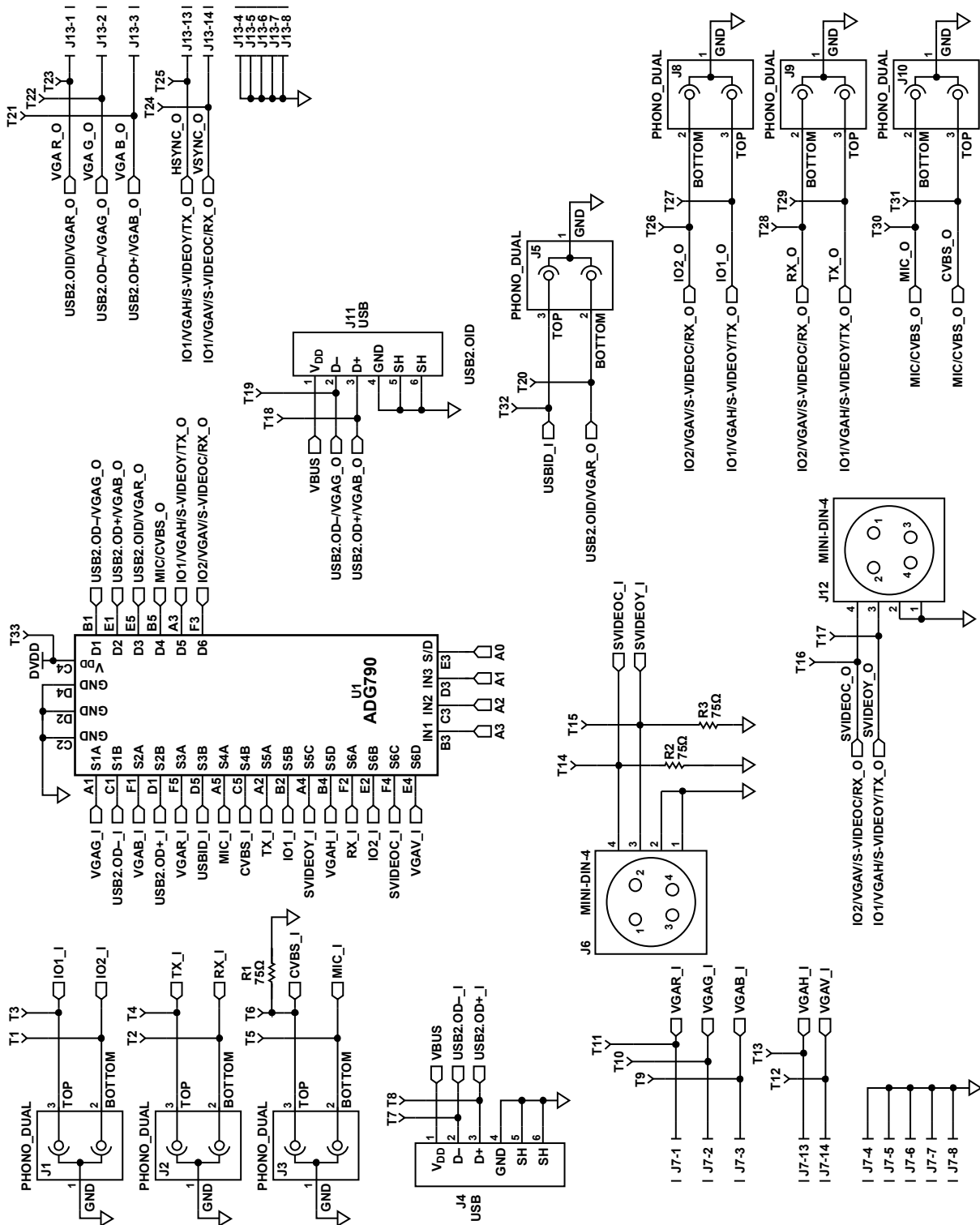


Figure 28. EVAL-ADG790 Schematic Switch Section

OUTLINE DIMENSIONS

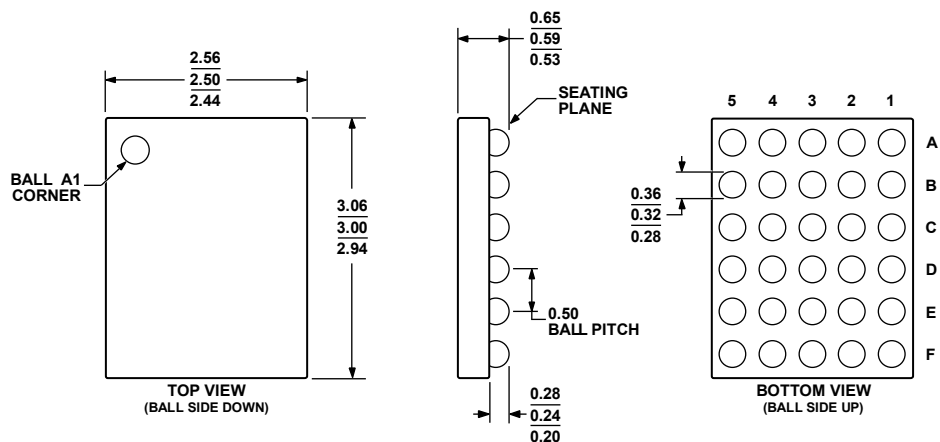


Figure 29. 30-Ball Wafer Level Chip Scale Package [WLCSP] (CB-30-1)
Dimensions shown in millimeters

092106-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG790BCBZ-REEL ¹	-40°C to +85°C	30-Ball Wafer Level Chip Scale Package [WLCSP]	CB-30-1
EVAL-ADG790EBZ ¹		Evaluation Board	

¹ Z = RoHS Compliant Part.

ADG790

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