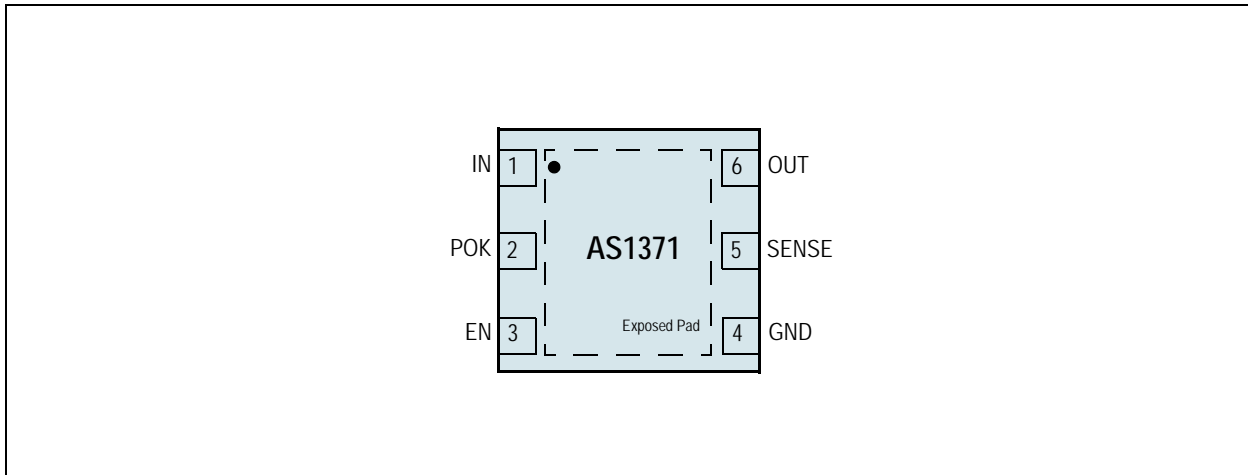


## 4 Pin Assignments

Figure 2. Pin Assignments (Top View)



### 4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	IN	<b>LDO Input.</b> Input voltage range: 1.2V to 3.6V. Bypass with 1 $\mu$ F to GND.
2	POK	<b>Power-OK Output.</b> Active-low, open-drain output indicates an out-of-regulation condition. Connect a 100k $\Omega$ pull-up resistor to pin OUT for logic levels. Leave this pin unconnected if the Power-OK feature is not used.
3	EN	<b>Active-High Enable Input.</b> A logic low reduces the supply current to < 1 $\mu$ A. Connect to pin IN for normal operation.
4	GND	<b>Ground.</b> This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.
5	SENSE	<b>Sense Input.</b> Represents the input for the Power-OK behavior. If connected to GND the POK output is related to OUT.
6	OUT	<b>LDO Output.</b> Bypass with 1 $\mu$ F to GND.
Exposed Pad	GND	<b>Exposed Pad.</b> This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation. Internally it is connected GND.

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Section 6 Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
<b>Electrical Parameters</b>				
IN and EN to GND	-0.3	+5.0	V	
POK and OUT to GND	-0.3	V <sub>IN</sub> + 0.3	V	
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
<b>Electrostatic Discharge</b>				
Electrostatic Discharge HBM		±1000	V	Norm: MIL 883 E method 3015
<b>Temperature Ranges and Storage Conditions</b>				
Thermal Resistance $\theta_{JA}$	+78.6		°C/W	Junction-to-ambient thermal resistance is very dependent on application and board-layout. In situations where high maximum power dissipation exists, special attention must be paid to thermal dissipation during board design.
Junction Temperature		+125	°C	
Storage Temperature Range	-55	+125	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> . The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents a maximum floor life time of unlimited

## 6 Electrical Characteristics

$V_{IN} = V_{OUT} \text{ (Nominal)} + 0.5V$ ,  $EN = IN$ ,  $C_{IN} = C_{OUT} = 1\mu F$ ,  $T_{AMB} = -40^{\circ}C \text{ to } +85^{\circ}C$  (unless otherwise specified).  
Typical Values are at  $T_{AMB} = +25^{\circ}C$ .

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{AMB}$	Operating Temperature Range		-40		+85	$^{\circ}C$
$V_{IN}$	Input Voltage		1.2		3.6	V
$V_{OUT}$	Output Voltage	Available in 50mV steps, see <a href="#">Ordering Information on page 16</a>	0.6		3.3	V
	Output Voltage Accuracy	$T_{AMB} = +25^{\circ}C$ , $I_{OUT} = 1mA$ , $V_{OUT} > 1V$	-2		+2	%
		$T_{AMB} = -40 \text{ to } +85^{\circ}C$ , $I_{OUT} = 1mA$ , $V_{OUT} > 1V$	-3.5		+3.5	
$I_{OUT}$	Maximum Output Current		400			mA
$I_{LIM}$	Current Limit			650		mA
$I_Q$	Quiescent Current	$I_{OUT} = 0mA$		15	20	$\mu A$
		$I_{OUT} = 400mA$		50		
$V_{IN-V_{OUT}}$	Dropout Voltage <sup>1</sup>	$I_{OUT} = 100mA$		20	50	mV
		$I_{OUT} = 400mA$		80		
$\Delta V_{LNR}$	Line Regulation	$I_{OUT} = 1mA$	-15	0	+15	mV
$\Delta V_{LDR}$	Load Regulation	$I_{OUT} = 1mA \text{ to } 400mA$		0.003		%/mA
	Output Voltage Noise	$f = 10Hz \text{ to } 100kHz$ , $I_{OUT} = 10mA$		100		$\mu V_{RMS}$
PSRR	Output Voltage AC Power-Supply Rejection Ratio	$f = 10kHz$ , $I_{OUT} = 10mA$		50		dB
$C_{OUT}$	Output Capacitor	Load Capacitor Range	0.47	1		$\mu F$
		ESR Load			500	m $\Omega$
<b>Shutdown<sup>2</sup></b>						
$t_{ON}$	Exit Delay from Shutdown <sup>3,4</sup>			90	150	$\mu s$
$I_{OFF}$	Enable Supply Current	$EN = GND$ , $T_{AMB} = +25^{\circ}C$		0.01	1	$\mu A$
		$EN = GND$ , $T_{AMB} = +85^{\circ}C$		0.04		
$V_{IH}$	Enable Input Threshold		1.0			V
$V_{IL}$					0.4	
$I_{EN}$	Enable Input Bias Current	$EN = IN \text{ or } GND$ , $T_{AMB} = +25^{\circ}C$		0.03	100	nA
		$EN = IN \text{ or } GND$ , $T_{AMB} = +85^{\circ}C$		0.2		
<b>Power-OK Output</b>						
$V_{POK}$	Power-OK Voltage Threshold <sup>5</sup>	SENSE = GND, $V_{POK\text{FALLING}}$	90	94	97	% $V_{OUT}$
		SENSE = GND, Hysteresis		1		
$V_{SENSE}$	Power-OK Sense Voltage Threshold	$V_{OUT} = 1.05V$ , $V_{SENSE}$ falling	650	800	950	mV
		Hysteresis		50		
$V_{OL}$	POK Output Voltage Low	$I_{SINK} = 100\mu A$			0.4	V

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I <sub>POK</sub>	POK Output Leakage Current	$0 \leq V_{POK} \leq 3.6V$ , T <sub>AMB</sub> = +25°C, V <sub>OUT</sub> in regulation			1	μA
<b>Thermal Protection</b>						
T <sub>SHDN</sub>	Thermal Shutdown Temperature			150		°C
ΔT <sub>SHDN</sub>	Thermal Shutdown Hysteresis			15		°C

1. Dropout voltage = V<sub>IN</sub> - V<sub>OUT</sub> when V<sub>OUT</sub> is 100mV < V<sub>OUT</sub> for V<sub>IN</sub> = V<sub>OUT(NOM)</sub> + 0.5V (applies only to output voltages ≥ 1.3V).
2. The rise and fall time of the shutdown signal must not exceed 1ms.
3. The delay time is defined as time required to set V<sub>OUT</sub> to 95% of its final nominal value.
4. Guaranteed by design.
5. The functionality is proven by production test, limits are guaranteed by design.

**Note:** All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

## 7 Typical Operating Characteristics

$V_{OUT} = 1.8V$ ,  $V_{IN} = 2.3V$ ,  $I_{OUT} = 1mA$ ,  $T_{AMB} = +25^{\circ}C$  (unless otherwise specified).

Figure 3. Output Voltage vs. Temperature

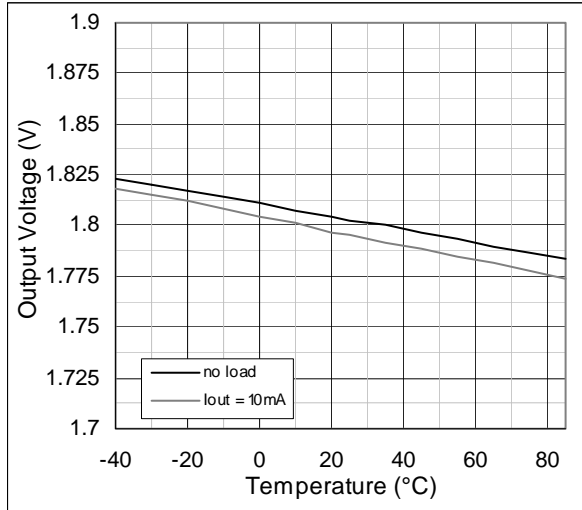


Figure 4. Line Regulation,  $V_{OUT}$  vs.  $V_{IN}$

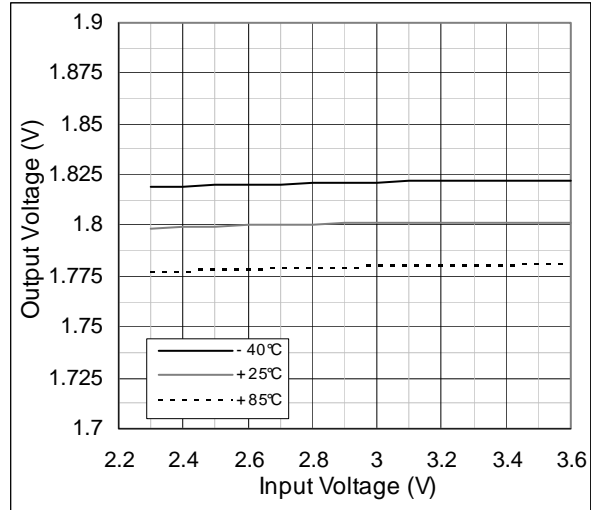


Figure 5. Load Regulation,  $V_{OUT}$  vs.  $I_{OUT}$

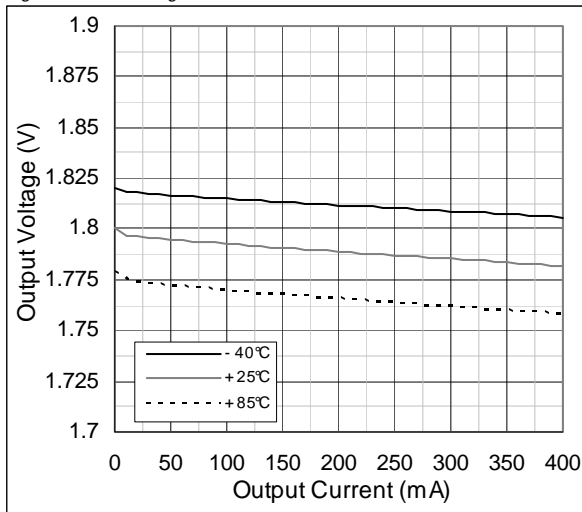


Figure 6. Quiescent Current vs. Input Voltage

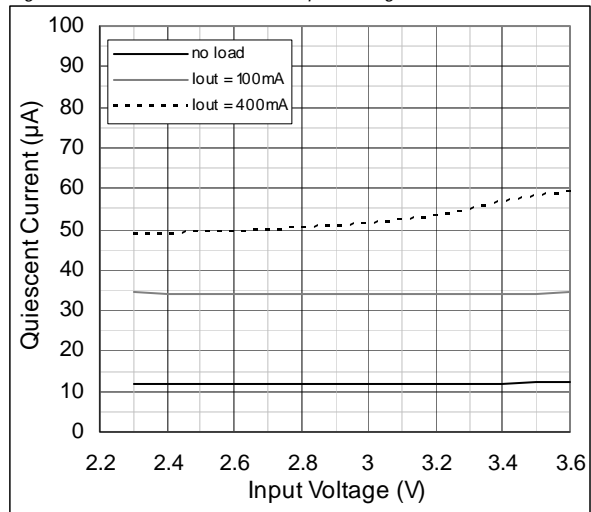


Figure 7. POK Voltage Threshold vs. Temperature

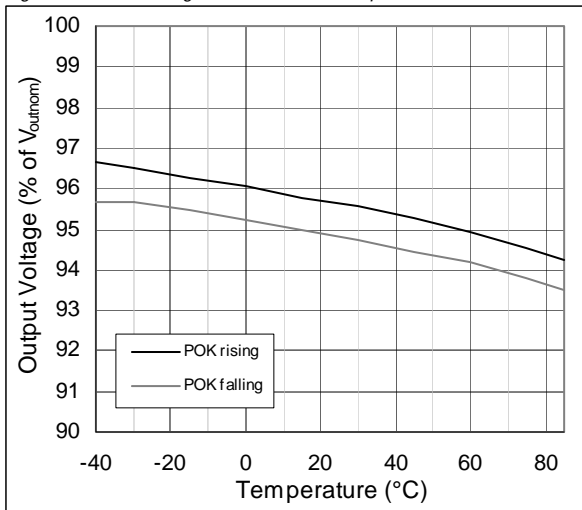


Figure 8. Dropout Voltage vs. Output Current

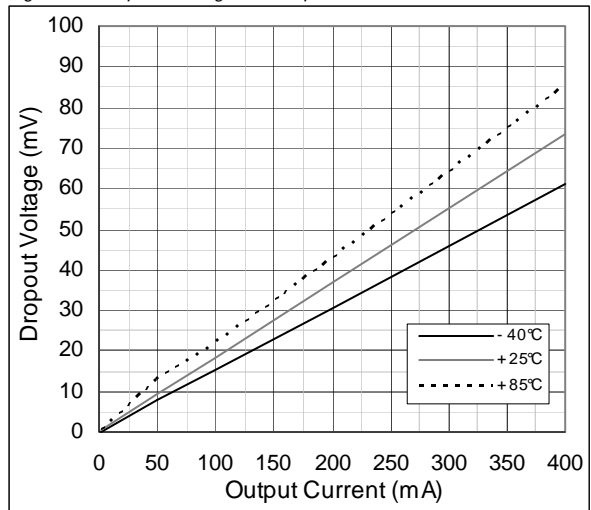


Figure 9. Line Transient Response;  $V_{IN} = 2.3V$  to  $2.8V$ , No load

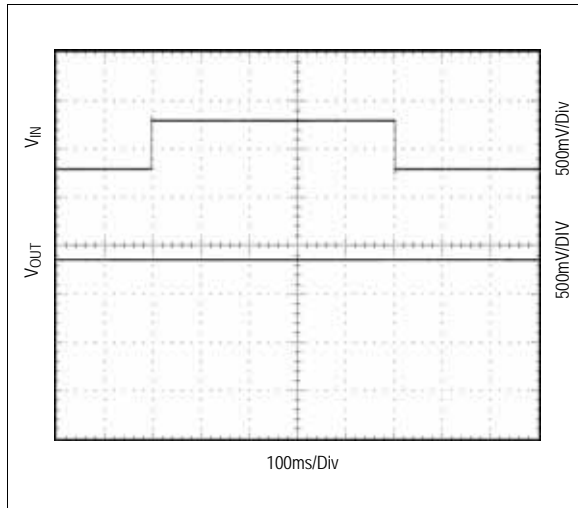


Figure 10. Load Transient Response;  $I_{OUT} = 0mA$  to  $100mA$

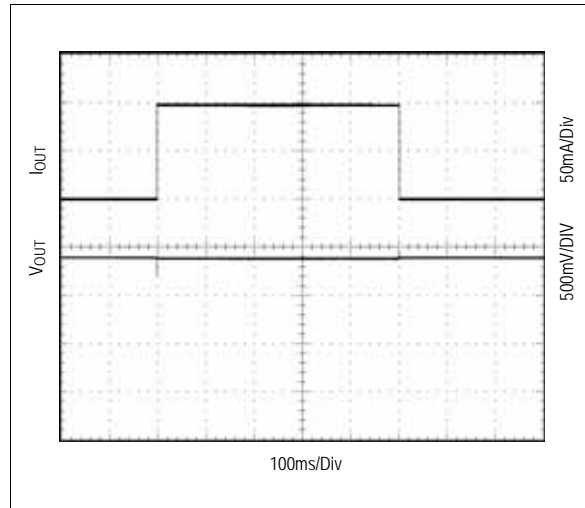


Figure 11. Turn ON

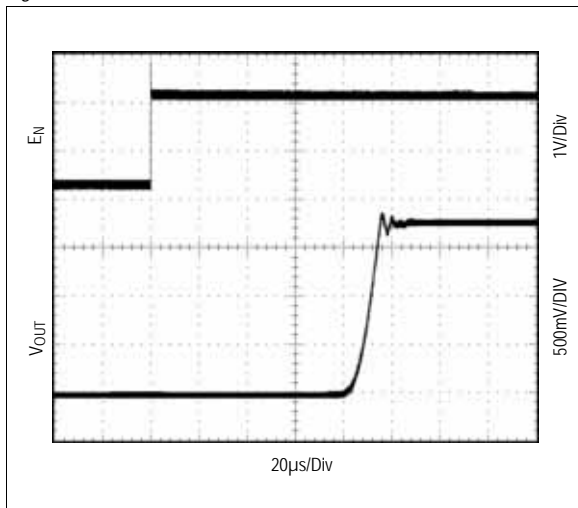
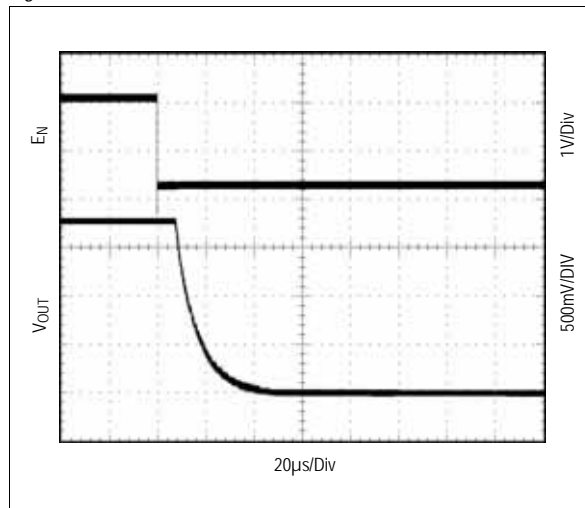


Figure 12. Turn OFF



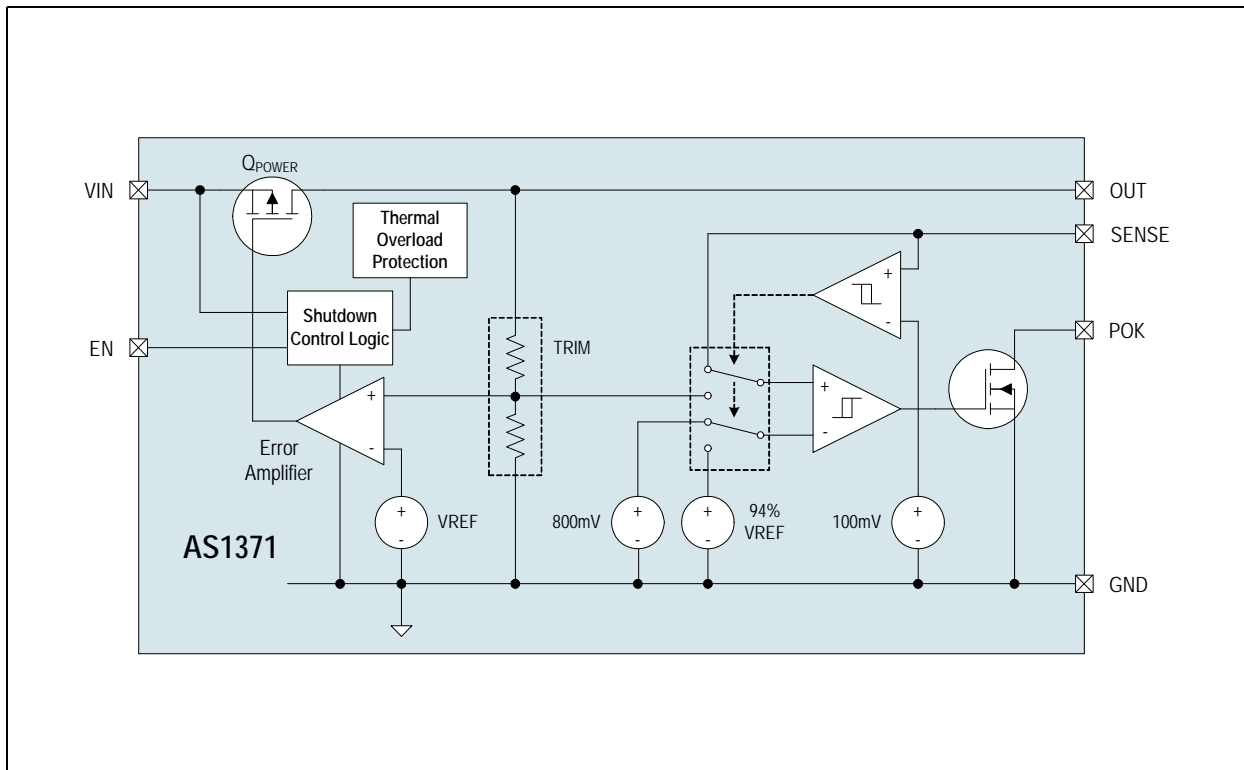
## 8 Detailed Description

The AS1371 is a low-dropout, low-quiescent-current linear regulator intended for LDO regulator applications where output current load requirements range from no load to 400mA. All devices come with fixed output voltage from 0.6V to 3.3V. See [Ordering Information on page 16](#).

The AS1371 also features a Power-OK output to indicate when the output is within 10% (max) of final value when the Enable pin is grounded. When the Enable pin is raised above ground, the POK comparator inputs are switched to change the functionality. The comparator reference is now 800mV and the Enable pin becomes an uncommitted comparator input. See [Power-OK and Low-Battery-Detect Functionality \(page 9\)](#) for setting resistor values when monitoring other voltages (i.e. VOUT). Shutdown current for the whole regulator is typically 10nA. The device features integrated short-circuit and over current protection. Under-Voltage lockout prevents erratic operation when the input voltage is slowly decaying (e.g. in a battery powered application). Thermal Protection shuts down the device when die temperature reaches 150°C. This is a useful protection when the device is under sustained short circuit conditions.

[Figure 13](#) shows the block diagram of the AS1371. It identifies the basics of a series linear regulator employing a P-Channel MOSFET as the control element. A stable voltage reference (REF in [Figure 13](#)) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-channel MOSFET, especially under transient conditions, when additional drive current is required. Input supply variations are absorbed by the series element, and output voltage variations with loading are absorbed by the low output impedance of the regulator.

Figure 13. AS1371 - Block Diagram



### 8.1 Output Voltages

Standard products are factory-set with output voltages from 0.6V to 3.3V. A two-digit suffix of the part number identifies the nominal output (see [Ordering Information on page 16](#)). Non-standard devices are available.

For more information contact: <http://www.austriamicrosystems.com/contact>

## 8.2 Power-OK and Low-Battery-Detect Functionality

The AS1371's power-ok or low-battery-detect circuitry is built around an N-channel MOSFET. The circuitry monitors the voltage on pin SENSE and if the voltage goes out of regulation (e.g. during dropout, current limit or thermal shutdown) the pin POK goes low. The pin SENSE can be connected to a resistive-divider to monitor a particular definable voltage and compare it with an internal voltage reference. If the SENSE pin is connected to GND an internal resistive-divider is activated and connected to the output. Therefore, the Power-OK functionality can be realized with no additional external components.

The Power-OK feature is not active during shutdown and provides a power-on-reset function that can operate down to  $V_{IN} = 1.2V$ . A capacitor to GND may be added to generate a power-on-reset delay. To obtain a logic-level output, connect a pull-up resistor from pin POK to pin OUT. Larger values for this resistor will help to minimize current consumption; a 100k $\Omega$  resistor is perfect for most applications (see Figure 1 on page 1).

For the circuit shown in the left of Figure 14 on page 9, the input bias current into SENSE is very low, permitting large-value resistor-divider networks while maintaining accuracy. Place the resistor-divider network as close to the device as possible. Use a defined resistor for R2 and then calculate R1 as:

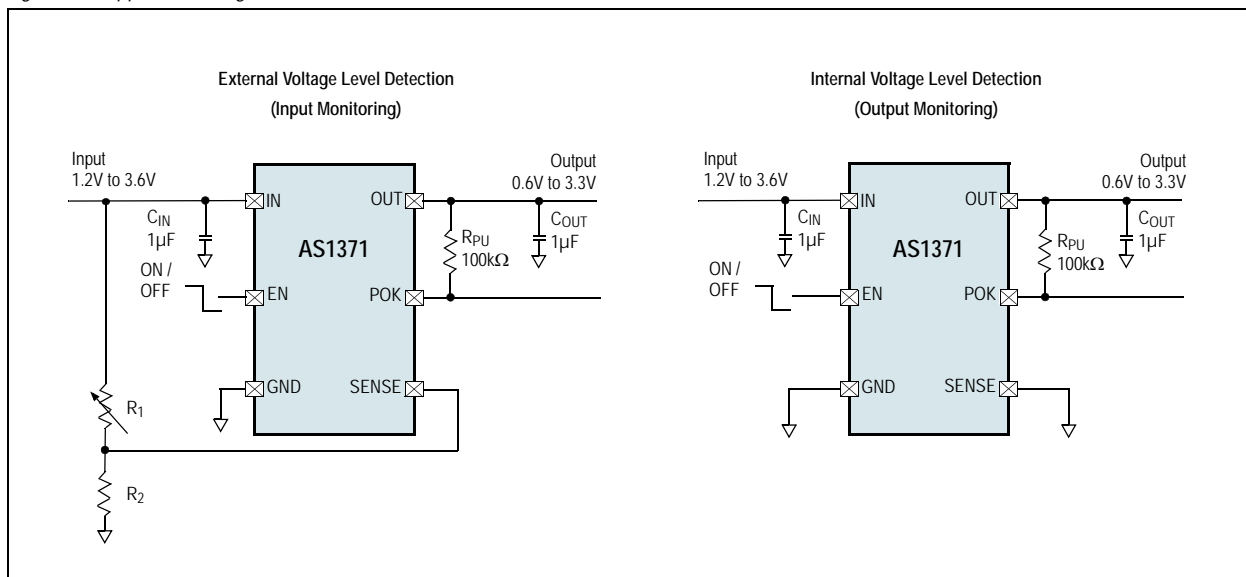
$$R_1 = R_2 \times \left( \frac{V_{IN}}{V_{SENSE}} - 1 \right) \quad (EQ 1)$$

Where:

$$V_{SENSE} = 800mV \pm 150mV.$$

In case of the SENSE pin is connected to GND, an internal resistor-divider network is activated and compares the output voltage with a 94% (typ.) voltage threshold. For this particular Power-OK application, no external resistive components are necessary.

Figure 14. Application Diagrams



## 8.3 Current Limiting

The AS1371 include current limiting circuitry to protect against short-circuit conditions. The circuitry monitors and controls the gate voltage of the P-channel MOSFET, limiting the output current to 400mA. The P-channel MOSFET output can be shorted to ground for an indefinite period of time without damaging the device.

## 8.4 Thermal-Overload Protection

The devices are protected against thermal runaway conditions by the integrated thermal sensor circuitry. Thermal shutdown is an effective instrument to prevent die overheating since the power transistor is the principle heat source in the device.

If the junction temperature exceeds 150°C with 15°C hysteresis, the thermal sensor starts the shutdown logic, at which point the P-channel MOSFET is switched off. After the device temperature has dropped by approximately 15°C, the thermal sensor will turn the P-channel MOSFET on again. Note that this will be exhibited as a pulsed output under continuous thermal-overload conditions.



## 9 Application Information

### 9.1 Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and, in particular at the regulator maximum one. From this is obtained the MOSFET maximum series resistance over temperature etc. More generally:

$$V_{DROPOUT} = I_{LOAD} \times R_{SERIES} \quad (EQ 2)$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful "end of life" of the battery before replacement or re-charge is required.

Figure 15. Graphical Representation of Dropout Voltage

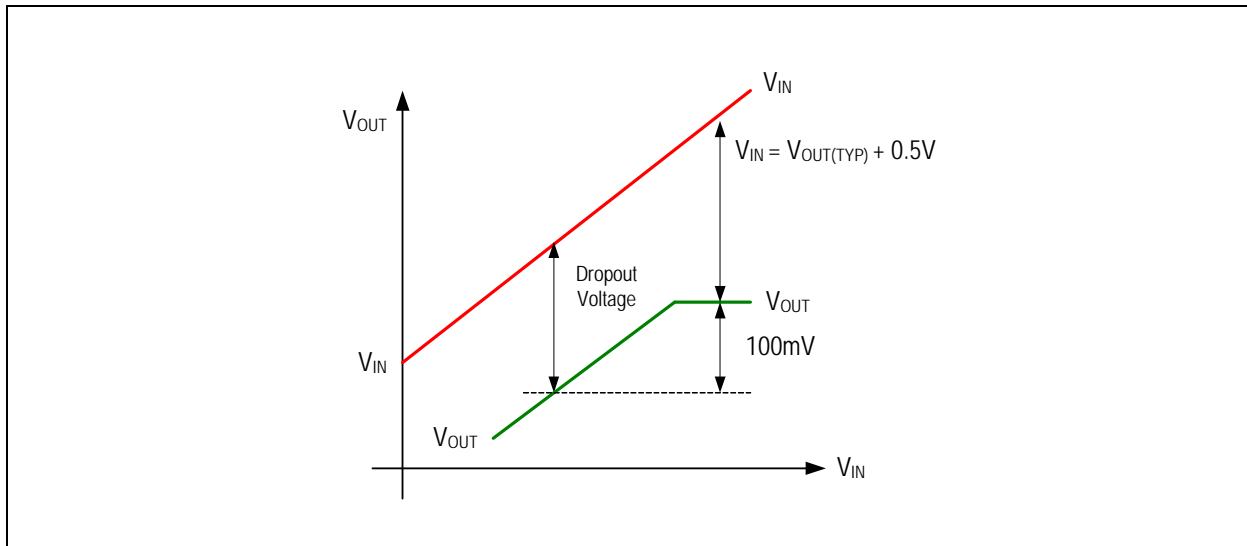


Figure 15 shows the variation of  $V_{OUT}$  as  $V_{IN}$  is varied for a certain load current. The practical value of dropout is the differential voltage ( $V_{OUT} - V_{IN}$ ) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

### 9.2 Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

$$Efficiency = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100 \% \quad (EQ 3)$$

Where:

$I_Q$  = Quiescent current of LDO

### 9.3 Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

$$PD_{(MAX)}(Seriespass) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)}) \text{ Watts} \quad (EQ 4)$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD_{(MAX)}(Bias) = V_{IN(MAX)}I_Q \text{ Watts} \quad (EQ 5)$$

Total LDO power dissipation is calculated as:

$$PD_{(MAX)}(Total) = PD_{(MAX)}(Seriespass) + PD_{(MAX)}(Bias) \text{ Watts} \quad (EQ 6)$$

## 9.4 Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125°C (unless the data sheet specifically allows). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case ( $\theta_{JC}^{\circ}\text{C}/\text{W}$  fixed by the IC manufacturer), and adjustment of the case to ambient heat path ( $\theta_{CA}^{\circ}\text{C}/\text{W}$ ) by manipulation of the PCB copper area adjacent to the IC position.

Figure 16. Package Physical Arrangements

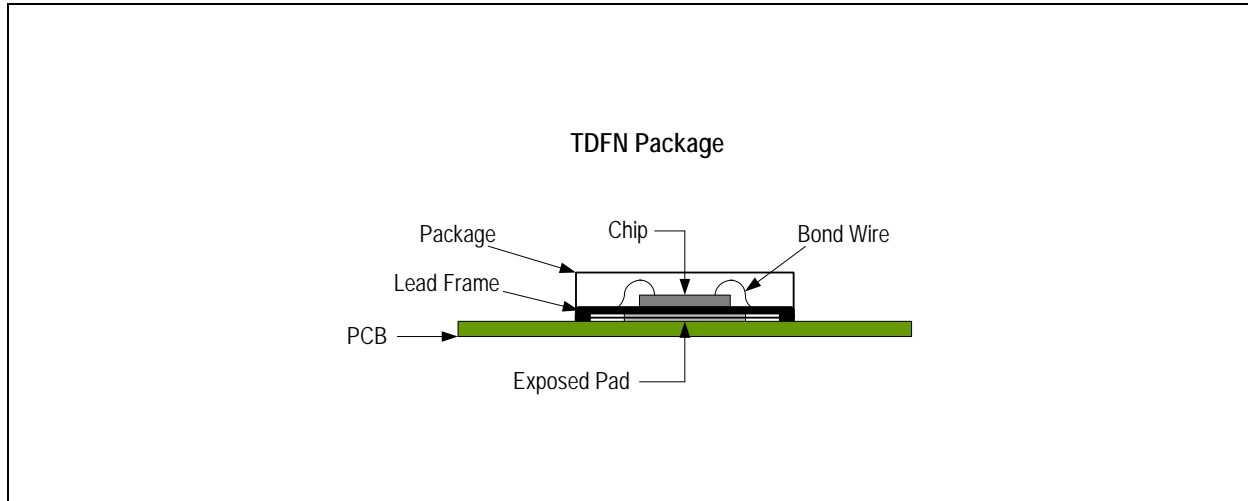
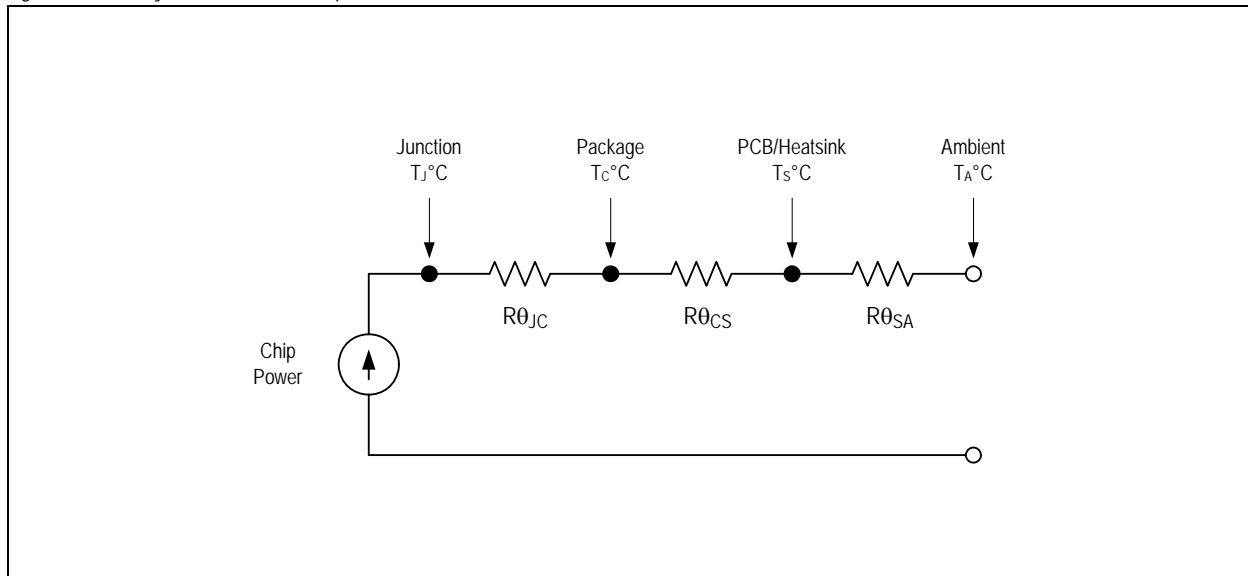


Figure 17. Steady State Heat Flow Equivalent Circuit



**Total Thermal Path Resistance:**

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA} \quad (\text{EQ } 7)$$

Junction Temperature ( $T_J^{\circ}\text{C}$ ) is determined by:

$$T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB} \text{ } ^{\circ}\text{C} \quad (\text{EQ } 8)$$

## 9.5 Explanation of Steady State Specifications

### 9.5.1 Line Regulation

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \text{ and is a pure number} \quad (\text{EQ 9})$$

In practise, line regulation is referred to the regulator output voltage in terms of % / V<sub>OUT</sub>. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \% / V \quad (\text{EQ 10})$$

### 9.5.2 Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \text{ and is units of ohms } (\Omega) \quad (\text{EQ 11})$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{\Delta V_{OUT}} \% / \text{mA} \quad (\text{EQ 12})$$

### 9.5.3 Setting Accuracy

Accuracy of the final output voltage is determined by the accuracy of the ratio of R1 and R2, the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

When the regulator has a SET or SENSE terminal, the output voltage may be adjusted externally. In this case, the tolerance of the external resistor network must be incorporated into the final accuracy calculation. Generally:

$$V_{OUT} = (V_{SET} \pm \Delta V_{SET}) \left( 1 + \frac{R1 \pm \Delta R1}{R2 \pm \Delta R2} \right) \quad (\text{EQ 13})$$

The reference tolerance is given both at 25°C and over the full operating temperature range.

### 9.5.4 Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

$$\text{Total \% Accuracy} = \text{Setting \% Accuracy} + \text{Load Regulation \%} + \text{Line Regulation \%} \quad (\text{EQ 14})$$

## 9.6 Explanation of Dynamic Specifications

### 9.6.1 Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

$$\text{PSRR} = 20 \text{Log} \frac{\delta V_{OUT}}{\delta V_{IN}} \text{ dB using lower case } \delta \text{ to indicate AC values} \quad (\text{EQ 15})$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

### 9.6.2 Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations in temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below  $T_{AMB} = -10^{\circ}\text{C}$ . With X7R or X5R capacitors, a  $1\mu\text{F}$  capacitor should be sufficient at all operating temperatures. Larger output capacitor values ( $10\mu\text{F}$ ) help to reduce noise and improve load transient-response, stability and power-supply rejection.

### 9.6.3 Input Capacitor

An input capacitor at  $V_{IN}$  is required for stability. It is recommended that a  $1.0\mu\text{F}$  capacitor be connected between the AS1371 power supply input pin  $V_{IN}$  and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the  $V_{IN}$  pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

### 9.6.4 Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems.

### 9.6.5 Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This "propagation time" is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR} \quad \text{Units are Volts, Amps, Ohms.} \quad (EQ 16)$$

Thus an initial +50mA change of output current will produce a -12mV transient when the  $ESR=240\text{m}\Omega$ . Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output of:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left( R_{ESR} + \frac{T}{C_{LOAD}} \right) \quad \text{Units are Volts, Seconds, Farads, Ohms.} \quad (EQ 17)$$

Where:

$C_{LOAD}$  is output capacitor

$T$  = Propagation delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for  $t < \text{"propagation time"}$ , so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1usec and the load cap is  $1\mu\text{F}$ .

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

### 9.6.6 Turn On Time

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at  $V_{IN}$  is stable and within the regulator min and max limits. Shutdown reduces the quiescent current to very low, mostly leakage values ( $<1\mu\text{A}$ ).

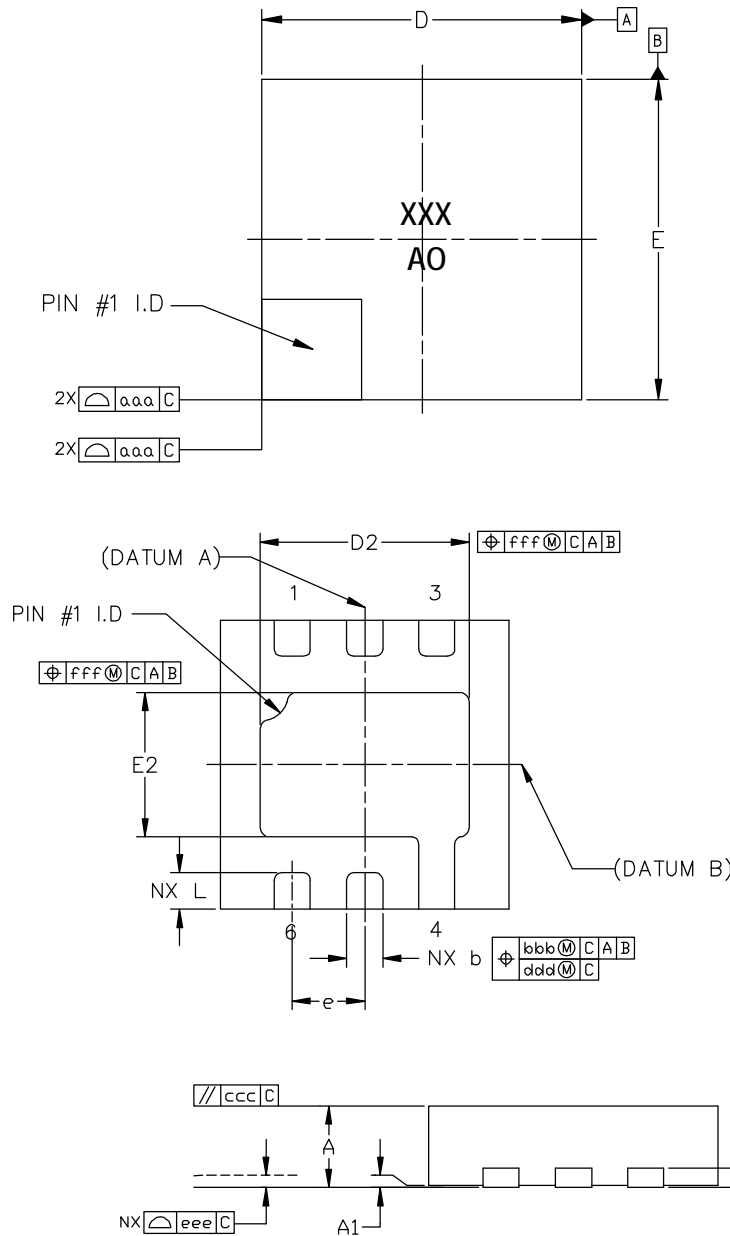
### 9.6.7 Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a  $150^{\circ}\text{C}$  threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of  $20^{\circ}\text{C}$  prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

# 10 Package Drawings and Markings

The device is available in a 6-pin 2x2 TDFN package.

Figure 18. Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.51	0.55	0.60
A1	0	0.02	0.05
A3	0.15 REF		
L	0.15	0.25	0.35
b	0.18	0.25	0.30
D	2.00 BSC		
E	2.00 BSC		
e	0.50 BSC		
D2	1.30	1.45	1.10
E2	0.85	1.00	
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N	6		



**Notes:**

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

## Revision History

Revision	Date	Owner	Description
1.5		afe	
1.6	02 Jan, 2012		Changes made across the document

**Note:** Typos may not be explicitly mentioned under revision history.

## 11 Ordering Information

The device is available as the standard products listed in [Table 4](#).

Table 4. Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1371-BTDT-105	AO	1.05V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-12 <sup>1</sup>	AM	1.2V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-15 <sup>1</sup>	AN	1.5V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-18 <sup>1</sup>	AT	1.8V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-20 <sup>1</sup>	AP	2.0V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-25 <sup>1</sup>	AQ	2.5V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-30 <sup>1</sup>	AR	3.0V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-SAMPLE <sup>1</sup>	AS	V <sub>OUT</sub> <sup>2</sup>	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN

1. Available on request.

2. Non-standard devices from 0.6V to 3.3V are available in 50mV steps.

**Note:** All products are RoHS compliant.

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