4. Functional diagram

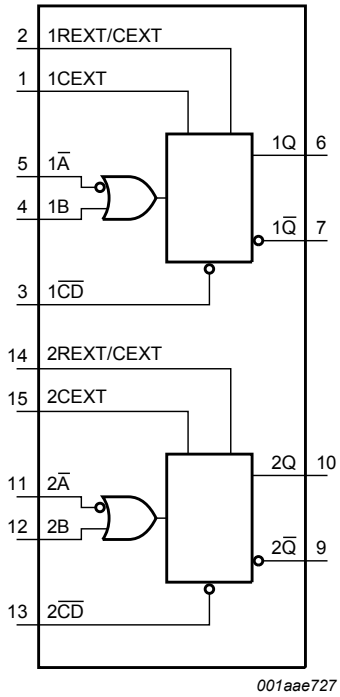


Fig. 1. Functional diagram

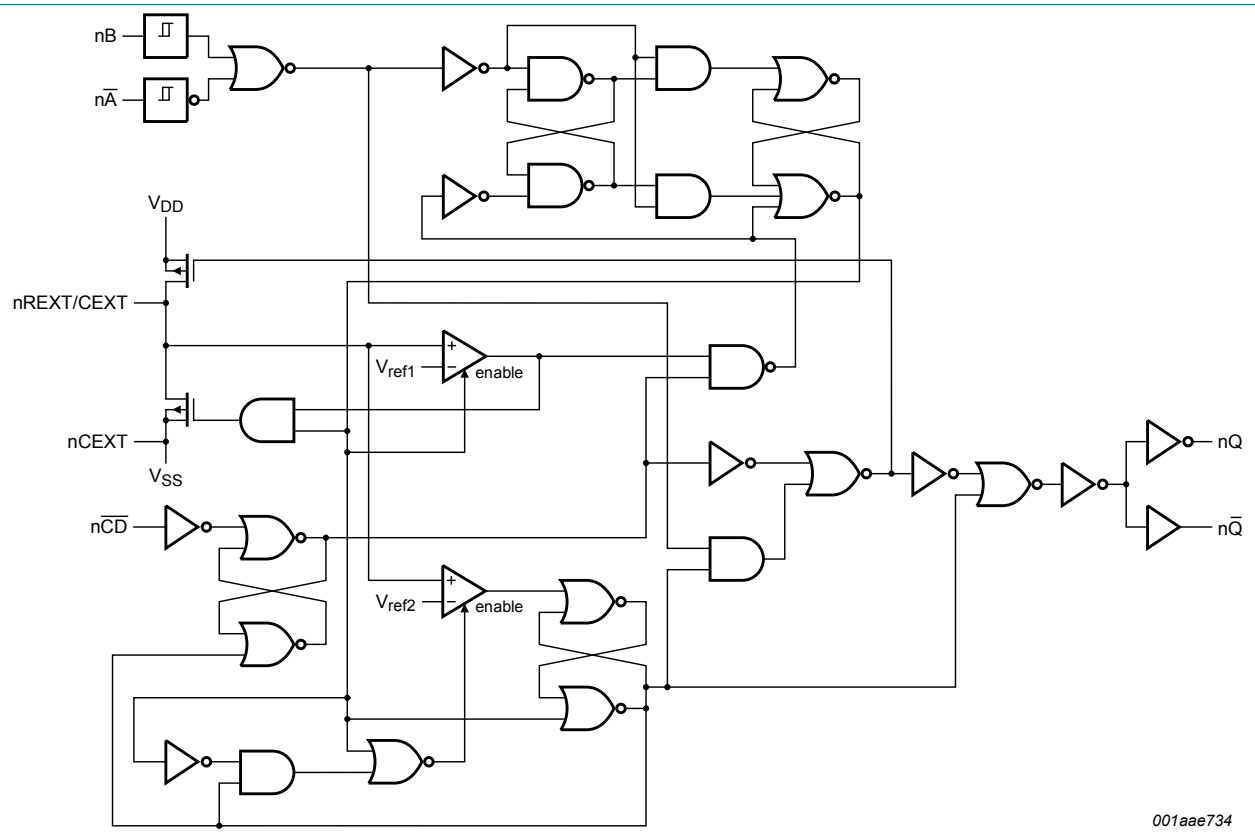


Fig. 2. Logic diagram (one multivibrator)

5. Pinning information

5.1. Pinning

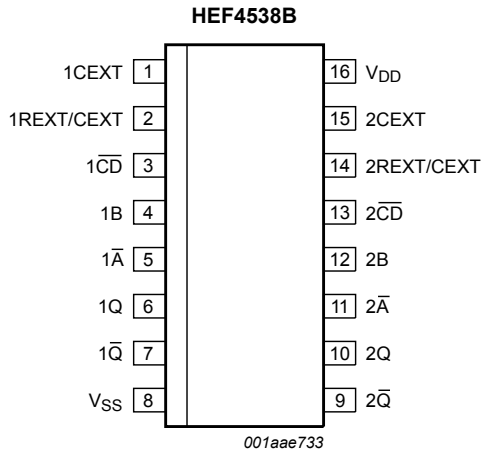


Fig. 3. Pin configuration SOT109-1 (SO16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CEXT, 2CEXT	1, 15	external capacitor connection (always connected to ground)
1REXT/CEXT, 2REXT/CEXT	2, 14	external capacitor/resistor connection
$1\overline{CD}$, $2\overline{CD}$	3, 13	direct reset input (active LOW)
1B, 2B	4, 12	input (LOW-to-HIGH triggered)
$1\overline{A}$, $2\overline{A}$	5, 11	input (HIGH-to-LOW triggered)
1Q, 2Q	6, 10	output
$1\overline{Q}$, $2\overline{Q}$	7, 9	complementary output (active LOW)
V_{SS}	8	ground supply voltage
V_{DD}	16	supply voltage

6. Functional description

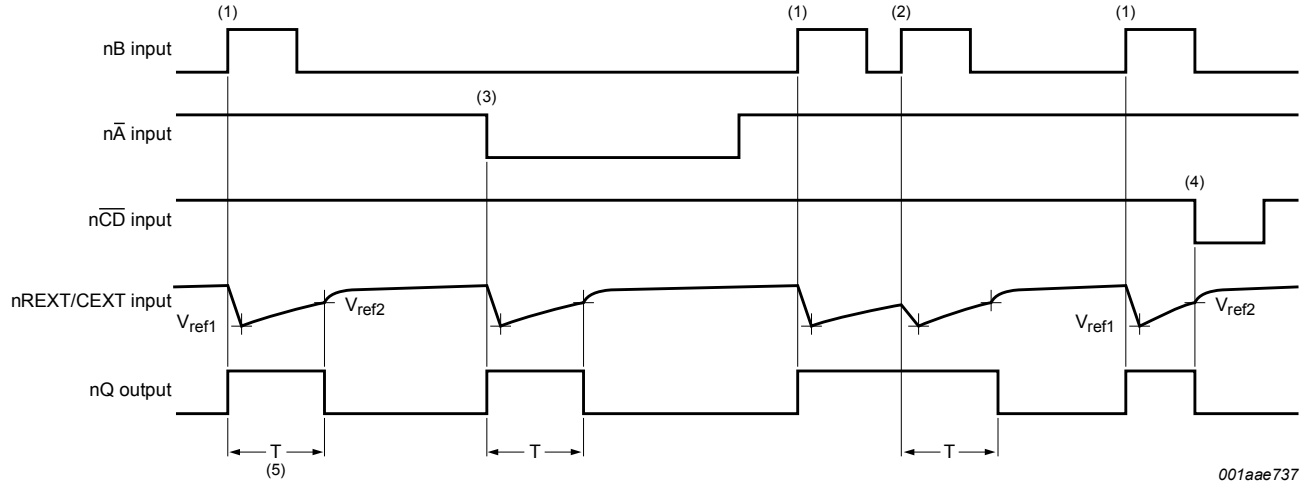
Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition;

⎍ *= one HIGH level output pulse, with the pulse width determined by C_{EXT} and R_{EXT};*

⎎ *= one LOW level output pulse, with the pulse width determined by C_{EXT} and R_{EXT}.*

Inputs			Outputs	
$n\overline{A}$	**nB**	**$n\overline{CD}$**	**nQ**	**$n\overline{Q}$**
↓	L	H	⎍	⎎
H	↑	H	⎍	⎎
X	X	L	L	H



(1) Positive edge triggering.
(2) Positive edge re-triggering (pulse lengthening).
(3) Negative edge triggering.
(4) Reset (pulse shortening).
(5) $T = R_{EXT} \times C_{EXT}$.

Fig. 4. Timing diagram

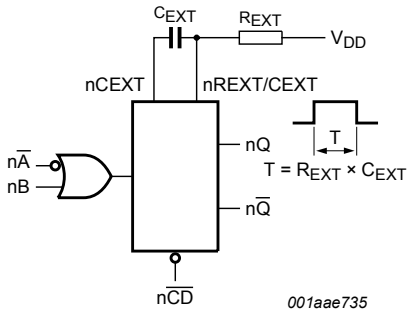


Fig. 5. Connection of the external timing components R_{EXT} and C_{EXT}

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_I < -0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	µs/V
		V_{DD} = 10 V	-	-	0.5	µs/V
		V_{DD} = 15 V	-	-	0.08	µs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		T_{amb} = 125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V_O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current	$n\bar{A}$, nB	15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	µA
		nREXT/CEXT	15 V	-	±0.3	-	±0.1	-	±1.0	-	±1.0	µA
C_I	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

Table 7. Typical static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; T_{amb} = +25 °C.

Symbol	Parameter	Conditions	V_{DD}	Typ	Unit
I_{DD}	supply current	active state	5 V [1]	55	µA
			10 V	150	µA
			15 V	220	µA
C_I	input capacitance	nREXT/CEXT	-	15	pF

[1] Only one monostable is switching: for the specified current during the output pulse (output nQ is HIGH).

10. Dynamic characteristics

Table 8. Dynamic characteristics

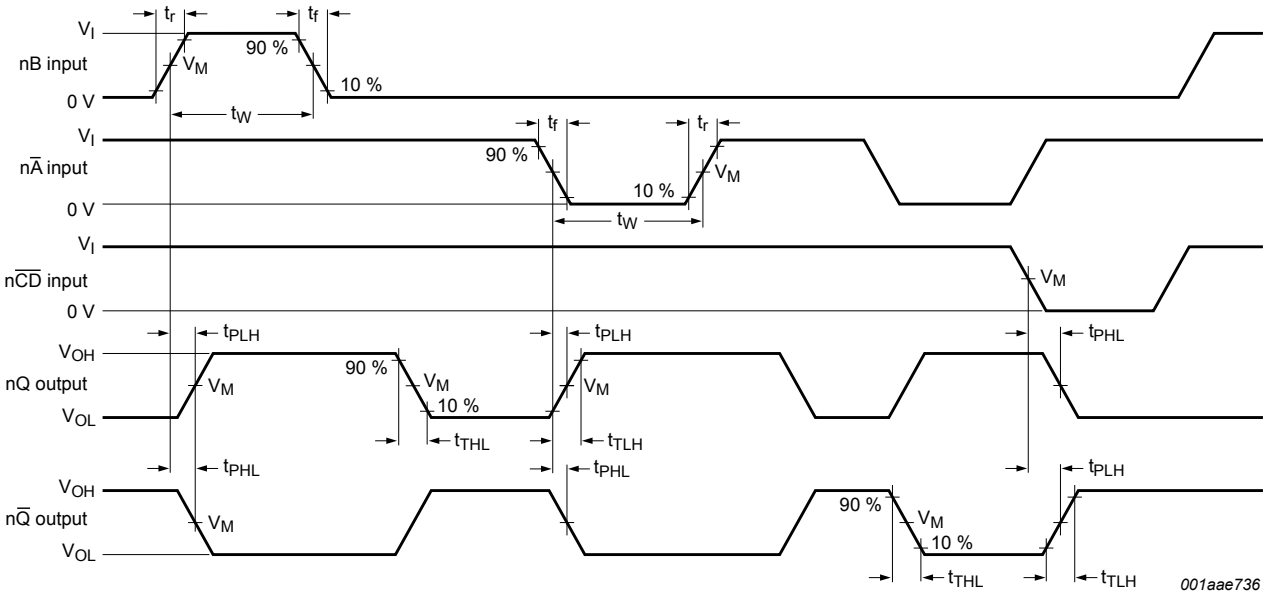
V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Fig. 11.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nA, nB to nQ; see Fig. 6	5 V	193 ns + (0.55 ns/pF) C_L	-	220	440	ns
			10 V	74 ns + (0.23 ns/pF) C_L	-	85	190	ns
			15 V	52 ns + (0.16 ns/pF) C_L	-	60	120	ns
		nCD to nQ; see Fig. 6	5 V	98 ns + (0.55 ns/pF) C_L	-	125	250	ns
			10 V	44 ns + (0.23 ns/pF) C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	80	ns
t_{PLH}	LOW to HIGH propagation delay	nA, nB to nQ; see Fig. 6	5 V	173 ns + (0.55 ns/pF) C_L	-	200	460	ns
			10 V	79 ns + (0.23 ns/pF) C_L	-	90	180	ns
			15 V	52 ns + (0.16 ns/pF) C_L	-	60	120	ns
		nCD to nQ; see Fig. 6	5 V	98 ns + (0.55 ns/pF) C_L	-	125	250	ns
			10 V	44 ns + (0.23 ns/pF) C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	80	ns
t_t	transition time	see Fig. 6	5 V [2]	10 ns + (1.00 ns/pF) C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF) C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF) C_L	-	20	40	ns
t_{rec}	recovery time	nCD to nA, nB; see Fig. 7	5 V		-	20	40	ns
			10 V		-	10	20	ns
			15 V		-	5	10	ns
t_{rtrig}	retrigger time	nQ, nQ to nA, nB; see Fig. 7	5 V		0	-	-	ns
			10 V		0	-	-	ns
			15 V		0	-	-	ns

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_W	pulse width	n$\overline{A}$ LOW; minimum width; see Fig. 7	5 V		90	45	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		nB HIGH;minimum width; see Fig. 7	5 V		50	25	-	ns
			10 V		24	12	-	ns
			15 V		20	10	-	ns
		n$\overline{CD}$ LOW; minimum width; see Fig. 7	5 V		55	25	-	ns
			10 V		25	12	-	ns
			15 V		20	10	-	ns
		nQ or n$\overline{Q}$; R_{EXT} = 100 kΩ; C_{EXT} =2.0 nF; see Fig. 7	5 V		218	230	242	µs
			10 V		213	224	235	µs
			15 V		211	223	234	µs
		nQ or n$\overline{Q}$; R_{EXT} = 100 kΩ; C_{EXT} = 0.1 µF; see Fig. 7	5 V		10.3	10.8	11.3	ms
			10 V		10.2	10.7	11.2	ms
			15 V		10.1	10.6	11.1	ms
		nQ or n$\overline{Q}$; R_{EXT} = 100 kΩ; C_{EXT} = 10 µF; see Fig. 7	5 V		1.01	1.09	1.11	s
			10 V		0.99	1.04	1.09	s
			15 V		0.99	1.04	1.09	s
Δt_W	pulse width variation	nQ or n$\overline{Q}$ variation over temperature range; see Fig. 8	5 V		-	±0.2	-	%
			10 V		-	±0.2	-	%
			15 V		-	±0.2	-	%
		nQ or n$\overline{Q}$ variation over V_{DD} voltage range 5 V to 15 V; see Fig. 9			-	±1.5	-	%
		nQ or n$\overline{Q}$ variation between monostables in the same device; R_{EXT} = 100 kΩ; C_{EXT} = 2 nF to 10 µF	5 V		-	±1	-	%
			10 V		-	±1	-	%
			15 V		-	±1	-	%
R_{EXT}	external timing resistor				5	-	[3]	kΩ
C_{EXT}	external timing capacitor				2000	-	no limits	pF

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] The maximum permissible resistance R_{EXT}, which holds the specified accuracy of t_W (nQ, n$\overline{Q}$ output), depends on the leakage current of the capacitor C_{EXT} and the leakage current of the HEF4538B.

10.1. Waveforms and test circuit



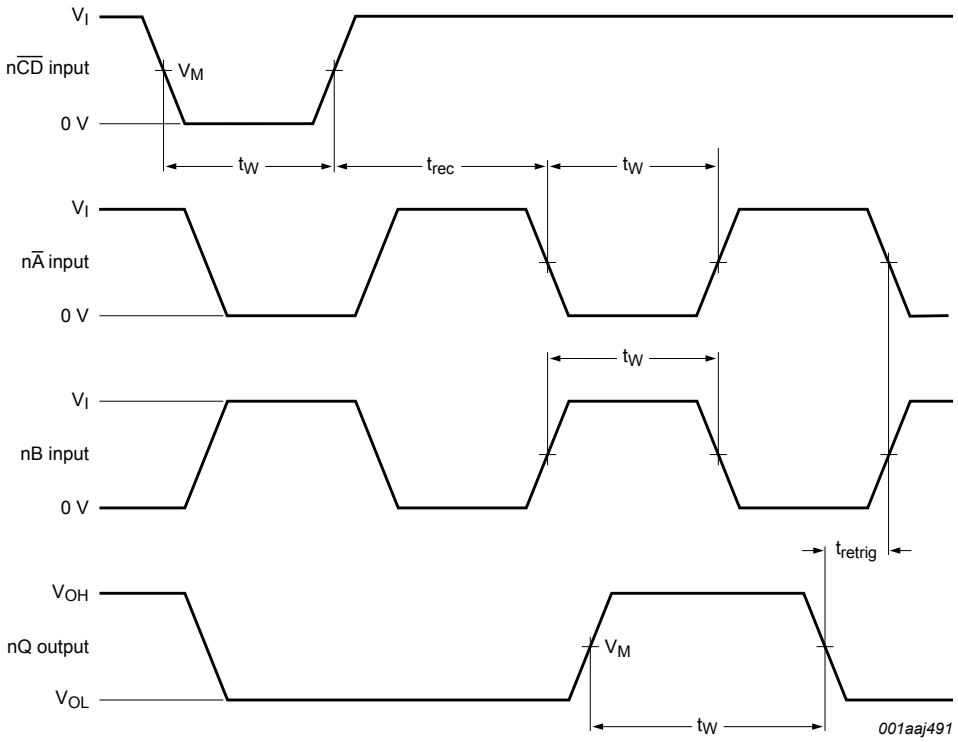
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 6. Waveforms showing propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$

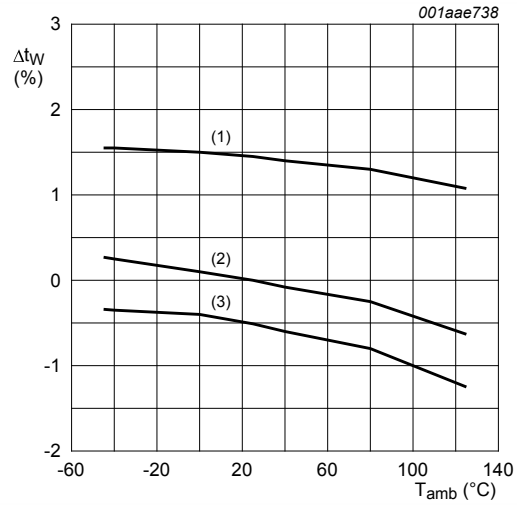


Measurement points are given in Table 9.

Recovery times are shown as positive values but may be specified as negative values.

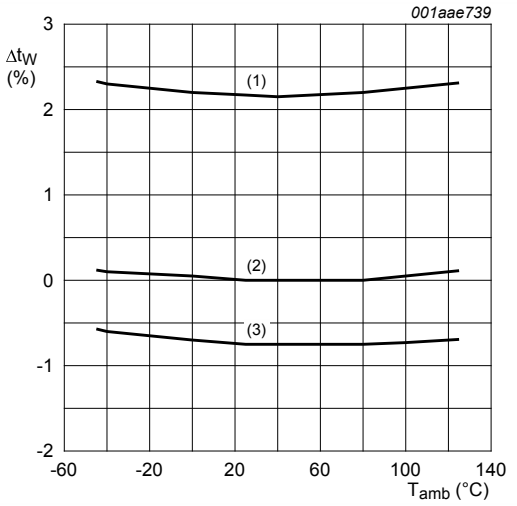
Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 7. Waveforms showing minimum nCD, nA, nB, and nQ pulse widths, recovery and retrigger times



a. R_{EXT} = 100 kΩ; C_{EXT} = 100 nF

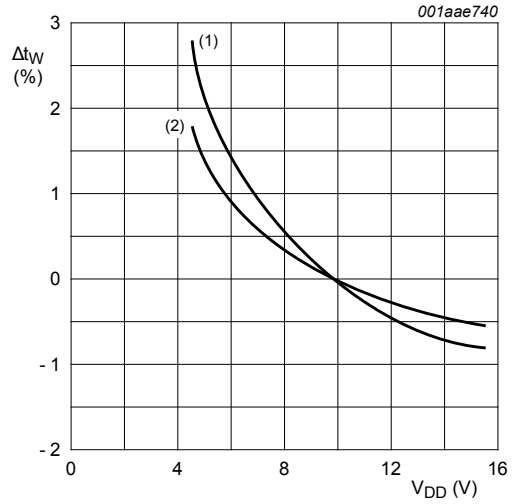
(1) V_{DD} = 5 V
(2) V_{DD} = 10 V
(3) V_{DD} = 15 V
Δt_W = 0 % at V_{DD} = 10 V and T_{amb} = 25 °C



b. R_{EXT} = 100 kΩ; C_{EXT} = 2 nF

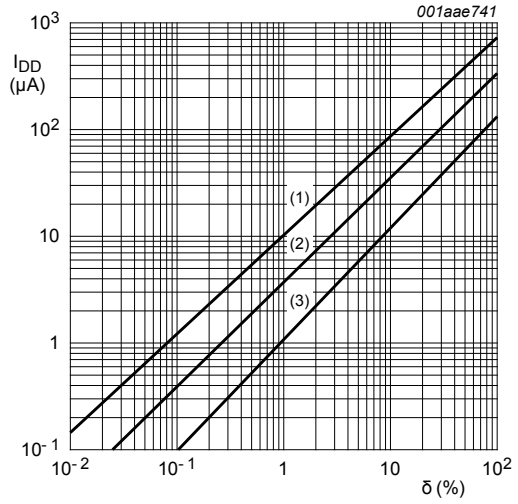
(1) V_{DD} = 5 V
(2) V_{DD} = 10 V
(3) V_{DD} = 15 V
Δt_W = 0 % at V_{DD} = 10 V and T_{amb} = 25 °C

Fig. 8. Typical normalized change in output pulse width as a function of ambient temperature



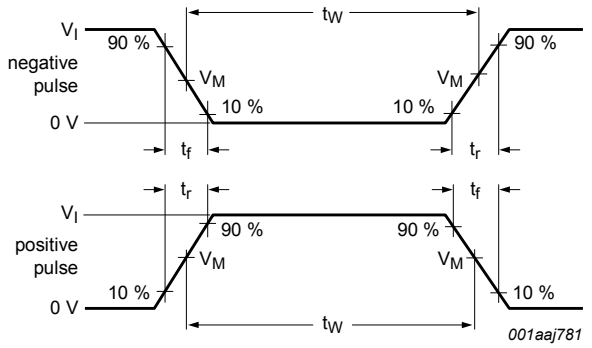
T_{amb} = 25 °C; Δt_W = 0 % at V_{DD} = 10 V; R_{EXT} = 100 kΩ
(1) C_{EXT} = 2 nF
(2) C_{EXT} = 100 nF

Fig. 9. Typical normalized change in output pulse width as a function of the supply voltage

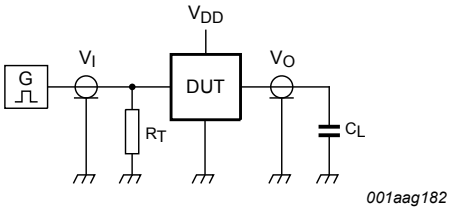


R_{EXT} = 100 kΩ; C_{EXT} = 100 nF; C_L = 50 pF; one monostable multivibrator switching only
(1) V_{DD} = 15 V
(2) V_{DD} = 10 V
(3) V_{DD} = 5 V

Fig. 10. Total supply current as a function of the output duty factor



a. Input waveforms



b. Test circuit

Test data is given in Table 10.
Definitions for test circuit:
DUT = Device Under Test.
C_L = load capacitance including jig and probe capacitance.
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

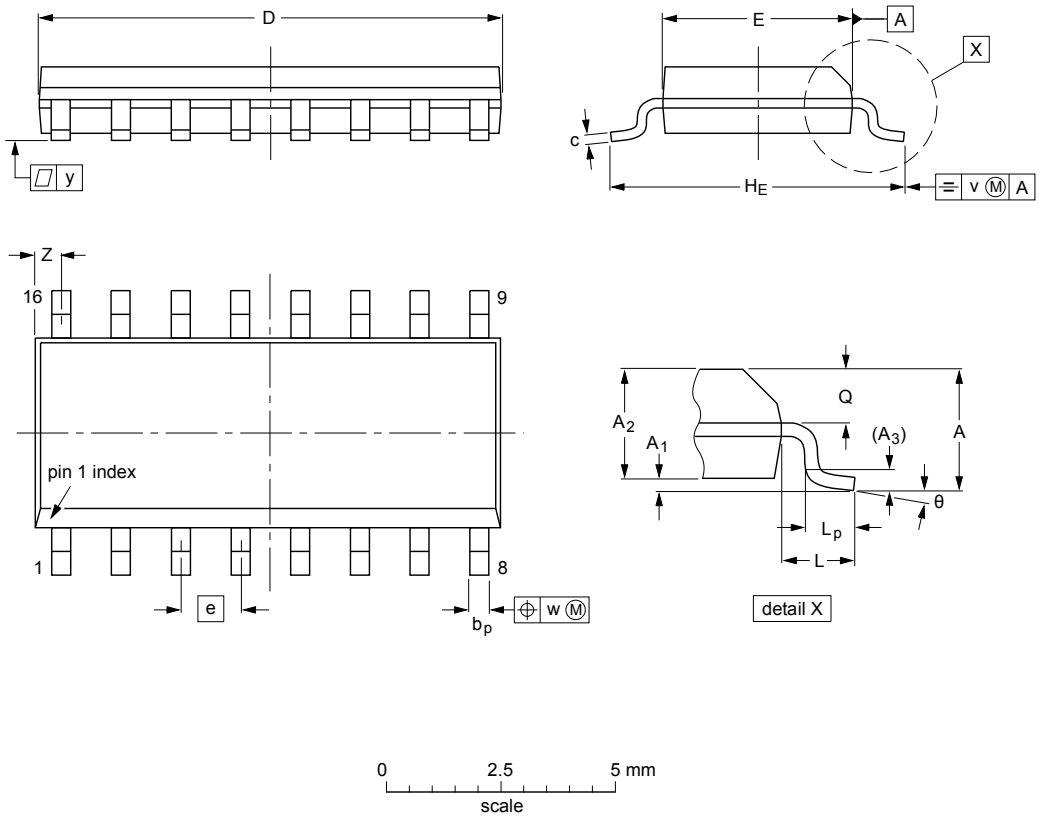
Fig. 11. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 12. Package outline SOT109-1 (SO16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4538B v.11	20181019	Product data sheet	-	HEF4538B v.10
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
HEF4538B v.10	20160401	Product data sheet	-	HEF4538B v.9
Modifications:	• Type number HEF4538BP (SOT38-4) removed.			
HEF4538B v.9	20131210	Product data sheet	-	HEF4538B v.8
Modifications:	• Fig. 8 and Fig. 9 updated to show output pulse width over full temperature range.			
HEF4538B v.8	20111116	Product data sheet	-	HEF4538B v.7
HEF4538B v.7	20110217	Product data sheet	-	HEF4538B v.6
HEF4538B v.6	20091102	Product data sheet	-	HEF4538B v.5
HEF4538B v.5	20090304	Product data sheet	-	HEF4538B v.4
HEF4538B v.4	20090206	Product data sheet	-	HEF4538B_CNV v.3
HEF4538B_CNV v.3	19950101	Product specification	-	HEF4538B_CNV v.2
HEF4538B_CNV v.2	19950101	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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