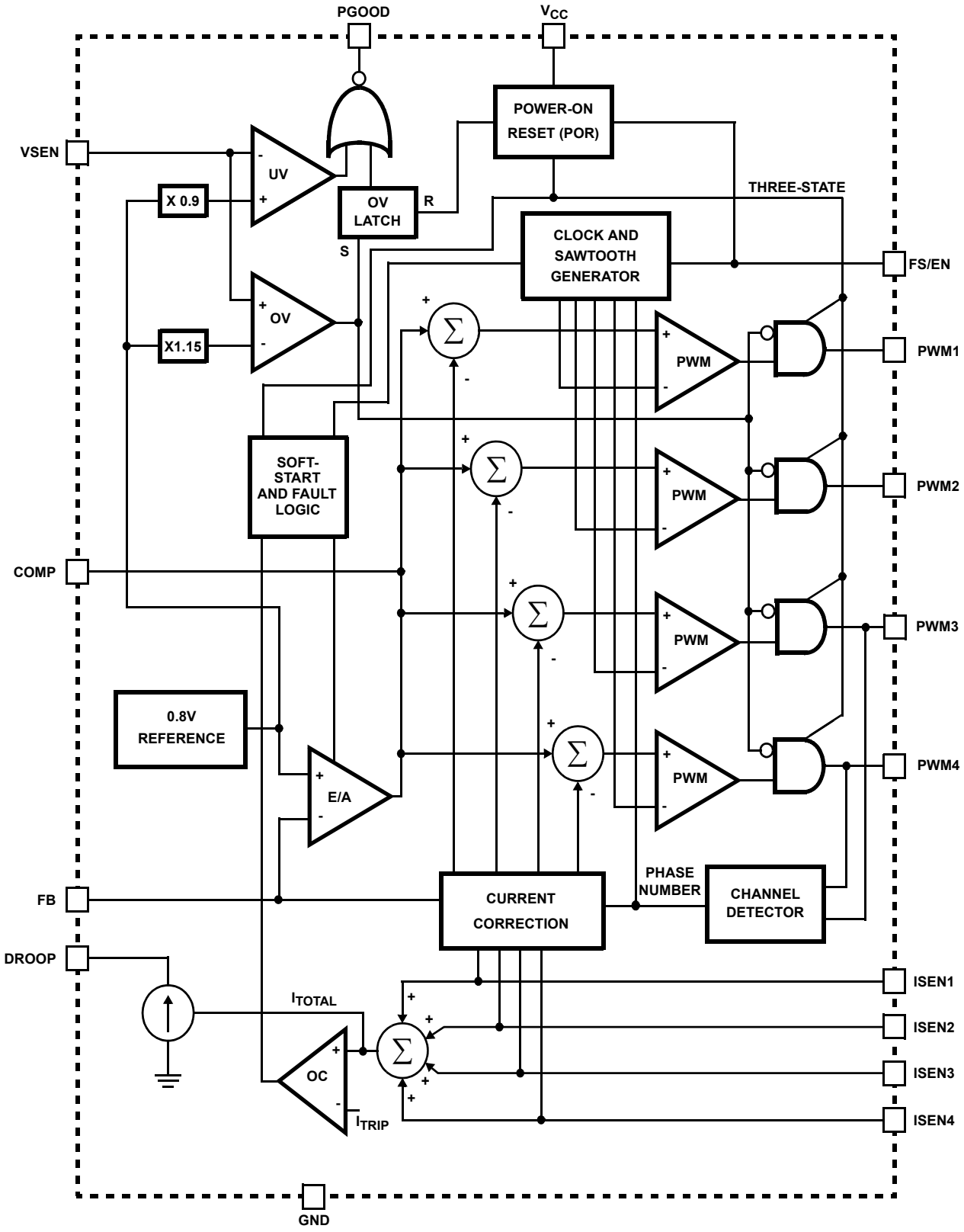
Ordering Information

PART NUMBER	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6558CBZA (Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.15
ISL6558CBZA-T (Note)	16 Ld SOIC Tape and Reel (Pb-free)		M16.15
ISL6558CRZ (Note)	0 to 70	20 Ld 5x5 QFN (Pb-free)	L20.5x5
ISL6558CRZ-T (Note)	20 Ld 5x5 QFN Tape and Reel (Pb-free)		L20.5x5
ISL6558CRZA (Note) **(No longer available, Recommended Replacement ISL6558CRZ)**	0 to 70	20 Ld 5x5 QFN (Pb-free)	L20.5x5
ISL6558CRZA-T (Note) **(No longer available, Recommended Replacement ISL6558CRZ)**	20 Ld 5x5 QFN Tape and Reel (Pb-free)		L20.5x5
ISL6558IBZ (Note) **(No longer available, Recommended Replacement ISL6558CBZA)**	-40 to 85	16 Ld SOIC (Pb-free)	M16.15
ISL6558IBZ-T (Note) **(No longer available, Recommended Replacement ISL6558CBZA)**	16 Ld SOIC Tape and Reel (Pb-free)		M16.15
ISL6558IRZ (Note)	-40 to 85	20 Ld 5x5 QFN (Pb-free)	L20.5x5
ISL6558IRZ-T (Note)	20 Ld 5x5 QFN Tape and Reel (Pb-free)		L20.5x5
ISL6558IRZA (Note)	-40 to 85	20 Ld 5x5 QFN (Pb-free)	L20.5x5
ISL6558IRZA-T (Note)	20 Ld 5x5 QFN Tape and Reel (Pb-free)		L20.5x5
ISL6558EVAL2Z	Evaluation Board		

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Functional Pin Description

NOTE: Pin numbers refer to the SOIC package. Check PINOUT diagrams for QFN pin numbers.

VCC (Pin 1)

Supplies all the power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin to a 5V (±5%) supply.

PGOOD (Pin 2)

Power good is an open drain output used to indicate the status of the output voltage. This pin is pulled low when the converter output voltage is either 10% below or 15% above the reference voltage.

COMP (Pin 3)

Output of the internal error amplifier. Connect this pin to the external feedback compensation network.

DROOP (Pin 4)

Output voltage droop or active voltage positioning is provided by connecting this pin to the FB pin. An internal current source creates the droop across an external feedback resistor, R_{FB}. If no droop is desired, this pin MUST be left open.

FB (Pin 5)

The FB pin is the inverting input of the internal error amplifier. Connect this pin to the external feedback compensation network and a resistor divider from the output for proper control and protection of converter load.

VSEN (Pin 6)

This pin is connected through a resistor divider to the converter's output voltage to provide remote sensing. The undervoltage and overvoltage protection comparators trigger off this input.

FS/EN (Pin 7)

Connecting a resistor from this pin to ground sets the internal oscillator frequency. The switching frequency, F_{SW}, of the converter is adjustable between 80kHz and 1.5MHz. Pulling this pin to ground disables the converter and three-states the PWM outputs.

GND (Pin 8)

Bias and reference ground for all controller signals.

PWM1 (Pin 13), PWM2 (Pin 12), PWM3 (Pin 9), PWM4 (Pin 16)

The controller PWM drive signals are connected to the individual HIP660x driver PWM input pins. The number of active channels is determined by the state of PWM3 and PWM4. If PWM3 is tied to VCC, this indicates to the controller that two channel operation is desired. In this case, PWM4 should be left open or tied to VCC. Tying PWM4 to VCC indicates that three channel operation is desired.

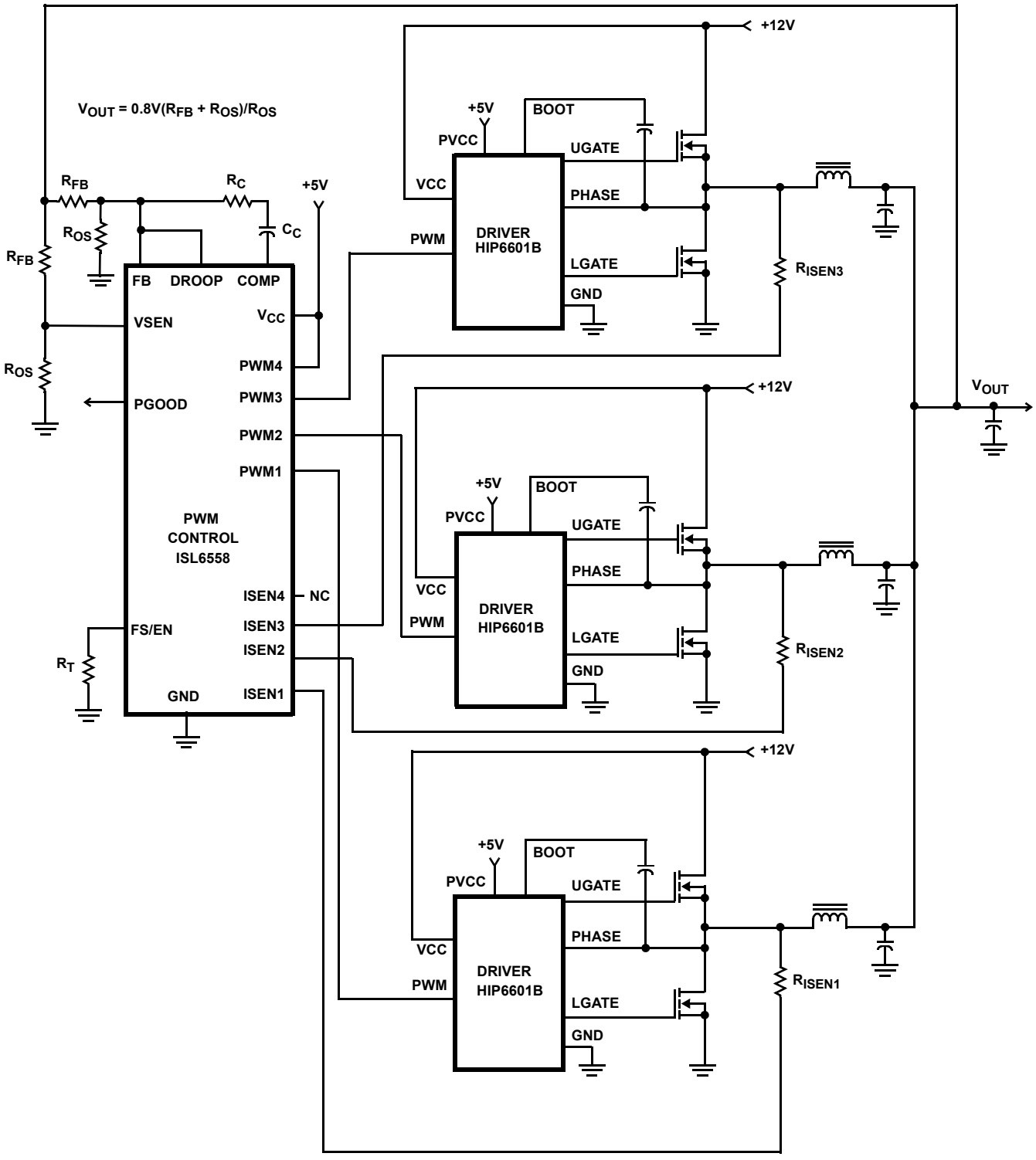
ISEN1 (Pin 14), ISEN2 (Pin 11), ISEN3 (Pin 10), ISEN4 (Pin 15)

These pins are used to monitor the voltage drop across the lower MOSFETs for current feedback, output voltage droop and overcurrent protection. A resistor must be placed in series with each of these inputs and their respective PHASE node. The resistor is sized such that the current feedback is 50µA at full load. Sense lines corresponding to inactive channels should be left open. Inactive channels are those in which the PWM pin has been tied to VCC or left open.

Thermal Pad (in QFN only)

In the QFN package, the pad underneath the center of the IC is a thermal substrate. The PCB "thermal land" design for this exposed die pad should include thermal vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the QFN to achieve its full thermal potential. This pad should be either grounded or floating, and it should not be connected to other nodes. Refer to TB389 for design guidelines.

Typical Application - 3 Phase Converter



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . +7V
Input, Output, or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification
Human Body Model 3kV
Machine Model 250V

Recommended Operating Conditions

Supply Voltage . . . . . +5V ±5%
Ambient Temperature . . . . . -40°C to 85°C
Maximum Operating Junction Temperature . . . . . 125°C

Thermal Information

Thermal Resistance (Typical Notes 1, 2, 3)	θ_{JA}(°C/W)	θ_{JC}(°C/W)
SOIC Package (Note 1)	70	N/A
QFN Package (Notes 2, 3)	35	5

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
3. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{CC} = 5V, T_A = -40°C to 85°C. Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY POWER					
Input Supply Current	VCC = 5VDC; R_T = 100kΩ ±1%	-	10	15	mA
POWER-ON RESET (POR)					
VCC Rising Threshold		4.25	4.38	4.5	V
VCC Falling Threshold		3.75	3.88	4.00	V
REFERENCE VOLTAGE					
Reference Voltage	ISL6558CB, ISL6558CR, T_A = 0°C to 70°C	0.792	0.8	0.808	V
	ISL6558IB, ISL6558IR, T_A = -40°C to 85°C	0.788	0.8	0.812	V
System Accuracy	ISL6558CB, ISL6558CR, T_A = 0°C to 70°C	-1.0	-	1.0	%
	ISL6558IB, ISL6558IR, T_A = -40°C to 85°C	-1.5	-	1.5	%
OSCILLATOR					
Channel Frequency Accuracy	R_T = 100kΩ. ±1%	224	280	336	kHz
Adjustment Range	See Figure 3	0.08	-	1.5	MHz
Disable Voltage	Maximum voltage at FS/EN to disable controller. $I_{FS/EN}$ = 1mA	-	1.2	1.0	V
Sawtooth Amplitude		-	1.33	-	V_{P-P}
Channel Maximum Duty Cycle, by Design (GBD)		-	75	-	%
ERROR AMPLIFIER					
DC Gain (GNT)	R_L = 10K to ground	-	72	-	dB
Gain-Bandwidth Product (GNT)	C_L = 100pF, R_L = 10K to ground	-	18	-	MHz
Slew Rate	C_L = 100pF, Load = ±400µA	-	5.3	-	V/µs
Maximum Output Voltage	R_L = 10K to ground	3.6	4.1	-	V
ISEN					
Recommended Full Scale Input Current		-	50	-	µA
Overcurrent Trip Level		67	-	85	µA

Electrical Specifications Operating Conditions: V_{CC} = 5V, T_A = -40°C to 85°C. Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER GOOD MONITOR					
Undervoltage Threshold	VSEN Rising	-	0.92	-	V_{REF}
Undervoltage Threshold	VSEN Falling	-	0.90	-	V_{REF}
PGOOD Low Output Voltage	I_{PGOOD} = 4mA	-	0.18	0.4	V
PROTECTION					
Overvoltage Threshold	VSEN Rising, ISL6558CB, ISL6558CR, T_A = 0°C to 70°C	1.12	1.15	1.2	V_{REF}
	VSEN Rising, ISL6558IB, ISL6558IR, T_A = -40°C to 85°C	1.085	1.15	1.2	V_{REF}
Percent Overvoltage Hysteresis (GNT)	VSEN Falling after Overvoltage	-	2	-	%

GBD = Guaranteed By Design
GNT = Guranteed Not Tesed

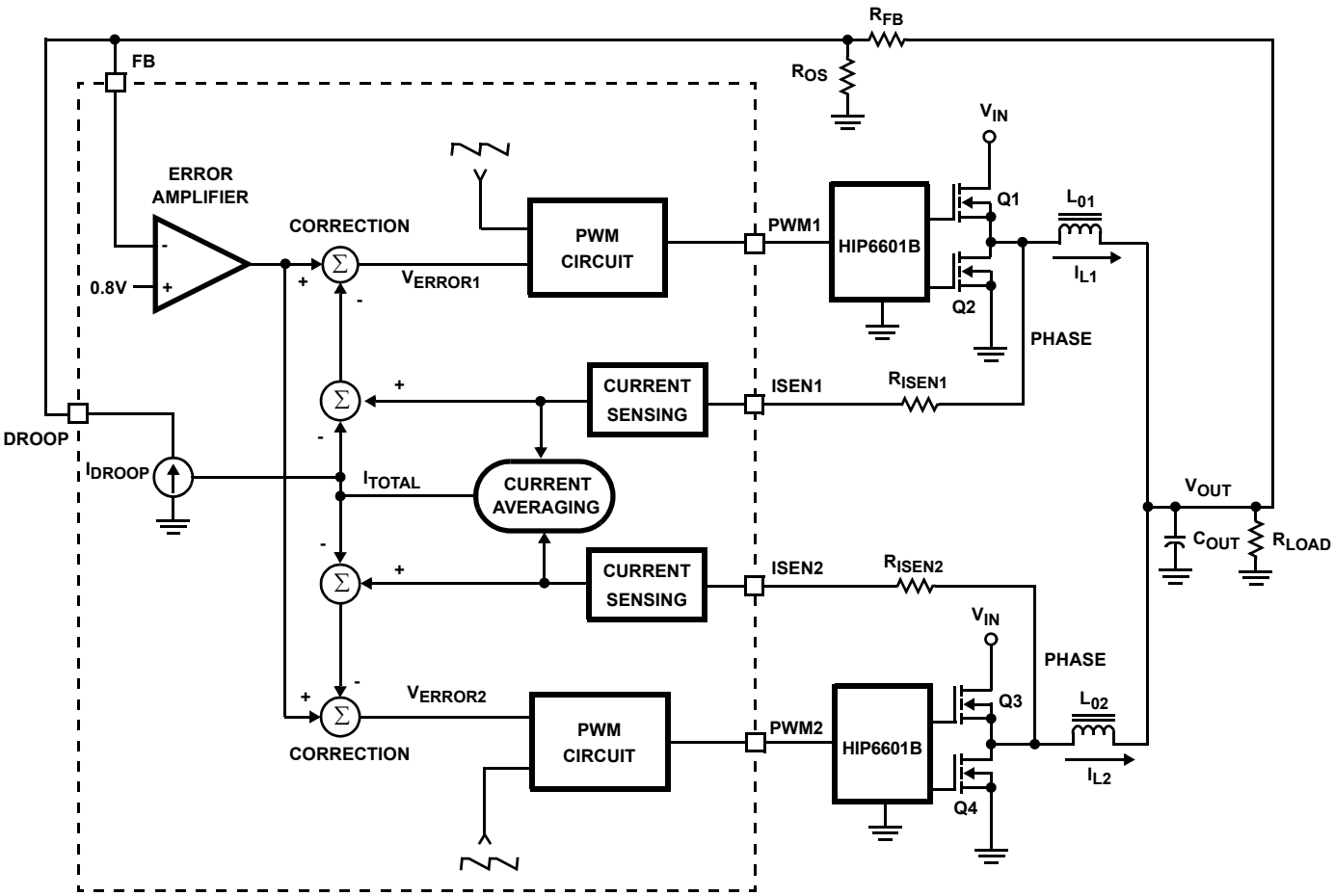


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF THE ISL6558 VOLTAGE AND CURRENT CONTROL LOOPS CONFIGURED FOR A TWO CHANNEL CONVERTER

Operation

Figure 1 shows a simplified diagram of the voltage regulation and current control loops for a two-phase converter. Both voltage and current feedback are used to precisely regulate output voltage and tightly control phase currents, I_{L1} and I_{L2}, of the two power channels.

Voltage Loop

Output voltage feedback is applied via the resistor combination of R_{FB} and R_{OS} to the inverting input of the error amplifier. This signal drives the error amplifier output high or low, depending upon the scaled output voltage in relation to the reference voltage of 0.8V. The amplifier output voltage is distributed among the active PWM channels and summed with their individual current correction signals. The resultant signal, V_{ERROR}, is fed into the PWM control circuitry for each channel. Within this block, the signal is compared with a sawtooth ramp signal. The sawtooth ramp signal applied to each channel is out-of-phase with the others. The resulting duty cycle signal for each channel is determined by the movement of the correction voltage, V_{ERROR}, relative to the sawtooth ramp. The individual duty cycle signals are sent to their respective HIP660x gate drivers from the PWM pins. The HIP660x gate drivers then switch their upper and lower MOSFETs in accordance to this PWM signal.

Current Loop

The current control loop keeps the channel currents in balance. During the PWM off-time of each channel, the voltage developed across the $r_{DS(ON)}$ of the lower MOSFET is sampled. The current is scaled by the R_{ISEN} resistor and provides feedback proportional to the output current of each channel. The scaled output current from all active channels are combined to create an average current reference, I_{TOTAL}, relative to the converter's total output current. This signal is then subtracted from the individual channel scaled output currents to produce a current correction signal for each channel. The current correction signal keeps each channel's output current contribution balanced relative to the other active channels. Each current correction signal is then subtracted from the error amplifier output and fed to the individual channel PWM circuits.

For example, assume the voltage sampled across Q4 in Figure 1 is higher than that sampled across Q2. The ISEN2 current would be higher then ISEN1. When the two reference currents are averaged, they still accurately represent the total output current of the converter. The reference current I_{TOTAL} is then subtracted from the ISEN currents. This results in a positive offset for Channel 2 and a negative offset for Channel 1. These offsets are subtracted from the error amplifier signal and perform phase balance correction. The V_{ERROR2} signal is reduced, while V_{ERROR1} would be increased. The PWM circuit would then reduce the pulse width to lower the output current contribution by Channel 2, while doing the opposite to Channel 1.

Droop Compensation

Microprocessors and other peripherals tend to change their load current demands often from near no-load to full load during operation. These same devices require minimal output voltage deviation from nominal during a load step.

A high di/dt load step will cause an output voltage spike. The amplitude of the spike is dictated by the output capacitor ESR (effective series resistance) multiplied by the load step magnitude and output capacitor ESL (equivalent series inductance) times the load step di/dt. A positive load step produces a negative output voltage spike and visa versa. The overall output voltage deviation could exceed the tolerance of some devices. One widely accepted solution to this problem is output voltage "droop" or active voltage positioning.

Droop is set relative to the output voltage tolerance specifications of the load device. Most device tolerance specifications straddle the nominal output voltage. At no-load, the output voltage is set to a slightly higher than nominal level, $V_{OUT,NL}$. At full load, the output voltage is set to a slightly lower than nominal level, $V_{OUT,FL}$. The result is a desire to have an output voltage characteristic as shown by the load line in Figure 2.

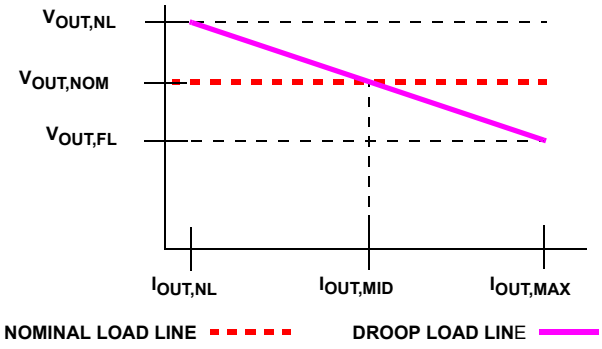


FIGURE 2. SIMPLE OUTPUT DEVICE LOAD LINE

With droop implemented and a positive load step, the resulting negative output voltage spike begins from the slightly elevated level of $V_{OUT,NL}$. Similarly, if the load steps from full load, $I_{OUT,MAX}$, back to no-load, $I_{OUT,NL}$, the output voltage starts from the slightly lower $V_{OUT,FL}$ position. These few millivolts of offset help reduce the size and cost of output capacitors required to handle a given load step.

Droop is an optional feature of the ISL6558. It is implemented by connecting the DROOP and FB pins as shown in Figure 1. An internal current source, I_{DROOP}, feeds out of the DROOP pin. The magnitude of I_{DROOP} is controlled by the scaled representation of the total output current created from the individual ISEN currents. I_{DROOP} creates a voltage drop across R_{FB} and offsets the output

voltage feedback seen at the FB pin, effectively creating the output voltage droop desired as a function of load current.

SELECTING R_{FB} AND R_{OS}

If output droop compensation is not required the DROOP pin must be left open. Simply select a value for R_{FB} and calculate R_{OS} based on the following equation:

$$R_{OS} = R_{FB} x \frac{0.8V}{V_{OUT} - 0.8V} \quad \text{(EQ. 1)}$$

In applications where droop compensation is desired, tie the DROOP and FB pins together. Select R_{FB} first given the following equation, where V_{DROOP} is the desired amount of output voltage droop at full load. This equation is contingent upon the correct selection of the ISEN resistors discussed in the *Fault Protection* section.

$$R_{FB} = \frac{V_{DROOP}}{50\mu A} = 20 \times 10^3 x V_{DROOP} \quad \text{(EQ. 2)}$$

Calculate R_{OS} based on R_{FB} using the following equation. Where $V_{OUT,NL}$ is the desired output voltage under no-load conditions.

$$R_{OS} = R_{FB} x \frac{0.8V}{V_{OUT,NL} - 0.8V} \quad \text{(EQ. 3)}$$

Initialization

Many functions are initiated by a rising supply voltage applied to the VCC pin of the ISL6558. Until the supply voltage reaches the Power-On Reset (POR) VCC rising threshold, the PWM drive signals are held in three-state. This results in no gate drive generation by the HIP660x gate drivers to the output MOSFETs. Once the supply voltage exceeds the POR rising threshold, the soft-start interval is initiated. If the supply voltage drops below the POR falling threshold, POR shutdown is triggered and the PWM outputs are again driven to three-state.

The FS/EN pin can also be used to initialize the converter. Holding this pin to ground overrides the onset of soft-start. Once this pin is released, soft-start is initialized and the converter output will begin to ramp. If FS/EN is grounded during operation, a POR shutdown is triggered and the PWM outputs are three-stated. Toggling this pin after an overvoltage event will not reset the controller; V_{CC} must be cycled.

Sequencing of the input supplies is recommended. An overcurrent spike due to supply voltage sequencing could occur if the controller becomes active before the drivers. If the POR rising threshold of the controller is met before that of the drivers, then a soft-start interval is started and could be completed before the drivers are active. Once the drivers become active the controller will be demanding maximum duty cycle due to the lack of output voltage and could cause an overcurrent trip. A soft-start interval would be initiated shortly after this event and normal PWM operation would result. The supply voltages should be sequenced such that the controller and gate drivers are initialized simultaneously or the drivers become active just before the controller. Most ATX supplies control the rise times of the individual voltage outputs and insure proper sequencing.

Soft-Start Interval

Before a soft-start cycle is initiated, the controller holds the active channel PWM drive signals in three-state as long as the FS/EN pin is held at ground or the voltage applied to VCC remains below the POR rising threshold.

Once VCC rises above the POR rising threshold and the FS/EN pin is released from ground, a soft-start interval is initiated. PWM operation begins and the resulting slow ramp-up of output voltage avoids hitting an overcurrent trip by slowly charging the discharged output capacitors. The soft-start interval ends when the PGOOD signal transitions to indicate the output voltage is within specification.

The soft-start interval is digitally controlled by the selection of switching frequency. The maximum soft-start interval, $SS_{Interval}$, can be estimated for a given application:

$$SS_{Interval} = \frac{2048}{F_{SW}} \quad \text{(EQ. 4)}$$

where F_{SW} is the channel switching frequency.

The converter used to create the waveforms in Figure 3 has a switching frequency of 125kHz. The soft-start interval calculated for this converter is just over 16ms. From the waveforms, the actual soft-start interval is just under 16ms.

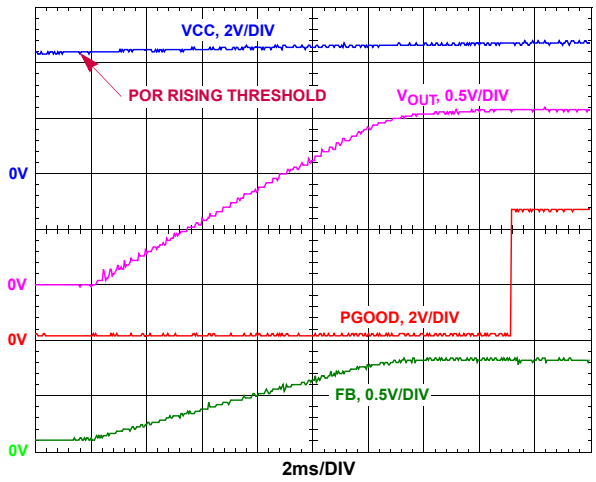


FIGURE 3. SOFT-START WAVEFORMS

PWM Drive Signals

The ISL6558 provides PWM channel drive signals for control of 2-, 3-, or 4-phase converters. The PWM signals drive the associated HIP660x gate drivers for each power channel. The number of active channels is determined by the status of PWM3 and PWM4. If PWM3 is tied to VCC, then the controller will interpret this as two channel operation and only PWM1 and PWM2 will be active. Since PWM4 is not active under these conditions, simply tie it to VCC or leave it open. If only PWM4 is tied to VCC, then the remaining three channels are all considered active by the controller.

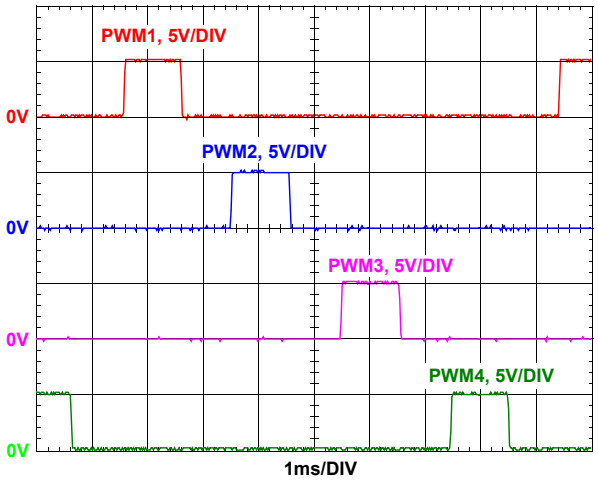


FIGURE 4. FOUR ACTIVE CHANNEL PWM DRIVE SIGNALS

The PWM drive signals are switched out of phase. The PWM drive signal phase relationship is 360° divided by the number of active channels. Figure shows the PWM drive signals for a four channel converter running at 125kHz. Each PWM drive signal is 90° out of phase with the other.

Frequency Setting

A resistor, R_T, connected between the FS/EN pin and ground sets the frequency of the internal oscillator. Tying the FS/EN pin to ground disables the oscillator, thus shutting down the converter. The resistor can be calculated given the desired channel switching frequency, F_{SW}.

$$R_T = 10^{10.9 - 1.1\log F_{SW}} \quad \text{(EQ. 5)}$$

Figure 5 provides a graph of oscillator frequency vs R_T. The maximum recommended channel frequency is 1.5MHz.

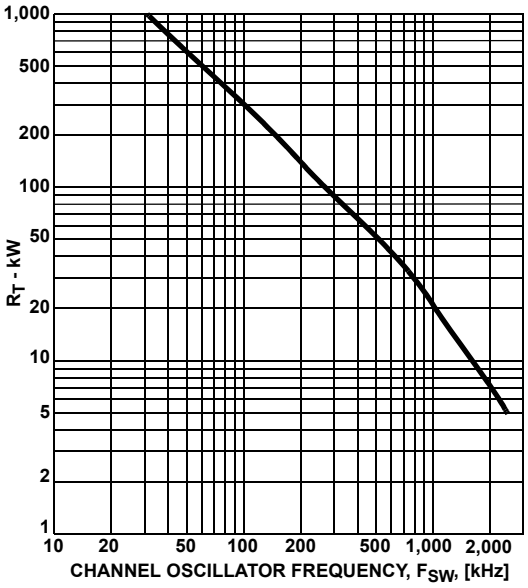


FIGURE 5. OSCILLATOR FREQUENCY vs R_T

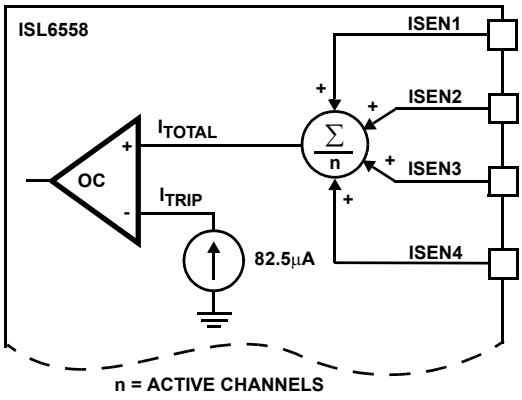


FIGURE 6. INTERNAL OVERCURRENT DETECTION CIRCUITRY

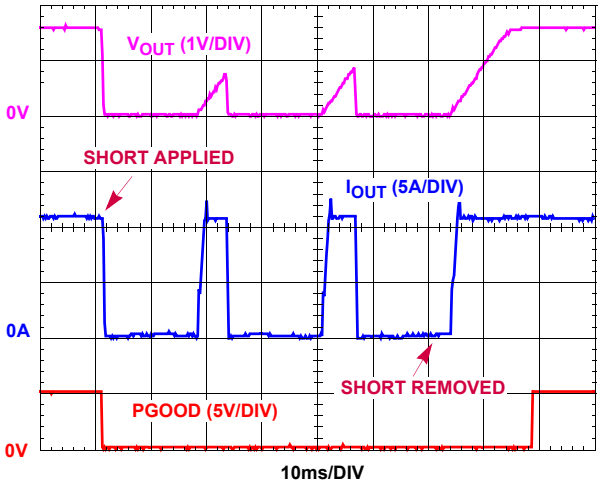


FIGURE 7. OVERCURRENT OPERATION

Reference Voltage

An internal 0.8V reference is used for both PWM duty cycle determination as well as output voltage protection. The reference is trimmed such that the system, including amplifier offset voltages, is accurate to ±1% over temperature range.

Fault Protection

The ISL6558 protects the load device from damaging stress levels. The overcurrent trip point is integral in preventing output shorts of varying degrees from causing current spikes which would damage a load device. The output voltage detection features insure a safe window of operation for the load device.

Overcurrent

The R_{ISEN} resistor scales the voltage sampled across the lower MOSFET and provides current feedback proportional to the output current of each active channel. The ISEN currents from all the active channels are averaged together to form a scaled version of the total output current, I_{TOTAL}.

See Figure 6. I_{TOTAL} is compared with an internally generated overcurrent trip current, I_{TRIP}. The overcurrent trip current source is trimmed to 82.5µA. If I_{TOTAL} exceeds the I_{TRIP} level, then the controller forces all PWM outputs into three-state. This condition results in the HIP660x gate drivers removing drive to the MOSFETs. The VSEN voltage will begin to fall and once it descends below the PGOOD falling threshold, the PGOOD signal transitions low.

A delay time, equal to the soft-start interval, is entered to allow the disturbance to clear. After the delay time, the controller then initiates a second soft-start interval. If the output voltage comes up and regulation is achieved,

PGOOD transitions high. If the OC trip current is exceeded during the soft start interval, the controller will again shut down PWM operation and three-state the drivers. The PGOOD signal will remain low and the soft-start interval will be allowed to expire. Another soft-start interval will be initiated after the delay interval. If an overcurrent trip occurs again, this same cycle repeats until the fault is removed. The OC function is shown in Figure 7 for a hard short of the output which is applied for only a brief moment. The converter quickly detects the short and attempts to restart twice before the short is removed.

Overcurrent protection reduces the regulator RMS output current under worst case conditions to 95% of the full load current.

SELECTING R_{ISEN}

The procedure for determining the value of R_{ISEN} is to insure that it scales a channel's maximum output current to 50µA. This will insure that the overcurrent trip point is properly detected when a current limit of 165% of the converter's full load current is breached. The ISEN resistor can be calculated as follows:

$$R_{ISEN} = \frac{I_{FL}}{n} x \frac{r_{DS(ON)}}{50\mu A} \quad \text{(EQ. 6)}$$

where I_{FL} is the maximum output current demanded by the load device and 'n' is the number of active channels.

OC TRIP LEVEL ADJUSTMENT

Setting the full load reference current, I_{TOTAL}, to 50µA is recommended for most applications. The ratio between the desired full load reference current and the internally set overcurrent trip current is the overcurrent trip ratio, K_{OC}. For those applications where an OC trip level of 1.65 times I_{TOTAL} is insufficient, the full load reference current can be scaled differently. Care must be taken in selection of certain components once the desired OC trip ratio is determined.

$$K_{OC} = \frac{82.5\mu A}{I_{TOTAL}} \quad \text{(EQ. 7)}$$

The new overcurrent trip ratio is then used to calculate the ISEN resistors for the new full load reference current.

$$R_{ISEN} = \frac{I_{FL}}{n} x \frac{r_{DS(ON)} x K_{OC}}{82.5\mu A} \quad \text{(EQ. 8)}$$

One commonly over looked component which will change due to the new overcurrent trip ratio is the feedback resistor, R_{FB}.

$$R_{FB} = \frac{V_{DROOP} x K_{OC}}{82.5\mu A} \quad \text{(EQ. 9)}$$

Temperature effects of the MOSFET $r_{DS(ON)}$ must be reviewed when changing the overcurrent trip level.

Output Voltage Monitoring

The output voltage must be tied to the VSEN pin to provide feedback used to create a window of operation. If the output voltage is not the reference voltage of 0.8V, it must be scaled externally down to this level. The VSEN voltage is then compared with two set voltage levels which indicate an overvoltage or undervoltage condition of the output. Violating either of these conditions results in the PGOOD pin output toggling low to indicate a problem with the output voltage.

OVERVOLTAGE

The VSEN voltage is compared with an internal overvoltage protection (OVP) reference set to 115% of the internal reference. If the VSEN voltage exceeds the OVP reference, the comparator simultaneously sets the OV latch and triggers the PWM output low. The drivers turn on the lower MOSFETs, shunting the converter output to ground. Once the output voltage falls below the nominal output voltage, the PWM outputs are placed in three-state. This prevents dumping of the output capacitors back through the lower MOSFETs. If the overvoltage conditions persist, the PWM outputs are cycled between the two states similar to a hysteretic regulator. The OV latch can only be reset by cycling the VCC supply voltage to initiate a POR and begin a soft-start interval.

UNDERVOLTAGE

The VSEN voltage is also compared to a undervoltage (UV) reference which is set to 90% of the internal reference. If the VSEN voltage is below the UV reference, the power good monitor triggers PGOOD to go low. The UV comparator does not influence converter operation.

VSEN SCALING

The output voltage, V_{OUT}, must be fed back to the VSEN pin separately from the feedback components to the FB pin. If VSEN and FB are tied together, the error amplifier will hold the VSEN voltage at the reference level while the actual output voltage level could be much different. This would mask the output voltage and prevent the protection features

from reacting to undervoltage or overvoltage conditions at the proper time.

If the output voltage is not the same as the internal 0.8V reference, then a resistor divider scaled like the FB resistors is required as shown is Figure 8. Otherwise, the output voltage should be tied directly back to the VSEN pin without a resistor divider.

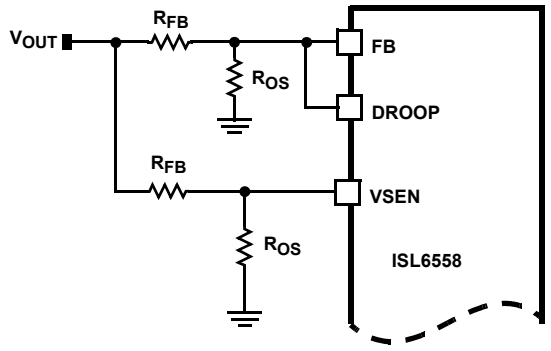


FIGURE 8. VSEN RESISTOR DIVIDER CONFIGURATION

PGOOD SIGNAL

The undervoltage comparator and overvoltage latch feed into the power good monitor and are NOR'd together. If either indicates a fault, the power good monitor triggers the PGOOD output low. A high on this open drain pin indicates proper output voltage.

Application Guidelines

Layout Considerations

Layout is very important in high frequency switching converter design. With MOSFETs switching efficiently at greater than 100kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter.

As an example, consider the turnoff transition of the PWM upper MOSFET. Prior to turnoff, the upper MOSFET was carrying the channel current. During turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using a ISL6558 controller and HIP660x gate drivers. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate equally large amounts of noise. Next are the small signal components which connect to sensitive nodes or supply critical bypassing current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 9 shows the connections of the critical components for one output channel of the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the HIP660x driver to the power MOSFET gates and source should be sized to carry at least 1A of current.

The switching components and HIP660x gate drivers should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Locate the output inductors and output capacitors between the MOSFETs and the load. Place the HIP660x gate drivers close to their respective channel MOSFETs.

The critical small signal components include the bypass capacitors for VCC on the ISL6558 controller as well as those on VCC and PVCC of the HIP660x gate drivers. Position the bypass capacitors, C_{BP}, close to the device pins. It is especially important to place the feedback resistors, R_{FB} and R_{OS}, and compensation components, R_C and C_C, associated with the input to the error amplifier close to the FB and COMP pins. Care should be taken in routing the current sense lines such that the ISEN resistors are close to their respective pins on the controller. Resistor R_T, which sets the oscillator frequency, should be positioned near the FS/EN pin.

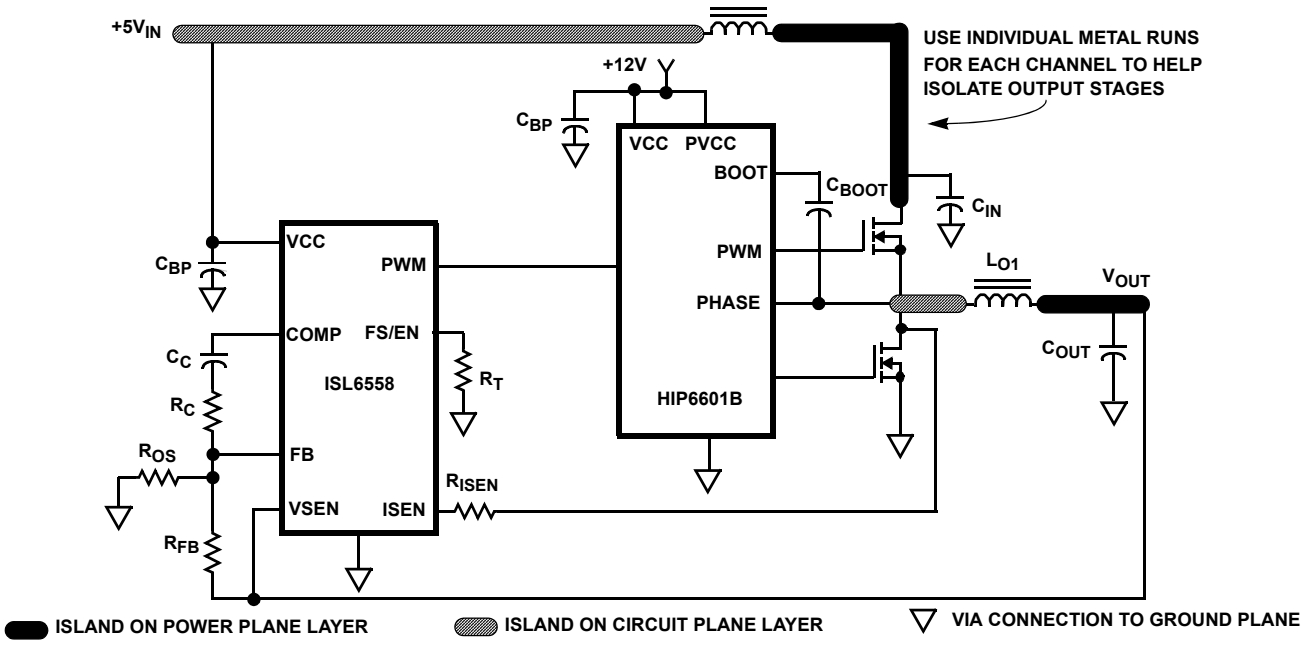


FIGURE 9. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Component Selection Guidelines

OUTPUT CAPACITOR SELECTION

Output capacitors are required to filter the output inductor current ripple and supply the load transient current. The filtering requirements are a function of the channel switching frequency and the output ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Some modern microprocessors can produce transient load rates above 200A/µs. High frequency capacitors are used to supply the initial transient current and slow the rate-of-change seen by the bulk capacitors. Bulk filter capacitor values are generally determined by the ESR and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load device for any specific decoupling requirements.

Specialized low-ESR capacitors intended for switching regulator applications are recommended for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient edge. Aluminum electrolytic capacitor ESR values are related to case size with lower ESR available in larger case sizes. However, the ESL of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

OUTPUT INDUCTOR SELECTION

The output inductor is selected to meet the voltage ripple requirements and minimize the converter response time to a load transient. In a multi-phase converter topology, the ripple current of one active channel partially cancels with the other active channels to reduce the overall ripple current. The reduction in total output ripple current results in a lower overall output voltage ripple.

The inductor selected for the power channels determines the channel ripple current. Increasing the value of inductance reduces the total output ripple current and total output voltage ripple. However, increasing the inductance value will slow the converter response time to a load transient.

One of the parameters limiting the converter's response time to a load transient is the time required to slew the inductor current from its initial current level to the transient current level. During this interval, the difference between the two levels must be supplied by the output capacitance. Minimizing the response time can minimize the output capacitance required.

The channel ripple current is approximated by the following equation:

$$DI_{CH} = \frac{V_{IN} - V_{OUT}}{F_{SW} x L} x \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 10)}$$

The total output ripple current can be determined from the curves in Figure 10. They provide the total ripple current as a function of duty cycle and number of active channels, normalized to the parameter K_{NORM} at zero duty cycle.

$$K_{NORM} = \frac{V_{OUT}}{LxF_{SW}} \quad \text{(EQ. 11)}$$

where L is the channel inductor value.

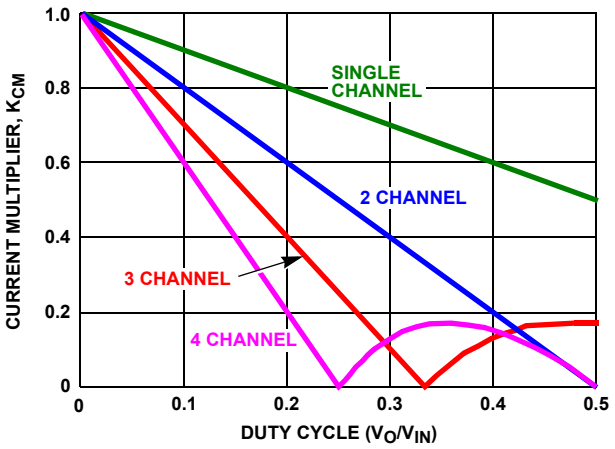


FIGURE 10. RIPPLE CURRENT vs DUTY CYCLE

Find the intersection of the active channel curve and duty cycle for your particular application. The resulting ripple current multiplier from the y-axis is then multiplied by the normalization factor, K_{NORM}, to determine the total output ripple current for the given application.

$$DI_{TOTAL} = K_{NORM} x K_{CM} \quad \text{(EQ. 12)}$$

INPUT CAPACITOR SELECTION

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

Two important parameters to consider when selecting the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select a bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current requirement for a converter design can be approximated with the aid of Figure 11. Follow the curve for the number of active channels in the converter design. Next determine the duty cycle for the converter and find the intersection of this value and the active channel curve. Find the corresponding y-axis value, which is the current multiplier. Multiply the total full load output current, not the channel value, by the current multiplier value found and the result is the RMS input current which must be supported by the input capacitors.

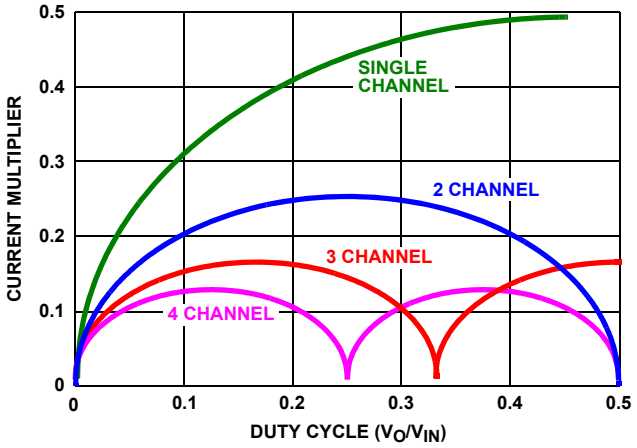


FIGURE 11. CURRENT MULTIPLIER vs DUTY CYCLE

MOSFET SELECTION AND CONSIDERATIONS

The ISL6558 requires two N-Channel power MOSFETs per active channel or more if parallel MOSFETs are employed. These MOSFETs should be selected based upon $r_{DS(ON)}$, total gate charge, and thermal management requirements.

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle of the converter (see the equations below). The conduction losses are the main component of power dissipation for the lower MOSFETs, Q2 and Q4 of Figure 1. Only the upper MOSFETs, Q1 and Q3 have significant switching losses, since the lower device turn on and off into near zero voltage.

The following equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFETs body diode. The gate-charge losses are dissipated in the HIP660x drivers and don't heat the MOSFETs. However, large gate-charge increases the switching time, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_{SW}}{2} \quad \text{(EQ. 13)}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ. 14)}$$

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 28, 2015	FN9027.13	Added Revision History beginning with Rev 13 Added About Intersil Verbiage Updated Ordering Information Table on page 2 Updated POD M16.15 to most recent revision. Removed "u" symbol from drawing (overlaps the "a" on Side View). Changes were made to some values in table.

About Intersil

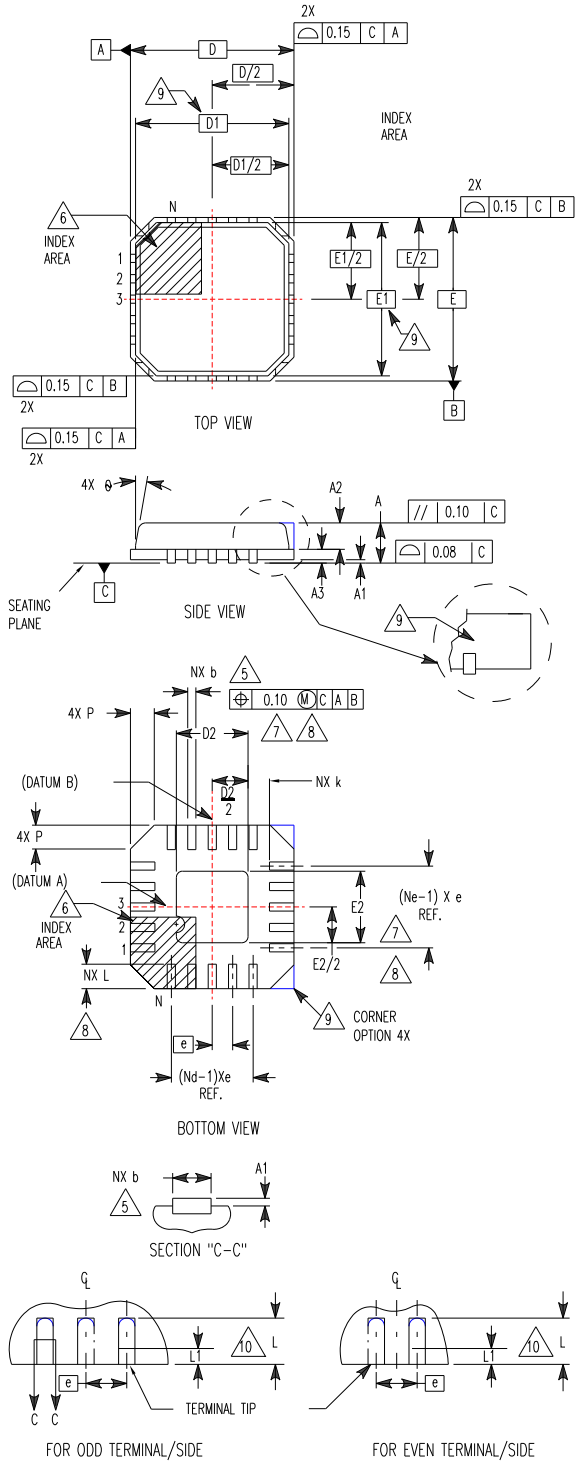
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.5x5

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

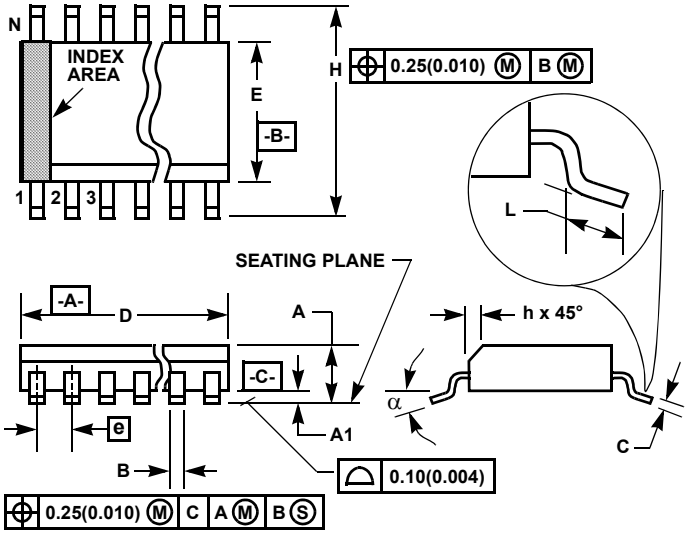
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	0.02	0.05	-
A2	-	0.65	1.00	9
A3		0.20 REF		9
b	0.23	0.30	0.38	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.65 BSC		-
k	0.20	-	-	-
L	0.35	0.60	0.75	8
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 4 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220VHHC Issue I except for the "b" dimension.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

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