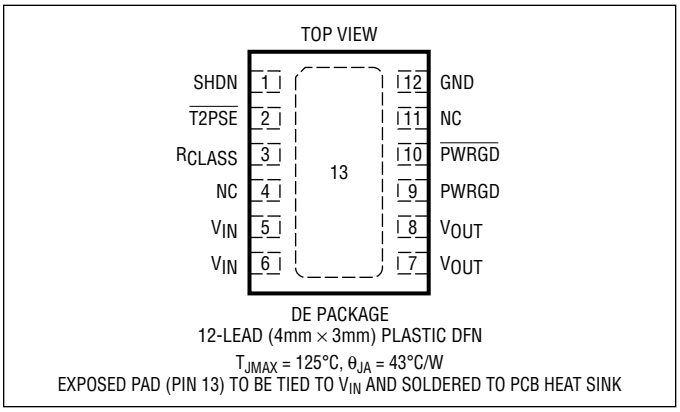
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

GND Voltage ..... –0.3V to 100V
V_{OUT} Voltage .....–0.3V to 100V (and ≤ GND)
V_{OUT} Pull-Up Current 1A
SHDN ..... –0.3V to 100V
R_{CLASS}, Voltage..... –0.3V to 7V
R_{CLASS} Current.....50mA
PWRGD Voltage (Note 4)
  Low Impedance Source .....V_{OUT} – 0.3V to V_{OUT} +11V
  Pull-Up Current.....5mA
$\overline{PWRGD}$, $\overline{T2PSE}$ Voltage..... –0.3V to 100V
$\overline{PWRGD}$, $\overline{T2PSE}$ Pull-Down Current 10mA
Junction Temperature ..... 125°C
Operating Ambient Temperature Range
  LTC4265C ..... 0°C to 70°C
  LTC4265I..... –40°C to 85°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) TO BE TIED TO V_{IN} AND SOLDERED TO PCB HEAT SINK

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4265CDE#PBF	LTC4265CDE#TRPBF	4265	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC4265IDE#PBF	LTC4265IDE#TRPBF	4265	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Voltage	At GND Pin (Note 5)				60	V
Signature Range		●	1.5		9.8	V
Classification Range		●	12.5		21	V
Turn-On Voltage		●			37.2	V
Undervoltage Lock Out		●	30.0			V
Overvoltage Lock Out				71		V
ON/UVLO Hysteresis Window		●	4.1			V
Signature/Class Hysteresis Window		●	1.4			V
Reset Threshold	State Machine Reset for 2-event Classification	●	2.57		5.40	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Supply Current at 60V	Measured at GND Pin	●			1.35	mA
Class 0 Current	GND = 17.5V, No R_{CLASS} Resistor	●			0.40	mA
SIGNATURE						
Signature Resistance	1.5V ≤ GND ≤ 9.8V (Note 6)	●	23.25		26	kΩ
Invalid Signature Resistance, SHDN Invoked	1.5V ≤ GND ≤ 9.8V, V_{SHDN} = 3V (Note 6)	●			11	kΩ
Invalid Signature Resistance During Mark Event	(Notes 6, 7)	●			11	kΩ
CLASSIFICATION						
Class Accuracy	10mA < I_{CLASS} < 40mA, 12.5V < GND < 21V (Note 8, 9)	●			±3.5	%
Classification Stability Time	GND Pin Step to 17.5V, R_{CLASS} = 30.9, I_{CLASS} Within 3.5% of Ideal Value (Notes 8, 9)	●			1	ms
NORMAL OPERATION						
Inrush Current	GND = 54, V_{OUT} = 3V	●	60	100	180	mA
Power FET On Resistance	Tested at 600mA into V_{OUT}, GND = 54V	●		0.70	1.0	Ω
Power FET Leakage Current at V_{OUT}	GND = SHDN = V_{OUT} = 57V	●			1	µA
DIGITAL INTERFACE						
SHDN Input High Level Voltage		●	3			V
SHDN Input Low Level Voltage		●			0.45	V
SHDN Input Resistance	GND = 9.8V, SHDN = 9.65V	●	100			kΩ
$\overline{PWRGD}$, $\overline{T2PSE}$ Voltage Output Low	Tested at 1mA, GND = 54V. For $\overline{T2PSE}$, Must Complete 2-event Classification to See Active Low.	●			0.15	V
$\overline{PWRGD}$, $\overline{T2PSE}$ Leakage Current	Pin Voltage Pulled 57V, GND = V_{IN} = 0	●			1	µA
PWRGD Voltage Output Low	Tested at 0.5mA, GND = 52V, V_{OUT} = 48V, Output Voltage is with Respect to V_{OUT}	●			0.4	V
PWRGD Voltage Clamp	Tested at 2mA, V_{OUT} = 0V, Voltage with Respect to V_{OUT}	●	12		16.5	V
PWRGD Leakage Current	V_{PWRGD} = 11V, V_{OUT} = V_{IN} = 0V, GND = 54V	●			1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to V_{IN} pin unless otherwise noted.

Note 3: Pins with 100V absolute maximum guaranteed for T ≥ 0°C, otherwise 90V.

Note 4: PWRGD voltage clamps at 14V with respect to V_{OUT}.

Note 5: Input voltage specifications are defined with respect to LTC4265 pins and meet IEEE 802.3af/at specifications when the input diode bridge is included.

Note 6: Signature resistance is measured via the ΔV/ΔI method with a minimum ΔV of 1V. The LTC4265 signature resistance accounts for the additional series resistance in the input diode bridge.

Note 7: An invalid signature after the 1st classification event is mandated by IEEE 802.3at standard. See Applications Information.

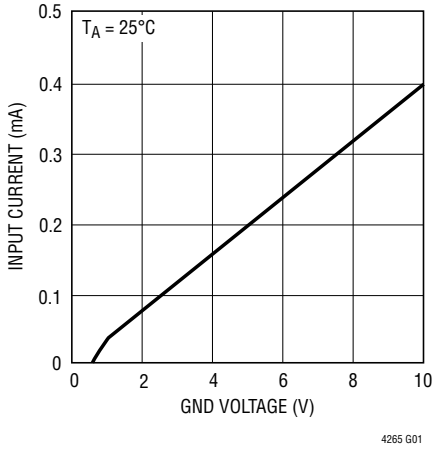
Note 8: Class accuracy is with respect to the ideal current defined as 1.237/R_{CLASS} and does not include variations in R_{CLASS} resistance.

Note 9: This parameter is assured by design and wafer level testing.

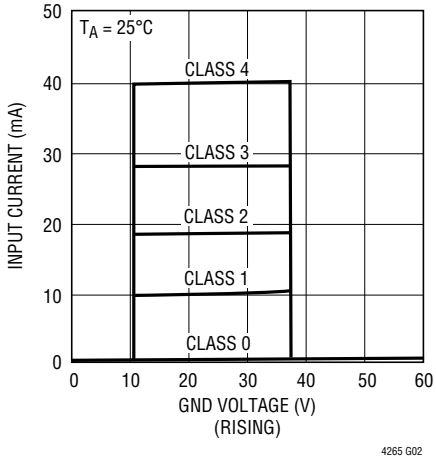
Note 10: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

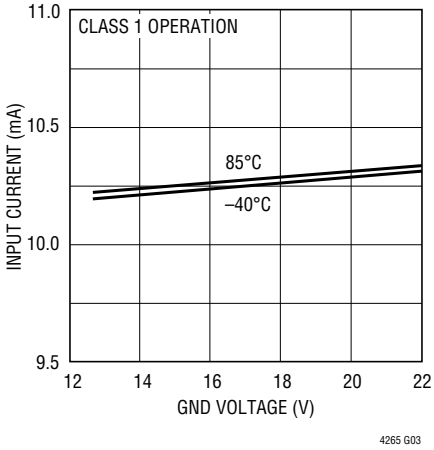
Input Current vs Input Voltage 25k Detection Range



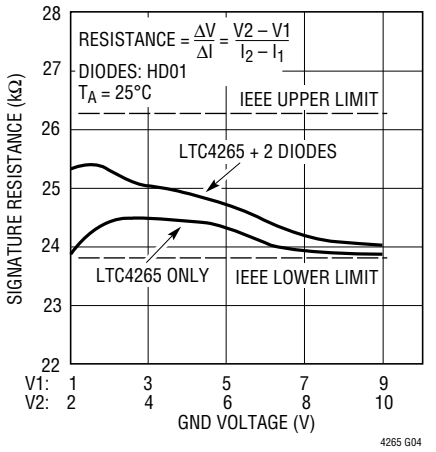
Input Current vs Input Voltage



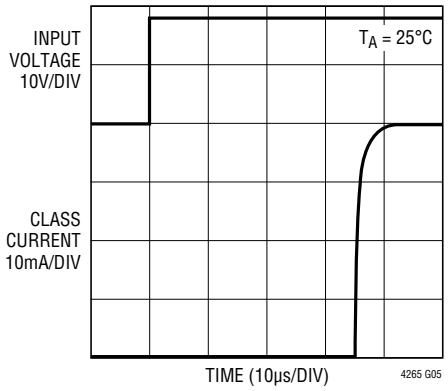
Input Current vs Input Voltage



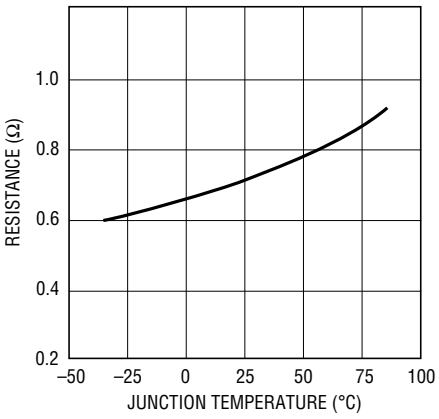
Signature Resistance vs Input Voltage



Class Operation vs Time

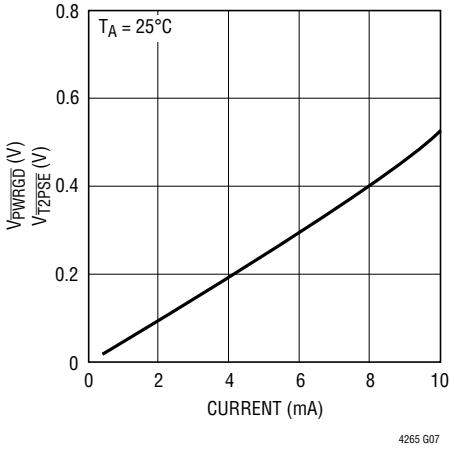


On Resistance vs Temperature

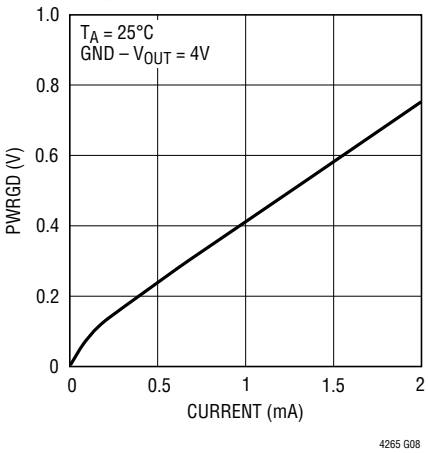


TYPICAL PERFORMANCE CHARACTERISTICS

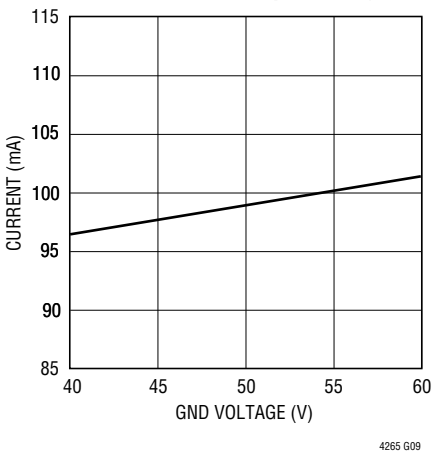
$\overline{\text{PWRGD}}$, $\overline{\text{T2PSE}}$ Output Low Voltage vs Current



Active High PWRGD Output Low Voltage vs Current



Inrush Current vs Input Voltage



PIN FUNCTIONS

SHDN (Pin 1): Shutdown Input. Use this pin for auxiliary power application. Drive SHDN high to disable LTC4265 operation and corrupt the signature resistance. If unused, tie SHDN to V_{IN}.

$\overline{\text{T2PSE}}$ (Pin 2): Type-2 PSE Indicator, Open-Drain. Low impedance indicates the presence of a Type-2 PSE.

R_{CLASS} (Pin 3): Class Select Input. Connect a resistor between R_{CLASS} and V_{IN} to set the classification load current. (See Table 2.)

NC (Pin 4, 11): No Connect.

V_{IN} (Pins 5, 6): Input Voltage, Negative Rail. Pins 5 and 6 must be electrically tied together at the package.

V_{OUT} (Pins 7, 8): Output Voltage Negative Rail. Connects V_{OUT} to V_{IN} through an internal power MOSFET. Pins 7 and 8 must be electrically tied together at the package.

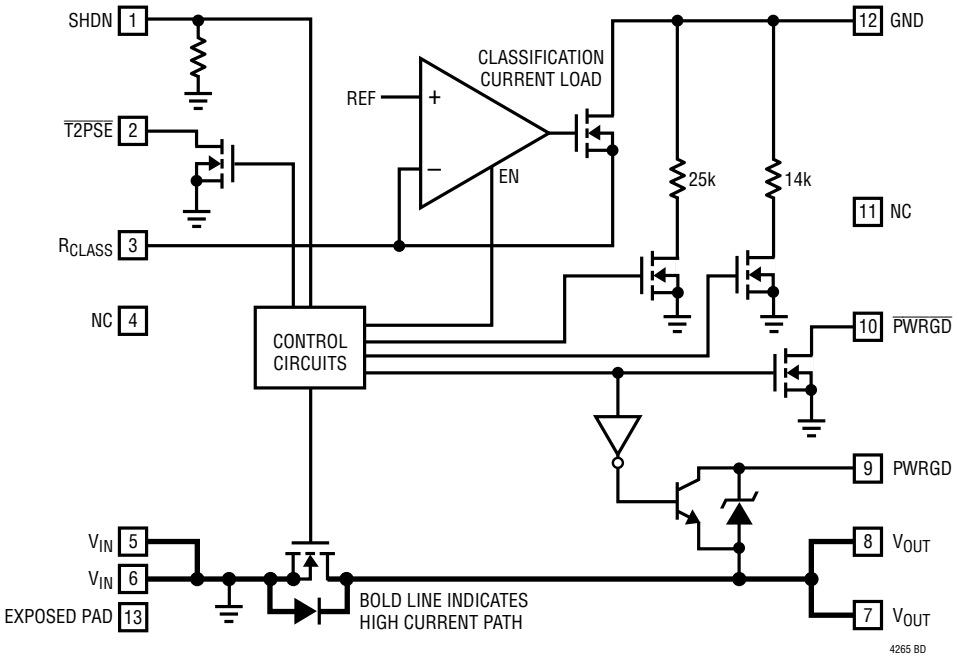
PWRGD (Pin 9): Power Good Output, Open Collector. High impedance signals power-up completion. PWRGD is referenced to V_{OUT} and features a 14V clamp.

$\overline{\text{PWRGD}}$ (Pin 10): Complementary Power Good Output, Open-Drain. Low impedance signals power up completion. $\overline{\text{PWRGD}}$ is referenced to V_{IN}.

GND (Pin 12): Input Voltage, Positive Rail. This pin is connected to the PD positive rail.

Exposed Pad (Pin 13): Tie to V_{IN} and PCB heat sink.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as more products are taking advantage of having DC power and high speed data available from a single RJ45 connector. As PoE continues to grow in the marketplace, Powered Device (PD) equipment vendors are running into the 12.95W power limit established by the IEEE 802.3af standard.

The IEE802.3at standard establishes a higher power allocation for Power-over-Ethernet while maintaining backwards compatibility with the existing IEEE802.3af systems. Power Sourcing Equipments (PSE) and Powered Devices are distinguished as Type-1 complying with the IEEE 802.3af power levels, or Type-2 complying with the IEEE 802.3at power levels. The maximum available power of a Type-2 PD is 25.5W.

The IEEE802.3at standard also establishes a new method of acquiring power classification from a PD and communicating the presence of a Type-2 PSE. A Type-2 PSE has the option of acquiring PD power classification by performing 2-event classification (Layer 1) or by communicating with the PD over the data line (Layer 2). In turn, a Type-2 PD must be able to recognize both layers of communications and identify a Type-2 PSE.

The LTC4265 is specifically designed to support the front end of a PD that must operate under the IEEE802.3at standard. In particular, the LTC4265 provides the $\overline{T2PSE}$ indicator bit which recognizes 2-event classification. This indicator bit may be used to alert the LTC4265 output load that a Type-2 PSE is present. With an internal signature resistor, classification circuitry, inrush control, and thermal shutdown, the LTC4265 is a complete PD Interface solution capable of supporting in the next generation PD applications.

MODES OF OPERATION

The LTC4265 has several modes of operation depending on the input voltage applied between the GND and V_{IN} pins. Figure 1 presents an illustration of voltage and current waveforms the LTC4265 may encounter with the various modes of operation summarized in Table 1.

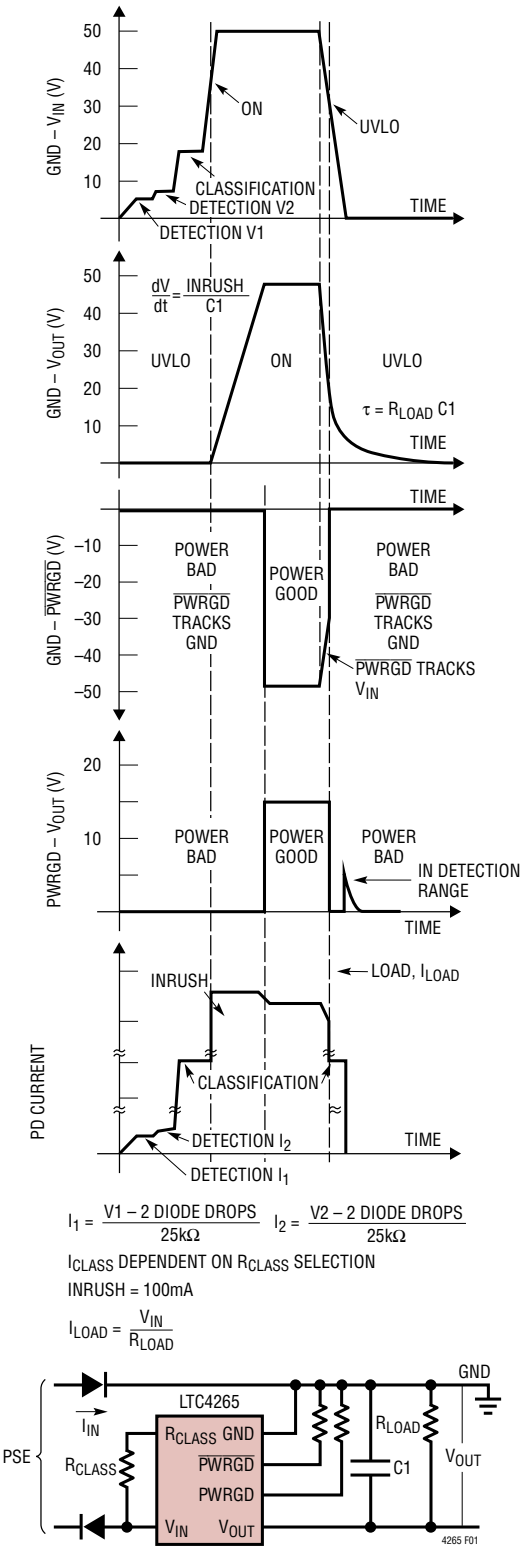


Figure 1. Output Voltage, $\overline{PWRGD}$, PWRGD and PD Current as a Function of Input Voltage

APPLICATIONS INFORMATION

These modes satisfy the requirements defined in the IEEE 802.3af/at specification.

Table 1. LTC4265 Modes of Operation as a Function of Input Voltage

GND (V)	LTC4265 MODES OF OPERATION
0V to 1.4V	Inactive (Reset After 1st Classification Event)
1.5V to 9.8V (5.4V to 9.8V)	25k Signature Resistor Detection Before 1st Classification Event (Mark, 11k Signature Corrupt After 1st Classification Event)
12.5V to ON/UVLO*	Classification Load Current Active
ON/UVLO* to 60V	Inrush and Power Applied To PD Load
>71V	Overvoltage Lockout, 4265 Operations are Disabled

*ON/UVLO includes hysteresis. Rising input threshold, 37.2V Max. Falling input threshold, 30V Min.

INPUT DIODE BRIDGE

In the IEEE 802.3af/at standard, the modes of operation reference the input voltage at the PD's RJ45 connector. Since the PD must handle power received in either polarity from either the data or the spare pair, input diode bridges BR1 and BR2 are connected between the RJ45 connector and the LTC4265 (Figure 2).

The input diode bridge introduces a voltage drop that affects the range for each mode of operation. The LTC4265 compensates for these voltage drops so that a PD built with the LTC4265 meets the IEEE 802.3af/at-established voltage ranges. Note that the Electrical Specifications reference with respect to the LTC4265 package pins.

DETECTION

During detection, the PSE looks for a 25k signature resistor which identifies the device as a PD. The PSE will apply two voltages in the range of 2.8V to 10V and measures the corresponding currents. Figure 1 shows the detection voltages V1 and V2 and the corresponding PD current. The PSE calculates the signature resistance using the $\Delta V/\Delta I$ measurement technique.

The LTC4265 presents its precision, temperature-compensated 25k resistor between the GND and V_{IN} pins, alerting the PSE that a PD is present and requests power to be applied. The LTC4265 signature resistor also compensates for the additional series resistance introduced by the input diode bridge. Thus a PD built with the LTC4265 conforms to the IEEE 802.3af/at detection specifications.

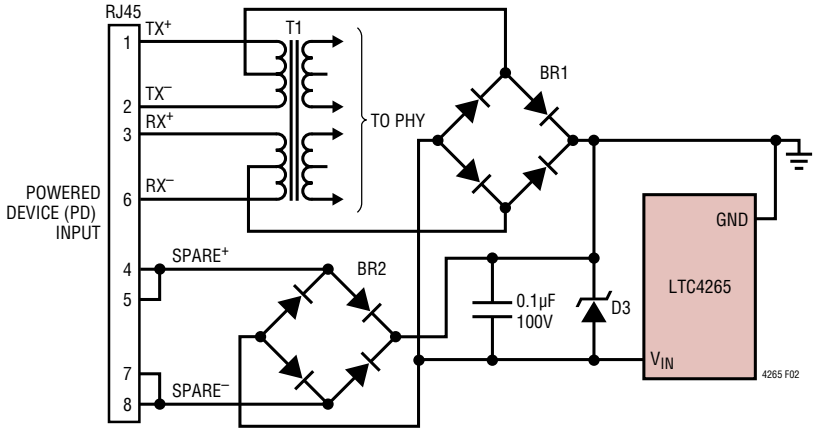


Figure 2. PD Front End Using Diode Bridges on Main and Spare Inputs

APPLICATIONS INFORMATION

SIGNATURE CORRUPT OPTION

In some designs that include an auxiliary power option, it is necessary to prevent a PD from being detected by a PSE. The LTC4265 signature resistance can be corrupted with the SHDN pin (Figure 3). Taking the SHDN pin high will reduce the signature resistor below 11k which is an invalid signature per the IEEE 802.3af/at specification, and alerts the PSE not to apply power. Invoking the SHDN pin also ceases operation for classification and disconnects the LTC4265 load from the PD input. If this feature is not used, connect SHDN to V_{IN}.

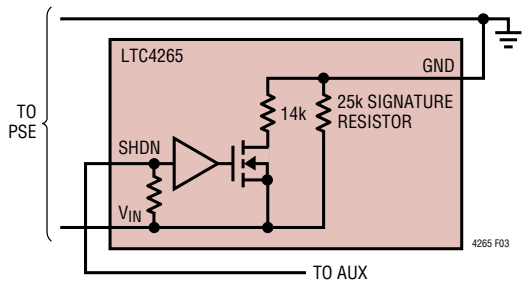


Figure 3. 25k Signature Resistor with Disable

CLASSIFICATION

Classification provides a method for more efficient power allocation by allowing the PSE to identify a PD power classification. Class 0 is included in the IEEE specification for PDs that don't support classification. Class 1-3 partitions PDs into 3 distinct power ranges. Class 4 includes the new power range under IEEE802.3at (See Table 2).

During classification probing, the PSE presents a fixed voltage between 15.5V and 20.5V to the PD (Figure 2). The LTC4265 asserts a load current representing the PD power classification. The classification load current is programmed with a resistor R_{CLASS} that is chosen from Table 2.

Table 2. Summary of Power Classifications and LTC4265 R_{CLASS} Resistor Selection

CLASS	USAGE	MAXIMUM AVERAGE POWER LEVELS AT INPUT OF PD (W)	NOMINAL CLASSIFICATION LOAD CURRENT (mA)	LTC4265 R_{CLASS} RESISTOR (Ω, 1%)
0	Default	0.44 to 13.0	< 0.4	Open
1	Optional	0.44 to 3.84	10.5	124
2	Optional	3.84 to 6.49	18.5	69.8
3	Optional	6.49 to 13.0	28	45.3
4	Optional	13.0 to 25.5	40	30.9

2-EVENT CLASSIFICATION AND THE $\overline{T2PSE}$ PIN

A Type-2 PSE may declare the availability of high power by performing 2-event classification (Layer 1) or by communicating over the high speed data line (Layer 2). A Type-2 PD must recognize both layers of communication. Since Layer 2 communications takes place directly between the PSE and the LTC4265 load, the LTC4265 concerns itself only with recognizing 2-event classification.

APPLICATIONS INFORMATION

In 2-event classification, a Type-2 PSE probes for power classification twice. Figure 4 presents an example of a 2-event classification. The 1st classification event occurs when the PSE presents an input voltage between 14.5V to 20.5V and the LTC4265 presents a class 4 load current. The PSE then drops the input voltage into the mark voltage range of 6.9V to 10V, signaling the 1st mark event. The PD in the mark voltage range presents a load current between 0.25mA to 4mA.

The PSE repeats this sequence, signaling the 2nd Classification and 2nd mark event occurrence. This alerts the LTC4265 that a Type-2 PSE is present. The Type-2 PSE then applies power to the PD and the LTC4265 charges up the reservoir capacitor C1 with a controlled inrush current. When C1 is fully charged, and the LTC4265 declares power good, the $\overline{T2PSE}$ pin presents an active low signal, or low impedance output with respect to V_{IN}. The $\overline{T2PSE}$ output becomes inactive when the LTC4265 input voltage falls outside the normal operating range.

SIGNATURE CORRUPT DURING MARK

As a member of the IEEE802.3at working group, Linear notes that it is possible for a Type-2 PD to receive a false indication of a 2-event classification if a PSE port is pre-charged to a voltage above the detection voltage range before the first detection cycle. The IEEE working group modified the standard to prevent this possibility by requiring a Type-2 PD to corrupt the signature resistance during the mark event, alerting the PSE not to apply power. The LTC4265 conforms to this standard by internally corrupting the signature resistance. This also discharges the port before the PSE begins the next detection cycle.

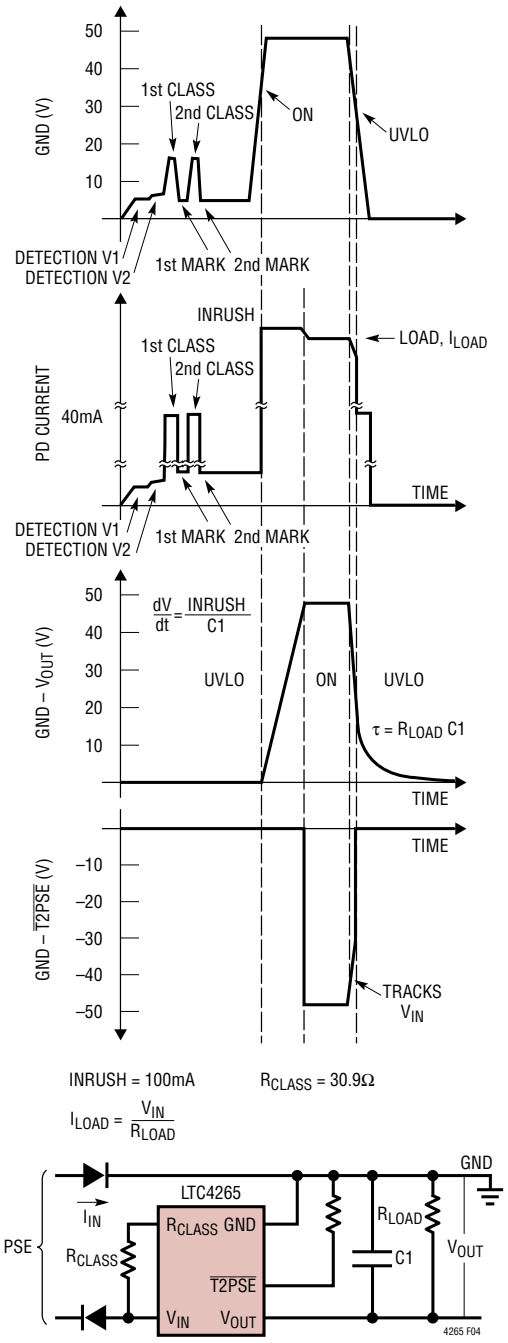


Figure 4. V_{OUT}, $\overline{T2PSE}$, and PD Current as a Result of 2-event Classification

APPLICATIONS INFORMATION

PD STABILITY DURING CLASSIFICATION

Classification presents a challenging stability problem due to the wide range of possible classification load current. The onset of the classification load current introduces a voltage drop across the cable and increases the forward voltage of the input diode bridge. This may cause the PD to oscillate between detection and classification with the onset and removal of the classification load current.

The LTC4265 prevents this oscillation by introducing a voltage hysteresis window between the detection and classification ranges. The hysteresis window accommodates the voltage changes a PD encounters at the onset of the classification load current, thus providing a trouble-free transition between detection and classification modes.

The LTC4265 also maintains a positive I-V slope throughout the classification ranges up to the ON voltage. In the event a PSE overshoots beyond the classification voltage range, the available load current aids in returning the PD back into the classification voltage range. (The PD input may otherwise be "trapped" by a reverse-biased diode bridge and the voltage held by the 0.1µF capacitor.)

INRUSH CURRENT

Once the PSE detects and optionally classifies the PD, the PSE then applies powers on the PD. When the LTC4265 input voltage rises above the ON voltage threshold, LTC4265 connects V_{OUT} to V_{IN} through the internal power MOSFET.

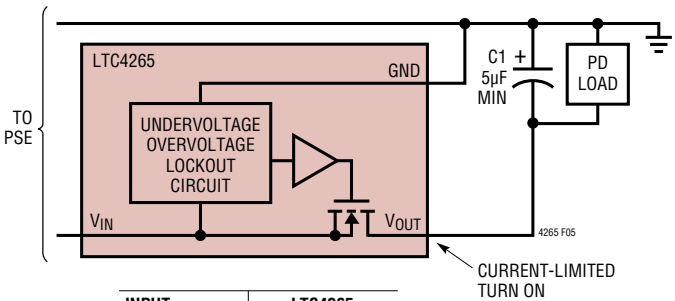
To control the power-on surge currents in the system, the LTC4265 provides a fixed inrush current, allowing C1 to ramp up to the line voltage in a controlled manner.

The LTC4265 keeps the PD inrush current below the PSE current limit to provide a well-controlled power-up characteristic that is independent of the PSE behavior. This ensures a PD using the LTC4265 interoperability with any PSE.

UNDERVOLTAGE LOCKOUT

The IEEE 802.3af/at specification for the PD dictates a maximum turn-on voltage of 42V and a minimum turn-off voltage of 30V. This specification provides an adequate voltage to begin PD operation, and to discontinue PD operation when the input voltage is too low. In addition, this specification allows PD designs to incorporate an on-off hysteresis window to prevent start-up oscillations.

The LTC4265 features an ON-undervoltage lockout (UVLO) hysteresis window (See Figure 5) that conforms with the IEEE 802.3af/at specifications and accommodates the voltage drop in the cable and input diode bridge at the onset of the inrush current.



INPUT VOLTAGE	LTC4265 POWER MOSFET
0V TO ON*	OFF
>ON*	ON
<UVLO*	OFF
>OVLO	OFF

*INCLUDES ON-UVLO HYSTERESIS
ON THRESHOLD ≅ 36.1V
UVLO THRESHOLD ≅ 30.7V
OVLO THRESHOLD ≅ 71.0V

Figure 5. LTC4265 Undervoltage and Overvoltage Lockout

APPLICATIONS INFORMATION

Once C1 is fully charged, the LTC4265 turns on is internal MOSFET and passes power to the PD load. The LTC4265 continues to power the PD load as long as the input voltage does not fall below the UVLO threshold. When the LTC4265 input voltage falls below the UVLO threshold, the PD load is disconnected, and classification mode resumes. C1 discharges through the LTC4265 circuitry.

COMPLEMENTARY POWERGOOD

When LTC4265 fully charges the load capacitor (C1), power good is declared and the LTC4265 load can safely begin operation. The LTC4265 provides complementary power good signals that remain active during normal operation and are de-asserted when the input voltage falls below the UVLO threshold, when the input voltage exceeds the over-voltage lockout (OVLO) threshold, or in the event of a thermal shutdown. See Figure 6.

The PWRGD pin features an open collector output referenced to V_{OUT} which can interface directly with the "Run" pin of a DC/DC converter product. When power good is declared and active, the PWRGD pin is high impedance with respect to V_{OUT}. An internal 14V clamp protects the DC/DC converter from an excessive voltage.

The active low $\overline{PWRGD}$ pin connects to an internal, open drain MOSFET referenced to V_{IN} and can interface directly to the shutdown pin of a DC/DC converter product. When power good is declared and active, the $\overline{PWRGD}$ pin is low impedance with respect to V_{IN}.

PWRGD PIN WHEN SHDN IS INVOKED

In PD applications where an auxiliary power supply invokes the SHDN feature, the PWRGD pin becomes high impedance. This prevents the PWRGD pin that is connected to the "Run" pin of the DC/DC converter from interfering with the DC/DC converter operations when powered by an auxiliary power supply.

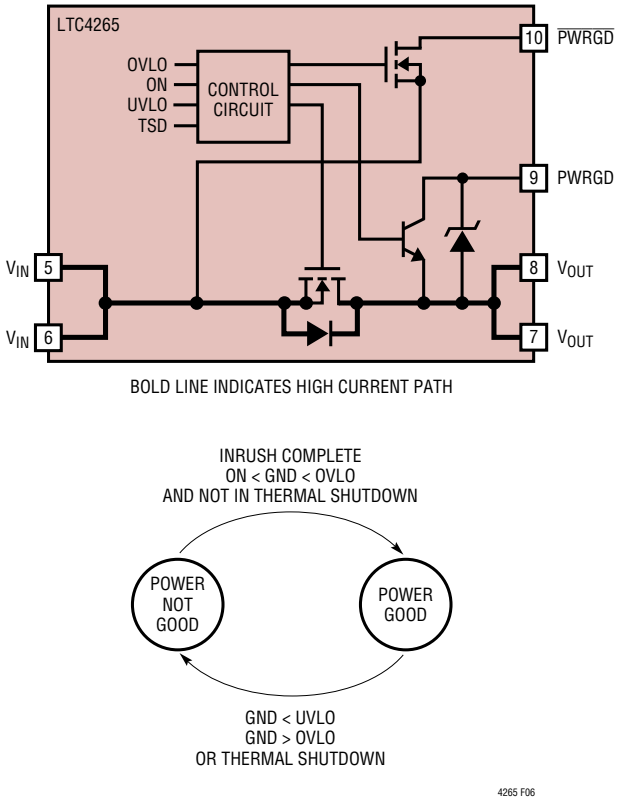


Figure 6. LTC4265 Power Good Functional and State Diagram

APPLICATIONS INFORMATION

OVERVOLTAGE LOCKOUT

The LTC4265 includes an overvoltage lockout (OVLO) feature (Figure 5) which protects the LTC4265 and its load from an overvoltage event. If the input voltage exceeds the OVLO threshold, the LTC4265 discontinues PD operation. Normal operations resume when the input voltage falls below the OVLO threshold and when C1 is charged up.

THERMAL PROTECTION

The IEEE 802.3af/at specification requires a PD to withstand any applied voltage from 0V to 57V indefinitely. However, there are several possible scenarios where a PD may encounter excessive heating.

During classification, excessive heating may occur if the PSE exceeds the 75ms probing time limit. At turn-on, when the load capacitor begins to charge, the instantaneous power dissipated by the PD Interface can be large before it reaches the line voltage. And if the PD experiences a fast input positive voltage step in its operational mode (for example, from 37V to 57V), the instantaneous power dissipated by the PD Interface can be large.

The LTC4265 includes a Thermal Protection feature which protects the LTC4265 from excessive heating. If the LTC4265 junction temperature exceeds the over-temperature threshold, the LTC4265 discontinues PD operations and power-good becomes inactive. Normal operation resumes when the junction temperature falls below the over-temperature threshold and when C1 is charged up.

EXTERNAL INTERFACE AND COMPONENT SELECTION

Transformer

Nodes on an Ethernet network commonly interface to the outside world via an isolation transformer. For PDs, the isolation transformer must also include a center tap on the RJ45 connector side (See Figure 7).

The increased current levels in a Type-2 PD over a Type-1 increase the current imbalance in the magnetics which can interfere with data transmission. In addition, proper termination is also required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions. Transformer vendors such as

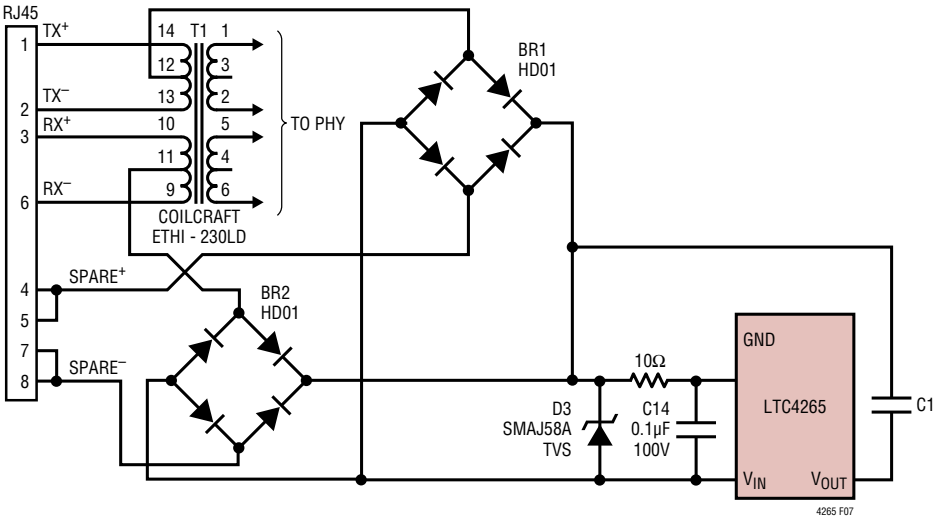


Figure 7. PD Front-End with Isolation Transformer, Diode Bridges, Capacitors, and a Transient Voltage Suppressor (TVS).

APPLICATIONS INFORMATION

Bel Fuse, Coilcraft, Halo, Pulse, and Tyco (Table 4) can assist in selecting an appropriate isolation transformer and proper termination methods.

Table 4. Power-over-Ethernet Transformer Vendors

VENDOR	CONTACT INFORMATION
Bel Fuse Inc.	206 Van Vorst Street Jersey City, NJ 07302 Tel: 201-432-0463 www.belfuse.com
Coilcraft Inc.	1102 Silver Lake Road Gary, IL 60013 Tel: 847-639-6400 www.coilcraft.com
Halo Electronics	1861 Landings Drive Mountain View, CA 94043 Tel: 650-903-3800 www.haloelectronics.com
PCA Electronics	16799 Shoenborn Street North Hills, CA 91343 Tel: 818-892-0761 www.pca.com
Pulse Engineering	12220 World Trade Drive San Diego, CA 92128 Tel: 858-674-8100 www.pulseeng.com
Tyco Electronics	308 Constitution Drive Menlo Park, CA 94025-1164 Tel: 800-227-7040 www.circuitprotection.com

Input Diode Bridge

Figure 2 shows how two diode bridges are typically connected in a PD application. One bridge is dedicated to the data pair while the other bridge is dedicated to the spare pair. The LTC4265 supports the use of either silicon or Schottky input diode bridges. However, there are tradeoffs in the choice of diode bridges.

An input diode bridge must exceed the maximum current the PD application will encounter at the temperature the PD will operate. Diode bridge vendors typically call out the operating current at room temperature, but derate the maximum current with increasing temperature. Consult the diode bridge vendors for the operating current derating curve.

A silicon diode bridge can consume over 4% of the available power in some PD applications. Using Schottky diodes can help reduce the power loss with a lower forward voltage.

A Schottky bridge may not be suitable for some high temperature PD application. The leakage current has a voltage dependency that can reduce the perceived signature resistance. In addition, the IEEE 802.3af/at specification mandates the leakage back-feeding through the unused bridge cannot generate more than 2.8V across a 100k resistor when a PD is powered with 57V.

Sharing Input Diode Bridges

At higher temperatures, a PD design may be forced to consider larger bridges in a bigger package because the maximum operating current for the input diode bridge is drastically de-rated. The larger package may not be acceptable in some space-limited environments.

One solution to consider is to reconnect the diode bridges so that only one of the four diodes conducts current in each package. This configuration extends the maximum operating current while maintaining a smaller package profiles. Figure 7 shows how to reconnect the two diode bridges. Consult the diode bridge vendors for the de-rating curve when only one of four diodes is in operation.

APPLICATIONS INFORMATION

Input Capacitor

The IEEE 802.3af/at standard includes an impedance requirement in order to implement the AC disconnect function. A 0.1µF capacitor (C14 in Figure 7) is used to meet this AC impedance requirement.

Input Series Resistance

Linear Technology has seen the customer community cable discharge requirements increase by nearly 500,000 times the original test levels. The PD must survive and operate reliably not only when an initially charged cable connects and dissipates the energy through the PD front end, but also when the electrical power system grounds are subject to very high energy events (e.g. lightning strikes).

In these high energy events, adding 10Ω series resistance into the V_{PORTP} pin greatly improves the robustness of the LTC4265 based PD. (See Figure 7.) The TVS limits the voltage across the port while the 10Ω and 0.1µF capacitance reduces the edge rate the LT4265 encounters across its pin. The added 10Ω series resistance does not operationally affect the LTC4265 PD Interface nor does it affect its compliance with the IEEE 802.3 standard.

Transient Voltage Suppressor

The LTC4265 specifies an absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events. However, the pins that interface to the outside world can routinely see excessive peak voltages. To protect the LTC4265, install a transient voltage suppressor (D3) between the input diode bridge and the LTC4265 as shown in Figure 7.

An SMAJ58A is recommended for typical PD applications. However, an SMBJ58A may be preferred in applications where the PD front-end must absorb higher energy discharge events.

Classification Resistor (R_{CLASS})

The R_{CLASS} resistor sets the classification load current, corresponding to the PD power classification. Select the value of R_{CLASS} from Table 2 and connect the resistor between the R_{CLASS} and V_{IN} pins as shown in Figure 4, or float the R_{CLASS} pin if the classification load current is not required. The resistor tolerance must be 1% or better to avoid degrading the overall accuracy of the classification circuit.

Load Capacitor

The IEEE 802.3af/at specification requires that the PD maintains a minimum load capacitance of 5µF and does not specify a maximum load capacitor. However, if the load capacitor is too large, there may be a problem with inadvertent power shutdown by the PSE.

This occurs when the PSE voltage drops quickly. The input diode bridge reverses bias, and the PD load momentarily powers off the load capacitor. If the PD does not draw power within the PSE's 300ms disconnection delay, the PSE may remove power from the PD. Thus, it is necessary to evaluate the load current and capacitance to ensure that an inadvertent shutdown cannot occur.

The load capacitor can store significant energy when fully charged. The PD design must ensure that this energy is not inadvertently dissipated in the LTC4265. For example, if the GND pin shorts to V_{IN} while the capacitor is charged, current will flow through the parasitic body diode of the internal MOSFET and may cause permanent damage to the LTC4265.

Power Good Interface

The LTC4265 provides complementary power good signals to simplify the DC/DC converter interface. Using the power good signal to delay converter operation until the load capacitor is fully charged is highly recommended to ensure trouble free start up.

Figure 8 presents examples of power good interface circuits. The active high PWRGD pin has an open collector transistor referenced to VOUT while the active low $\overline{\text{PWRGD}}$ pin has a high voltage, open-drain MOSFET referenced to V_{IN}. The designer can choose either signal to enable the DC/DC converter. When using $\overline{\text{PWRGD}}$, diode D9 and resistor R_S protects the converter shutdown pin from excessive reverse voltage.

APPLICATIONS INFORMATION

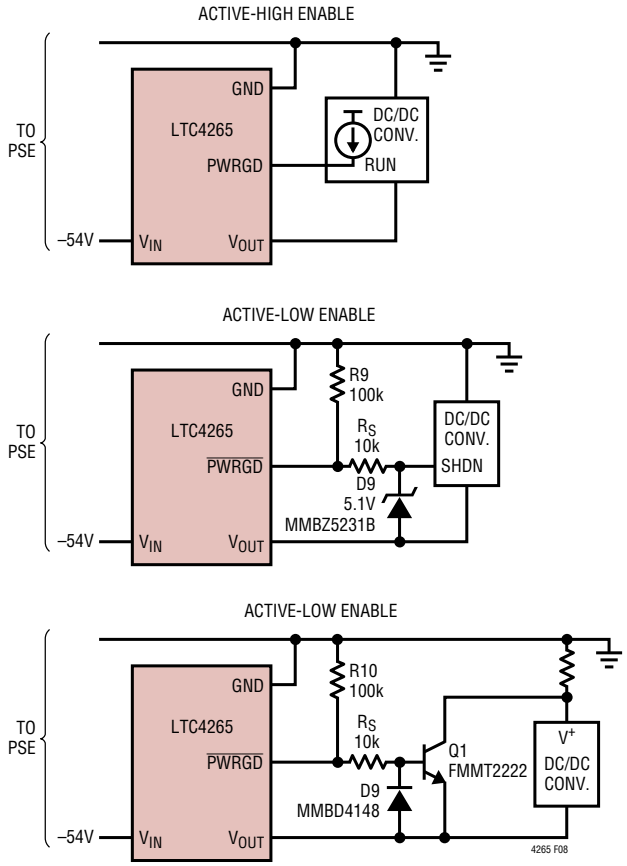


Figure 8. Power Good Interface Examples

T2PSE Interface

When a 2-event Classification sequence successfully completes, the LTC4265 recognizes this sequence, and provides an indicator bit, declaring the presence of a Type-2 PSE. The open drain output provides the option to use this signal to communicate to the LTC4265 load, or to leave the pin unconnected.

Figure 9 shows two interface options using the $\overline{T2PSE}$ pin and the opto-isolator. The $\overline{T2PSE}$ pin is active low and connects to an opt-isolater to communicate across the DC/DC converter isolation barrier. The pull up resistor R_P is sized according to the requirements of the opto-isolator operating current, the pull-down capability of the $\overline{T2PSE}$ pin, and the choice of V^+. V^+ for example can come from the PoE supply rail (which the LTC4265 GND is tied to), or from the voltage source that supplies power to the DC/DC converter. Option 1 has the advantage of not drawing power unless $\overline{T2PSE}$ is declared active.

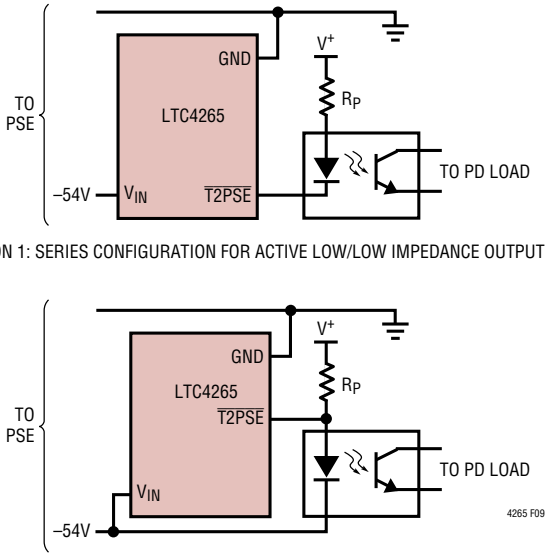


Figure 9. $\overline{T2PSE}$ Interface Examples

APPLICATIONS INFORMATION

Shutdown Interface

To corrupt the signature resistance, the SHDN pin can be driven high with respect to V_{IN} or connected to GND. If unused, connect SHDN directly to V_{IN}.

Exposed Pad

The LTC4265 uses a thermally enhanced DFN12 package that includes an Exposed Pad. The exposed pad must be electrically connected to V_{IN} and must connect to a printed circuit board heat sink.

Auxiliary Power Source

In some applications, it is desirable to power the PD from an auxiliary power source such as a wall adapter.

Auxiliary power can be injected into an LTC4265-based PD at the input of the LTC4265, the output of the LTC4265, or even the output of the DC/DC converter. In addition, some PD application may desire auxiliary supply dominance or may be configured for PoE dominance. Furthermore, PD applications may also opt for a seamless transition — that is, without power disruption — between PoE and auxiliary power.

The most common auxiliary power option injects power between the LTC4265 and the DC/DC converter. Figure 10 presents an example of this application.

In this example, the auxiliary port injects 48V onto the line via diode D1. The components surrounding the SHDN pin are selected so that the LTC4265 disconnects power to the output when the auxiliary supply reaches 36V.

This configuration is an auxiliary-dominant configuration. That is, the auxiliary power source supplies the power even if PoE power is already present. This configuration also provides a seamless transition from PoE to auxiliary power when auxiliary power is applied, however, the removal of auxiliary power to PoE power is not seamless.

Contact Linear Technology applications support for detail information on implementing a custom auxiliary power supply.

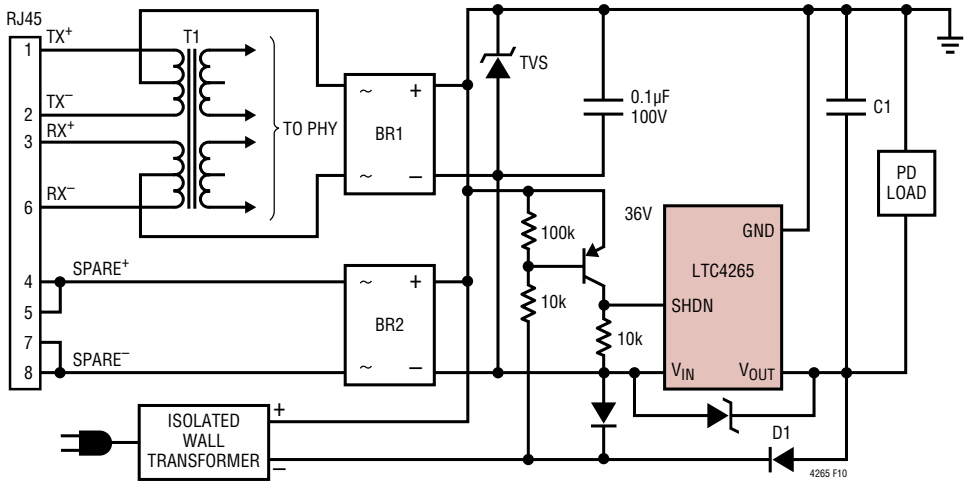


Figure 10. Auxiliary Power Dominant PD Interface

APPLICATIONS INFORMATION

IEEE 802.3at SYSTEM POWER-UP REQUIREMENT

Under the IEEE 802.3at standard, a PD must operate under 13.0 Watts as a Type 1 PD until it recognizes a Type-2 PSE. Initializing PD operation in 13.0-Watt mode eliminates interoperability issue in case a Type-2 PD is connects to a Type-1 PSE. Once the PD recognizes a Type-2 PSE, the IEEE 802.3at standard requires the PD to wait 80ms in 13.0W operation before 25.5W operation can commence.

MAINTAIN POWER SIGNATURE

In an IEEE 802.3af/at system, the PSE uses the maintain power signature (MPS) to determine if a PD continues to require power. The MPS requires the PD to periodically draw at least 10mA and also have an AC impedance less than 26.25k in parallel with 0.05µF. If one of these conditions is not met, the PSE may disconnect power to the PD.

LAYOUT CONSIDERATION FOR THE LTC4265

The LTC4265 is relatively immune to layout problems. Here are some recommendations.

Avoid excessive parasitic capacitance on the R_{CLASS} pin and place resistor R_{CLASS} close to the LTC4265.

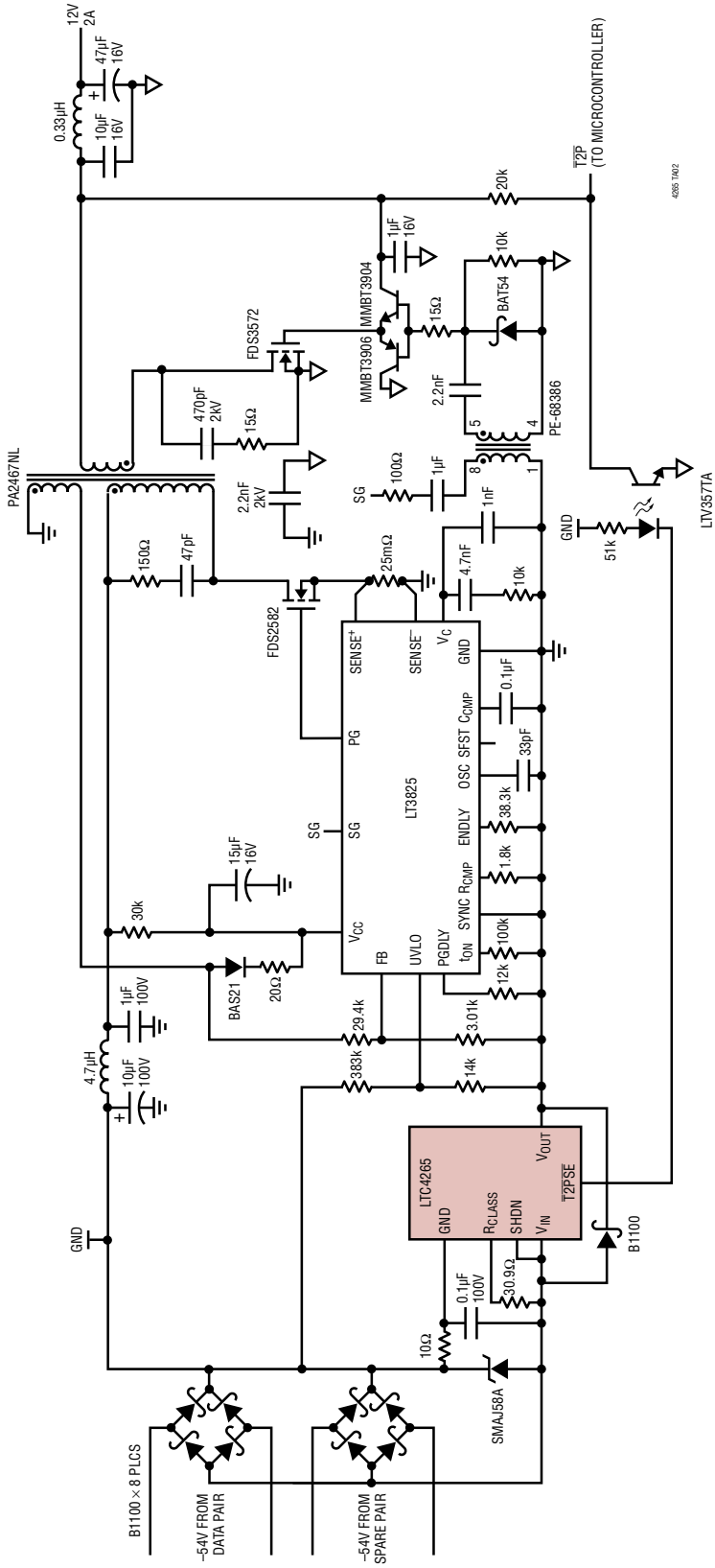
Connect the LTC4265 exposed pad to a PC board heat sink. Make the heat sink as large as possible.

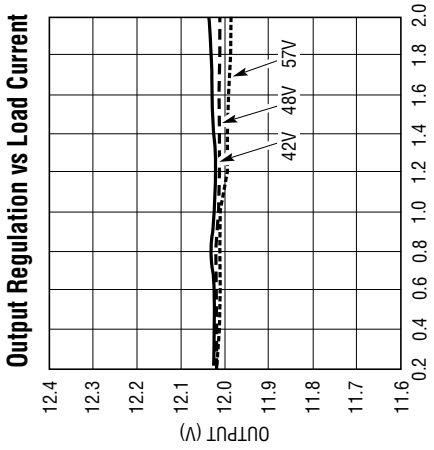
Place the input capacitor and transient voltage suppressor (C14 and D3 in Figure 7) as close to the LTC4265 as possible.

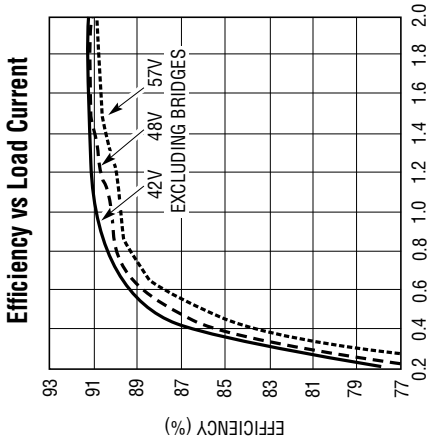
If using the SHDN pin for auxiliary power application, separate the SHDN pin from other high voltage connections, like GND and V_{OUT}, to avoid leakage and capacitive coupling shutting down the LTC4265.

APPLICATIONS INFORMATION

High Efficiency 12V Isolated Power Supply
(Contact LTC for 3.3V and 5V Power Supply Applications)

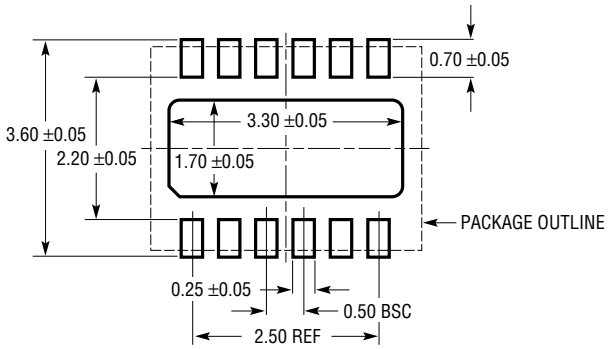




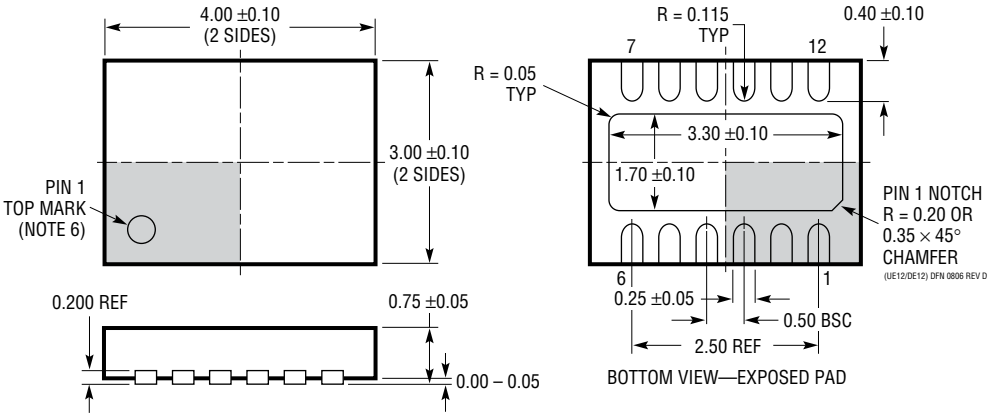


PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



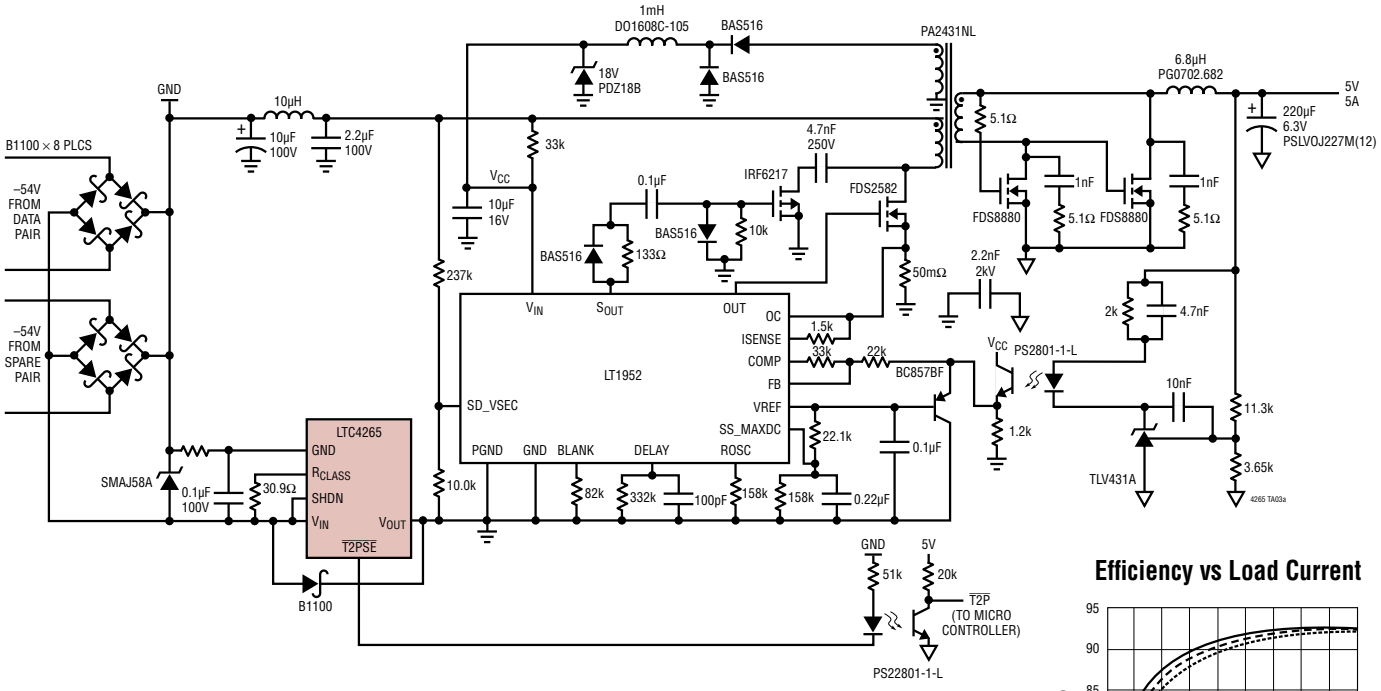
NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION
   (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

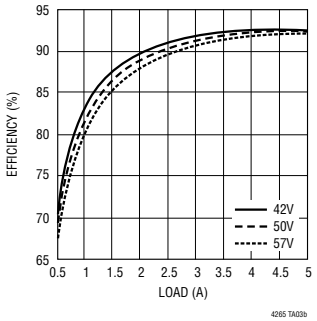
REV	DATE	DESCRIPTION	PAGE NUMBER
B	07/14	Revised Exposed Pad Connection Requirements	2
		Added Note 10 for Overtemperature Protection	3
		Added Input Series Resistance Section. Added SMAJ58A Recommendation	13
		Revised Figure 9 (Option 2)	15
		Revised Figure 10	16
		Revised High Efficiency 12V Isolated Power Supply Schematic	17
		Update DE/UE Package Drawings to Rev. D	19
		Revised PoE-Based Self-Driven Synchronous Forward Power Supply Schematic	20, 22

TYPICAL APPLICATION

PoE-Based Self-Driven Synchronous Forward Power Supply



Efficiency vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4257-1	IEEE 802.3af PD Interface Controller	Internal 100V, 400mA Switch, Dual Current Limit, Programmable Class
LTC4263	Single IEEE 802.3af PSE Controller	Internal FET Switch
LTC4266	Quad IEEE PoE/PoE+/LTPoE++ PSE Controller	With Programmable I_{CUT}/I_{LIM}, 2-Event Classification, Provides Up to 90W
LTC4267-3	IEEE 802.3af PD Interface with Integrated Switching Regulator	Internal 100V, 400mA Switch, Programmable Class, 300kHz Constant Frequency PWM
LTC4269	IEEE 802.3af PD Interface with Integrated Switching Regulator	2-Event Classification, Programmable Class, Synchronous Flyback/Forward Controller, Aux Support
LTC4270/LTC4271	12-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at and LTPoE++ PDs
LTC4274	Single IEEE PoE/PoE+/LTPoE++ PSE Controller	With Programmable I_{CUT}/I_{LIM}, 2-Event Classification, Provides Up to 90W
LT4275	PoE/PoE+/LTPoE++ PD Interface Controller	External MOSFET, Up to 90W, –40°C to 125°C Operation
LTC4278	IEEE 802.3af PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V Aux Support
LTC4290/LTC4271	8-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at and LTPoE++ PDs

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