

Dual/Triple Ultra-Low-Voltage SOT23 μ P Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

| | |
|---|-------------------------------|
| V_{CC1} , V_{CC2} | -0.3V to +6V |
| Open-Drain \overline{RST} , $\overline{RST1}$, $\overline{RST2}$, \overline{PFO} , \overline{RST} | -0.3V to +6V |
| Push-Pull \overline{RST} , $\overline{RST1}$, \overline{PFO} , \overline{RST} | -0.3V to ($V_{CC1} + 0.3V$) |
| Push-Pull $\overline{RST2}$ | -0.3V to ($V_{CC2} + 0.3V$) |
| RSTIN, PFI, MR, WDI | -0.3V to +6V |
| Input Current/Output Current (all pins) | 20mA |

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

| | |
|--|---|
| 5-Pin SOT23-5 (derate 7.1mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$) | 571mW |
| 6-Pin SOT23-6 (derate 8.7mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$) | 696mW |
| 8-Pin SOT23-8 (derate 8.9mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$) | 714mW |
| Operating Temperature Range | -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$ |
| Storage Temperature Range | -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$ |
| Junction Temperature | +150 $^\circ\text{C}$ |
| Lead Temperature (soldering, 10s) | +300 $^\circ\text{C}$ |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC1} = V_{CC2} = 0.8V$ to $5.5V$, $GND = 0$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------|------------|---------------------------------------|-------|-------|-----------------------|---------------|
| Supply Voltage | V_{CC} | | 0.8 | | 5.5 | V |
| Supply Current | I_{CC1} | $V_{CC1} < 5.5V$, all I/O pins open | | 15 | 39 | μA |
| | | $V_{CC1} < 3.6V$, all I/O pins open | | 10 | 28 | |
| | I_{CC2} | $V_{CC2} < 3.6V$, all I/O pins open | | 4 | 11 | |
| | | $V_{CC2} < 2.75V$, all I/O pins open | | 3 | 9 | |
| V_{CC1} Reset Threshold | V_{TH1} | L (falling) | 4.500 | 4.625 | 4.750 | V |
| | | M (falling) | 4.250 | 4.375 | 4.500 | |
| | | T (falling) | 3.000 | 3.075 | 3.150 | |
| | | S (falling) | 2.850 | 2.925 | 3.000 | |
| | | R (falling) | 2.550 | 2.625 | 2.700 | |
| | | Z (falling) | 2.250 | 2.313 | 2.375 | |
| | | Y (falling) | 2.125 | 2.188 | 2.250 | |
| | | W (falling) | 1.620 | 1.665 | 1.710 | |
| V_{CC2} Reset Threshold | V_{TH2} | V (falling) | 1.530 | 1.575 | 1.620 | V |
| | | T (falling) | 3.000 | 3.075 | 3.150 | |
| | | S (falling) | 2.850 | 2.925 | 3.000 | |
| | | R (falling) | 2.550 | 2.625 | 2.700 | |
| | | Z (falling) | 2.250 | 2.313 | 2.375 | |
| | | Y (falling) | 2.125 | 2.188 | 2.250 | |
| | | W (falling) | 1.620 | 1.665 | 1.710 | |
| | | V (falling) | 1.530 | 1.575 | 1.620 | |
| | | I (falling) | 1.350 | 1.388 | 1.425 | |
| | | H (falling) | 1.275 | 1.313 | 1.350 | |
| | | G (falling) | 1.080 | 1.110 | 1.140 | |
| | | F (falling) | 1.020 | 1.050 | 1.080 | |
| | | E (falling) | 0.810 | 0.833 | 0.855 | |
| | | D (falling) | 0.765 | 0.788 | 0.810 | |
| Reset Threshold Tempco | | | 20 | | ppm/ $^\circ\text{C}$ | |
| Reset Threshold Hysteresis | V_{HYST} | Referenced to V_{TH} typical | 0.5 | | % | |

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MAX6715-MAX6729

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC1} = V_{CC2} = 0.8V$ to $5.5V$, $GND = 0$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------------|--|----------------------|----------------------|------|-----------|
| V_{CC} to Reset Output Delay | t_{RD} | $V_{CC1} = (V_{TH1} + 100mV)$ to $(V_{TH1} - 100mV)$ or $V_{CC2} = (V_{TH2} + 75mV)$ to $(V_{TH2} - 75mV)$ | | 20 | | μs |
| Reset Timeout Period | t_{RP} | D1 | 1.1 | 1.65 | 2.2 | ms |
| | | D2 | 8.8 | 13.2 | 17.6 | |
| | | D3 | 140 | 210 | 280 | |
| | | D5 | 280 | 420 | 560 | |
| | | D6 | 560 | 840 | 1120 | |
| | | D4 | 1120 | 1680 | 2240 | |
| ADJUSTABLE RESET COMPARATOR INPUT (MAX6719/MAX6720/MAX6723-MAX6727) | | | | | | |
| RSTIN Input Threshold | V_{RSTIN} | | 611 | 626.5 | 642 | mV |
| RSTIN Input Current | I_{RSTIN} | | -25 | | +25 | nA |
| RSTIN Hysteresis | | | | 3 | | mV |
| RSTIN to Reset Output Delay | t_{RSTIND} | V_{RSTIN} to $(V_{RSTIN} - 30mV)$ | | 22 | | μs |
| POWER-FAIL INPUT (MAX6728/MAX6729) | | | | | | |
| PFI Input Threshold | V_{PFI} | | 611 | 626.5 | 642 | mV |
| PFI Input Current | I_{PFI} | | -25 | | +25 | nA |
| PFI Hysteresis | V_{PFH} | | | 3 | | mV |
| PFI to \overline{PFO} Delay | t_{DPF} | $(V_{PFI} + 30mV)$ to $(V_{PFI} - 30mV)$ | | 2 | | μs |
| MANUAL RESET INPUT (MAX6715-MAX6722/MAX6725-MAX6729) | | | | | | |
| \overline{MR} Input Voltage | V_{IL} | | | $0.3 \times V_{CC1}$ | | V |
| | V_{IH} | | $0.7 \times V_{CC1}$ | | | |
| \overline{MR} Minimum Pulse Width | | | 1 | | | μs |
| \overline{MR} Glitch Rejection | | | | 100 | | ns |
| \overline{MR} to Reset Delay | t_{MR} | | | 200 | | ns |
| \overline{MR} Pullup Resistance | | | 25 | 50 | 80 | $k\Omega$ |
| WATCHDOG INPUT (MAX6721-MAX6729) | | | | | | |
| Watchdog Timeout Period | t_{WD} | First watchdog period after reset timeout period | 35 | 54 | 72 | s |
| | | Normal mode | 1.12 | 1.68 | 2.24 | |
| WDI Pulse Width | t_{WDI} | (Note 2) | 50 | | | ns |
| WDI Input Voltage | V_{IL} | | | $0.3 \times V_{CC1}$ | | V |
| | V_{IH} | | $0.7 \times V_{CC1}$ | | | |
| WDI Input Current | I_{WDI} | WDI = 0 or V_{CC1} | -1 | | +1 | μA |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC1} = V_{CC2} = 0.8V$ to $5.5V$, $GND = 0$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------|--|----------------------|-----|-----|---------|
| RESET/POWER-FAIL OUTPUTS | | | | | | |
| $\overline{RST}/\overline{RST1}/\overline{RST2}/\overline{PFO}$ Output LOW (Push-Pull or Open-Drain) | V_{OL} | V_{CC1} or $V_{CC2} \geq 0.8V$, $I_{SINK} = 1\mu A$, output asserted | | | 0.3 | V |
| | | V_{CC1} or $V_{CC2} \geq 1.0V$, $I_{SINK} = 50\mu A$, output asserted | | | 0.3 | |
| | | V_{CC1} or $V_{CC2} \geq 1.2V$, $I_{SINK} = 100\mu A$, output asserted | | | 0.3 | |
| | | V_{CC1} or $V_{CC2} \geq 2.7V$, $I_{SINK} = 1.2mA$, output asserted | | | 0.3 | |
| | | V_{CC1} or $V_{CC2} \geq 4.5V$, $I_{SINK} = 3.2mA$, output asserted | | | 0.4 | |
| $\overline{RST}/\overline{RST1}/\overline{PFO}$ Output HIGH (Push-Pull Only) | V_{OH} | $V_{CC1} \geq 1.8V$, $I_{SOURCE} = 200\mu A$, output not asserted | $0.8 \times V_{CC1}$ | | | V |
| | | $V_{CC1} \geq 2.7V$, $I_{SOURCE} = 500\mu A$, output not asserted | $0.8 \times V_{CC1}$ | | | |
| | | $V_{CC1} \geq 4.5V$, $I_{SOURCE} = 800\mu A$, output not asserted | $0.8 \times V_{CC1}$ | | | |
| $\overline{RST2}$ Output HIGH (Push-Pull Only) | V_{OH} | $V_{CC2} \geq 1.8V$, $I_{SOURCE} = 200\mu A$, output not asserted | $0.8 \times V_{CC2}$ | | | V |
| | | $V_{CC2} \geq 2.7V$, $I_{SOURCE} = 500\mu A$, output not asserted | $0.8 \times V_{CC2}$ | | | |
| | | $V_{CC2} \geq 4.5V$, $I_{SOURCE} = 800\mu A$, output not asserted | $0.8 \times V_{CC2}$ | | | |
| RST Output HIGH (Push-Pull Only) | V_{OH} | $V_{CC1} \geq 1.0V$, $I_{SOURCE} = 1\mu A$, reset asserted | $0.8 \times V_{CC1}$ | | | V |
| | | $V_{CC1} \geq 1.8V$, $I_{SOURCE} = 150\mu A$, reset asserted | $0.8 \times V_{CC1}$ | | | |
| | | $V_{CC1} \geq 2.7V$, $I_{SOURCE} = 500\mu A$, reset asserted | $0.8 \times V_{CC1}$ | | | |
| | | $V_{CC1} \geq 4.5V$, $I_{SOURCE} = 800\mu A$, reset asserted | $0.8 \times V_{CC1}$ | | | |
| RST Output LOW (Push-Pull or Open Drain) | V_{OL} | V_{CC1} or $V_{CC2} \geq 1.8V$, $I_{SINK} = 500\mu A$, reset not asserted | | | 0.3 | V |
| | | V_{CC1} or $V_{CC2} \geq 2.7V$, $I_{SINK} = 1.2mA$, reset not asserted | | | 0.3 | |
| | | V_{CC1} or $V_{CC2} \geq 4.5V$, $I_{SINK} = 3.2mA$, reset not asserted | | | 0.4 | |
| $\overline{RST}/\overline{RST1}/\overline{RST2}/\overline{PFO}$ Output Open-Drain Leakage Current | | Output not asserted | | | 0.5 | μA |
| RST Output Open-Drain Leakage Current | | Output asserted | | | 0.5 | μA |

Note 1: Devices tested at $+25^{\circ}C$. Overtemperature limits are guaranteed by design and not production tested.

Note 2: Parameter guaranteed by design.

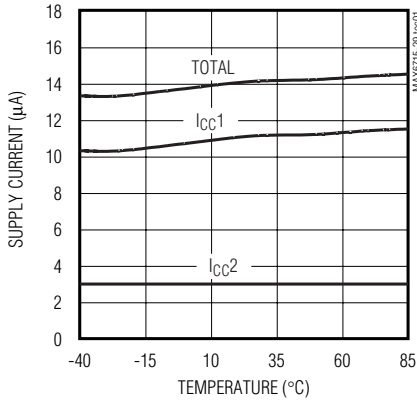
Dual/Triple Ultra-Low-Voltage SOT23 μ P Supervisory Circuits

Typical Operating Characteristics

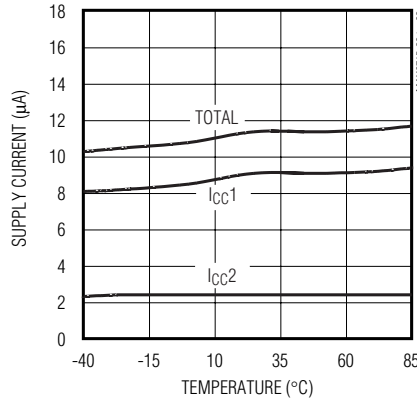
($V_{CC1} = 5V$, $V_{CC2} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX6715-MAX6729

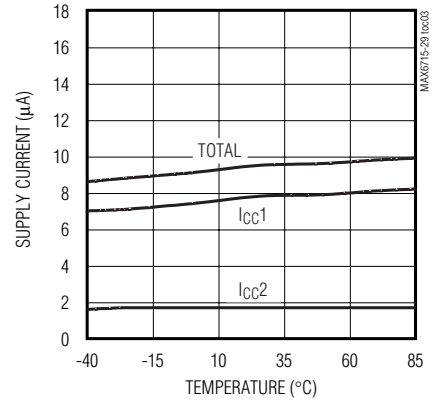
SUPPLY CURRENT vs. TEMPERATURE
 $V_{CC1} = 5V$, $V_{CC2} = 3.3V$



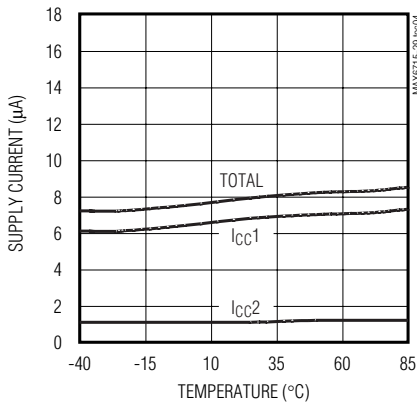
SUPPLY CURRENT vs. TEMPERATURE
 $V_{CC1} = 3.3V$, $V_{CC2} = 2.5V$



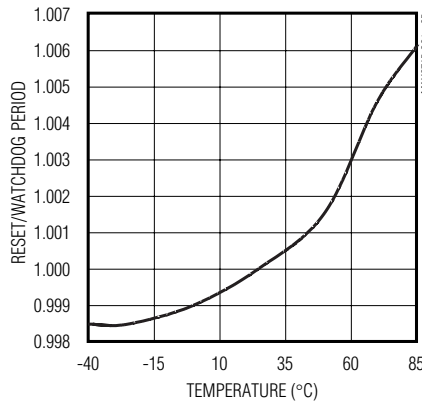
SUPPLY CURRENT vs. TEMPERATURE
 $V_{CC1} = 2.5V$, $V_{CC2} = 1.8V$



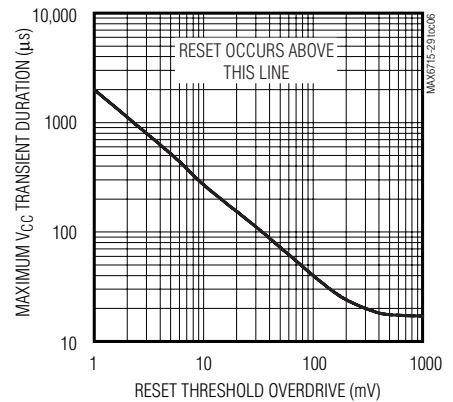
SUPPLY CURRENT vs. TEMPERATURE
 $V_{CC1} = 1.8V$, $V_{CC2} = 1.2V$



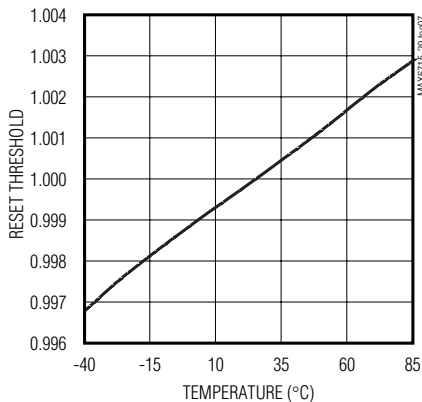
NORMALIZED RESET/WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



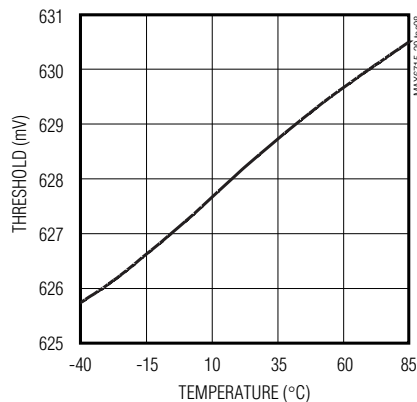
MAXIMUM V_{CC} TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



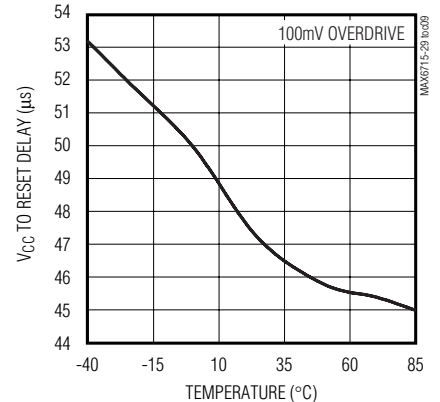
NORMALIZED V_{CC} RESET THRESHOLD vs. TEMPERATURE



RESET INPUT AND POWER-FAIL INPUT THRESHOLD vs. TEMPERATURE



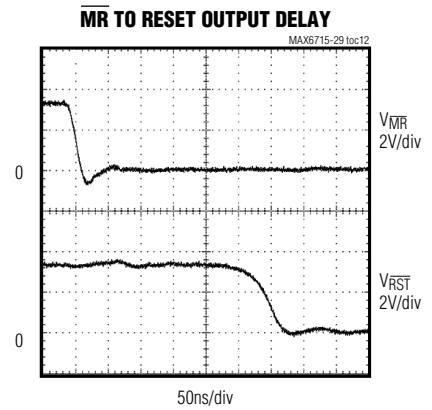
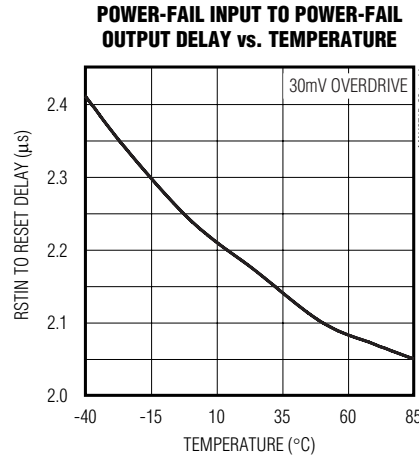
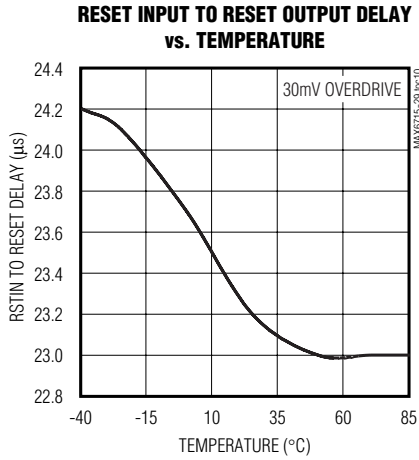
V_{CC} TO RESET DELAY vs. TEMPERATURE



Dual/Triple Ultra-Low-Voltage SOT23 μ P Supervisory Circuits

Typical Operating Characteristics (continued)

($V_{CC1} = 5V$, $V_{CC2} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

| PIN | | | | | | | | NAME | FUNCTION |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------|---------------------|-----------------------|---|
| MAX6715/ MAX6716 | MAX6717/ MAX6718 | MAX6719/ MAX6720 | MAX6721/ MAX6722 | MAX6723/ MAX6724 | MAX6725/ MAX6726 | MAX6727 | MAX6728/ MAX6729 | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1, 4 | 1 | $\overline{RST}/RST1$ | Active-Low Reset Output, Open-Drain or Push-Pull. $\overline{RST}/RST1$ changes from high to low when V_{CC1} or V_{CC2} drops below the selected reset thresholds, $RSTIN$ is below threshold, \overline{MR} is pulled low, or the watchdog triggers a reset. $\overline{RST}/RST1$ remains low for the reset timeout period after $V_{CC1}/V_{CC2}/RSTIN$ exceed the device reset thresholds, \overline{MR} goes low to high, or the watchdog triggers a reset. Open-drain outputs require an external pullup resistor. Push-pull outputs are referenced to V_{CC1} . |

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Pin Description (continued)

MAX6715-MAX6729

| PIN | | | | | | | | NAME | FUNCTION |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------|---------------------|--------------------------|--|
| MAX6715/ MAX6716 | MAX6717/ MAX6718 | MAX6719/ MAX6720 | MAX6721/ MAX6722 | MAX6723/ MAX6724 | MAX6725/ MAX6726 | MAX6727 | MAX6728/ MAX6729 | | |
| 5 | — | — | — | — | — | — | — | $\overline{\text{RST2}}$ | Active-Low Reset Output, Open-Drain or Push-Pull. $\overline{\text{RST2}}$ changes from high to low when V_{CC1} or V_{CC2} drops below the selected reset thresholds or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RST2}}$ remains low for the reset timeout period after $V_{\text{CC1}}/V_{\text{CC2}}$ exceed the device reset thresholds or $\overline{\text{MR}}$ goes low to high. Open-drain outputs require an external pullup resistor. Push-pull outputs are referenced to V_{CC2} . |
| 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | GND | Ground |
| 3 | 3 | 3 | 3 | — | 5 | 5 | 5 | $\overline{\text{MR}}$ | Active-Low Manual Reset Input. Internal 50k Ω pullup to V_{CC1} . Pull low to force a reset. Reset remains active as long as $\overline{\text{MR}}$ is low and for the reset timeout period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to V_{CC1} if unused. |
| 4 | 4 | 4 | 4 | 4 | 6 | 6 | 6 | V_{CC2} | Secondary Supply Voltage Input. Powers the device when it is above V_{CC1} and input for secondary reset threshold monitor. |
| 6 | 5 | 6 | 6 | 6 | 8 | 8 | 8 | V_{CC1} | Primary Supply Voltage Input. Powers the device when it is above V_{CC2} and input for primary reset threshold monitor. |

Dual/Triple Ultra-Low-Voltage SOT23 μ P Supervisory Circuits

MAX6715-MAX6729

Pin Description (continued)

| PIN | | | | | | | | NAME | FUNCTION |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------|---------------------|-------|--|
| MAX6715/ MAX6716 | MAX6717/ MAX6718 | MAX6719/ MAX6720 | MAX6721/ MAX6722 | MAX6723/ MAX6724 | MAX6725/ MAX6726 | MAX6727 | MAX6728/ MAX6729 | | |
| — | — | — | 5 | 3 | 3 | 3 | 3 | WDI | Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and the reset output asserts for the reset timeout period. The internal watchdog timer clears whenever a reset is asserted or WDI sees a rising or falling edge. The watchdog has a long timeout period (35s min) after each reset event and a short timeout period (1.12s min) after the first valid WDI transition. |
| — | — | 5 | — | 5 | 7 | 7 | — | RSTIN | Undervoltage Reset Comparator Input. High-impedance input for adjustable reset monitor. The reset output is asserted when RSTIN falls below the 0.626V internal reference voltage. Set the monitored voltage reset threshold with an external resistor-divider network. Connect RSTIN to V _{CC1} or V _{CC2} if not used. |
| — | — | — | — | — | — | — | 7 | PFI | Power-Fail Voltage Monitor Input. High-impedance input for internal power-fail monitor comparator. Connect PFI to an external resistor-divider network to set the power-fail threshold voltage (0.626V typical internal reference voltage). Connect to GND, V _{CC1} , or V _{CC2} if not used. |

Dual/Triple Ultra-Low-Voltage SOT23 μ P Supervisory Circuits

Pin Description (continued)

MAX6715-MAX6729

| PIN | | | | | | | | NAME | FUNCTION |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------|---------------------|------|---|
| MAX6715/ MAX6716 | MAX6717/ MAX6718 | MAX6719/ MAX6720 | MAX6721/ MAX6722 | MAX6723/ MAX6724 | MAX6725/ MAX6726 | MAX6727 | MAX6728/ MAX6729 | | |
| — | — | — | — | — | — | — | 4 | PFO | Active-Low Power-Fail Monitor Output, Open-Drain or Push-Pull. PFO is asserted low when PFI is less than 0.626V. PFO deasserts without a reset timeout period. Open-drain outputs require an external pullup resistor. Push-pull outputs are referenced to VCC1. |
| — | — | — | — | — | 4 | — | — | RST | Active-High Reset Output, Open-Drain or Push-Pull. RST changes from low to high when VCC1 or VCC2 drops below selected reset thresholds, RSTIN is below threshold, MR is pulled low, or the watchdog triggers a reset. RST remains HIGH for the reset timeout period after VCC1/VCC2/RSTIN exceed the device reset thresholds, MR goes low to high, or the watchdog triggers a reset. Open-drain outputs require an external pullup resistor. Push-pull outputs are referenced to VCC1. |

Detailed Description

Supply Voltages

The MAX6715–MAX6729 microprocessor (μ P) supervisory circuits maintain system integrity by alerting the μ P to fault conditions. These ICs are optimized for systems that monitor two or three supply voltages. The output-reset state is guaranteed to remain valid while either VCC1 or VCC2 is above 0.8V.

Threshold Levels

Input voltage threshold level combinations are indicated by a two-letter code in the *Reset Voltage Threshold*

Suffix Guide (Table 1). Contact factory for availability of other voltage threshold combinations.

Reset Outputs

The MAX6715–MAX6729 provides an active-low reset output (RST) and the MAX6725/MAX6726 provides both an active-high (RST) and an active-low reset output (RST). RST, RST, RST1, and RST2 are asserted when the voltage at either VCC1 or VCC2 falls below the voltage threshold level, RSTIN drops below threshold, or MR is pulled low. Once reset is asserted it stays low for the reset timeout period (see Table 2). If VCC1, VCC2, or RSTIN goes below the reset threshold before the reset timeout period is completed, the internal timer

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restarts. The MAX6715/MAX6717/MAX6719/MAX6721/MAX6723/MAX6725/MAX6727/MAX6728 contain open-drain reset outputs, while the MAX6716/MAX6718/MAX6720/MAX6722/MAX6724/MAX6726/MAX6729 contain push-pull reset outputs. The MAX6727 provides two separate open-drain $\overline{\text{RST}}$ outputs driven by the same internal logic.

Manual Reset Input

Many microprocessor-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{\text{MR}}$ asserts the reset output. Reset remains asserted while $\overline{\text{MR}}$ is low and for the reset timeout period (t_{RP}) after $\overline{\text{MR}}$ returns high. This input has an internal 50k Ω pullup resistor to V_{CC1} and can be left unconnected if not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in a noisy environment, connect a 0.1 μF capacitor from $\overline{\text{MR}}$ to GND to provide additional noise immunity.

Adjustable Input Voltage

The MAX6719/MAX6720 and MAX6723-MAX6727 provide an additional input to monitor a third system voltage. The threshold voltage at RSTIN is typically 626mV. Connect a resistor-divider network to the circuit as shown in Figure 1 to establish an externally controlled threshold voltage, $V_{\text{EXT_TH}}$.

$$V_{\text{EXT_TH}} = 626\text{mV} \cdot ((R1 + R2)/R2)$$

Low leakage current at RSTIN allows the use of large-valued resistors resulting in reduced power consumption of the system.

Watchdog Input

The watchdog monitors μP activity through the watchdog input (WDI). To use the watchdog function, connect WDI to a bus line or μP I/O line. When WDI remains high or low for longer than the watchdog timeout period, the reset output asserts.

The MAX6721-MAX6729 include a dual-mode watchdog timer to monitor μP activity. The flexible timeout architecture provides a long period initial watchdog mode, allowing complicated systems to complete lengthy boots, and a short period normal watchdog mode, allowing the supervisor to provide quick alerts

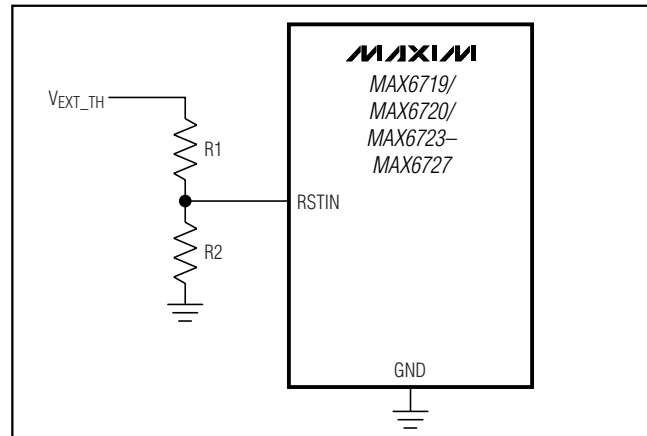


Figure 1. Monitoring a Third Voltage

when processor activity fails. After each reset event (V_{CC} power-up/brownout, manual reset, or watchdog reset), there is a long initial watchdog period of 35s minimum. The long watchdog period mode provides an extended time for the system to power-up and fully initialize all μP and system components before assuming responsibility for routine watchdog updates.

The normal watchdog timeout period (1.12s min) begins after the first transition on WDI before the conclusion of the long initial watchdog period (Figure 2). During the normal operating mode, the supervisor will issue a reset pulse for the reset timeout period if the μP does not update the WDI with a valid transition (high-to-low or low-to-high) within the standard timeout period (1.12s min).

Power-Fail Comparator

PFI is the noninverting input to a comparator. If PFI is less than V_{PFI} (626.5mV), PFO goes low. Common uses for the power-fail comparator include monitoring preregulated input of the power supply (such as a battery) or

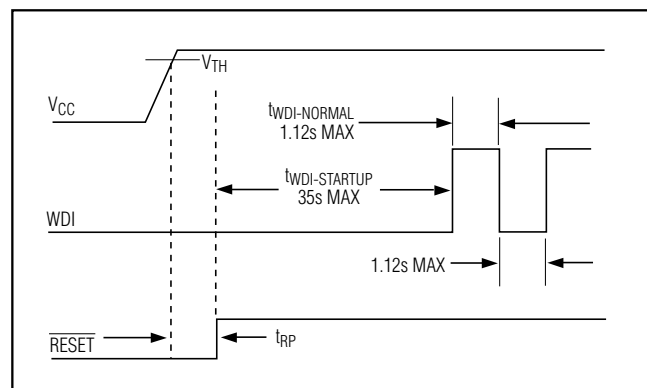


Figure 2. Normal Watchdog Startup Sequence

Dual/Triple Ultra-Low-Voltage SOT23 μ P Supervisory Circuits

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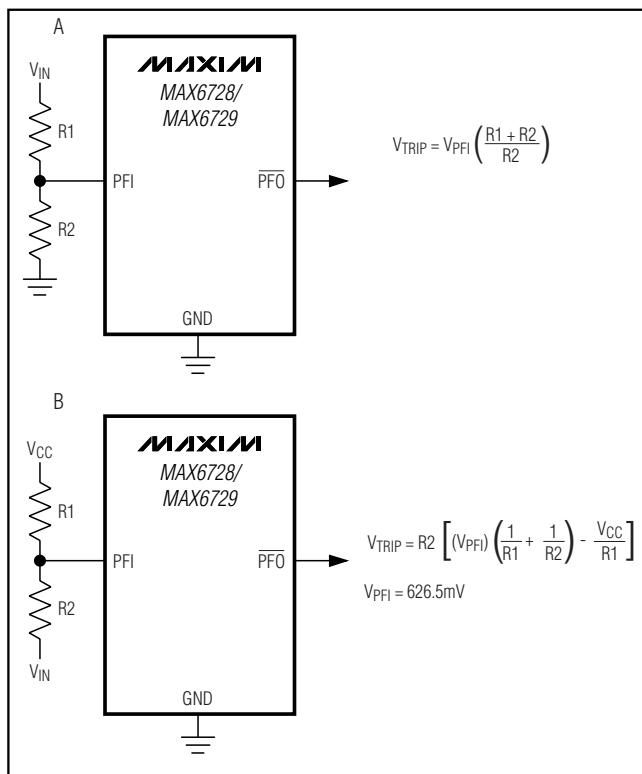


Figure 3. Using Power-Fail Input to Monitor an Additional Power-Supply a) V_{IN} is Positive b) V_{IN} is Negative

providing an early power-fail warning so software can conduct an orderly system shutdown. It can also be used to monitor supplies other than V_{CC1} or V_{CC2} by setting the power-fail threshold with a resistor-divider, as shown in Figure 3. PFI is the input to the power-fail comparator. The typical comparator delay is 2μ s from PFI to \overline{PFO} . Connect PFI to ground of V_{CC1} if unused.

Ensuring a Valid Reset Output Down to $V_{CC} = 0$

The MAX6715-MAX6729 are guaranteed to operate properly down to $V_{CC} = 0.8V$. In applications that require valid reset levels down to $V_{CC} = 0$ use a pull-down resistor at \overline{RST} to ground. The resistor value used is not critical, but it must be large enough not to load the reset output when V_{CC} is above the reset threshold. For most applications, $100k\Omega$ is adequate. This configuration does not work for the open-drain outputs of the MAX6715/MAX6717/MAX6719/MAX6721/MAX6723/MAX6725/MAX6727/MAX6728. For push-pull, active-high \overline{RST} output connect the external resistor as a pullup from \overline{RST} to V_{CC1} .

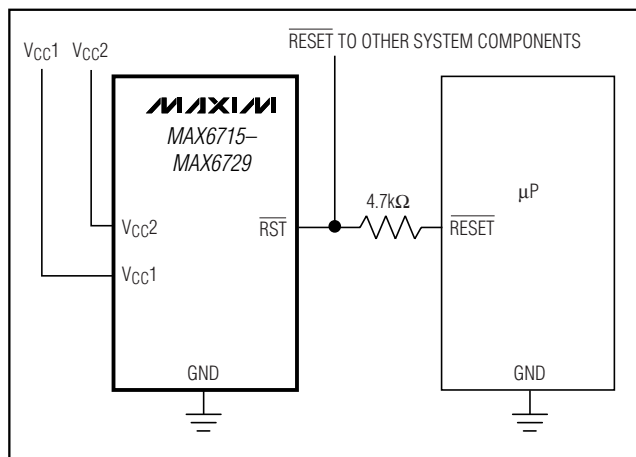


Figure 4. Interfacing to μ Ps with Bidirectional Reset I/O

Applications Information

Interfacing to μ Ps with Bidirectional Reset Pins

Most microprocessors with bidirectional reset pins can interface directly to open-drain \overline{RST} output options. Systems simultaneously requiring a push-pull \overline{RST} output and a bidirectional reset interface can be in logic contention. To prevent contention, connect a $4.7k\Omega$ resistor between \overline{RST} and the μ P's reset I/O port as shown in Figure 4.

Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of $3mV$. This is sufficient for most applications where a power-supply line is being monitored through an external voltage-divider (see the *Power-Fail Comparator* section). If additional noise margin is desired, connect a resistor between \overline{PFO} and PFI as shown in Figure 5. Select the values of R_1 , R_2 , and R_3 so PFI sees V_{PFI} ($626mV$) when V_{EXT} falls to its power-fail trip point (V_{FAIL}) and when V_{IN} rises to its power-good trip point (V_{GOOD}). The hysteresis window extends between the specified V_{FAIL} and V_{GOOD} thresholds. R_3 adds the additional hysteresis by sinking current from the R_1/R_2 divider network when \overline{PFO} is logic low and sourcing current into the network when \overline{PFO} is logic high. R_3 is typically an order of magnitude greater than R_1 or R_2 .

The current through R_2 should be at least $2.5\mu A$ to ensure that the $25nA$ (max) PFI input current does not significantly shift the trip points. Therefore, $R_2 < V_{PFI}/2.5\mu A < 248k\Omega$ for most applications. R_3 will provide additional hysteresis for \overline{PFO} push-pull ($V_{OH} = V_{CC1}$) or open-drain ($V_{OH} = V_{PULLUP}$) applications.

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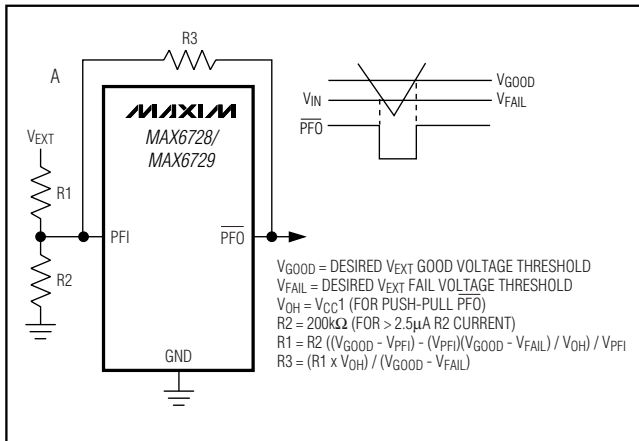


Figure 5. Adding Hysteresis to Power-Fail for Push-Pull PFO

Monitoring an Additional Power Supply

These μ P supervisors can monitor either positive or negative supplies using a resistor voltage-divider to PFI. \overline{PFO} can be used to generate an interrupt to the μ P or cause reset to assert (Figure 3).

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit shown in Figure 3. When the negative supply is valid, \overline{PFO} is low. When the negative supply voltage drops, \overline{PFO} goes high. The circuit's accuracy is affected by the PFI threshold tolerance, V_{CC} , $R1$, and $R2$.

Negative-Going V_{CC} Transients

The MAX6715-MAX6729 supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the μ P when V_{CC} experiences only small glitches. The *Typical Operating Characteristics* show Maximum Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going V_{CC} pulses, starting above V_{TH} and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. A $0.1\mu F$ bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Watchdog Software Considerations

Setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low, helps the

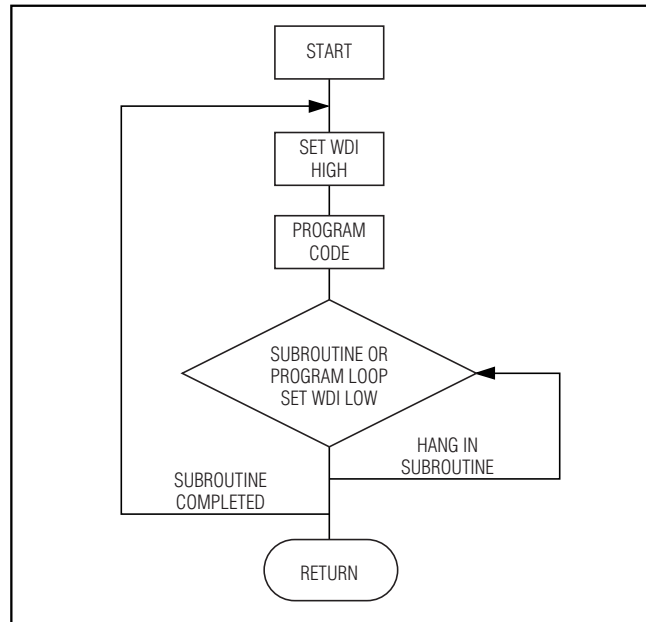


Figure 6. Watchdog Flow Diagram

watchdog timer to closely monitor software execution. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 6 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

Chip Information

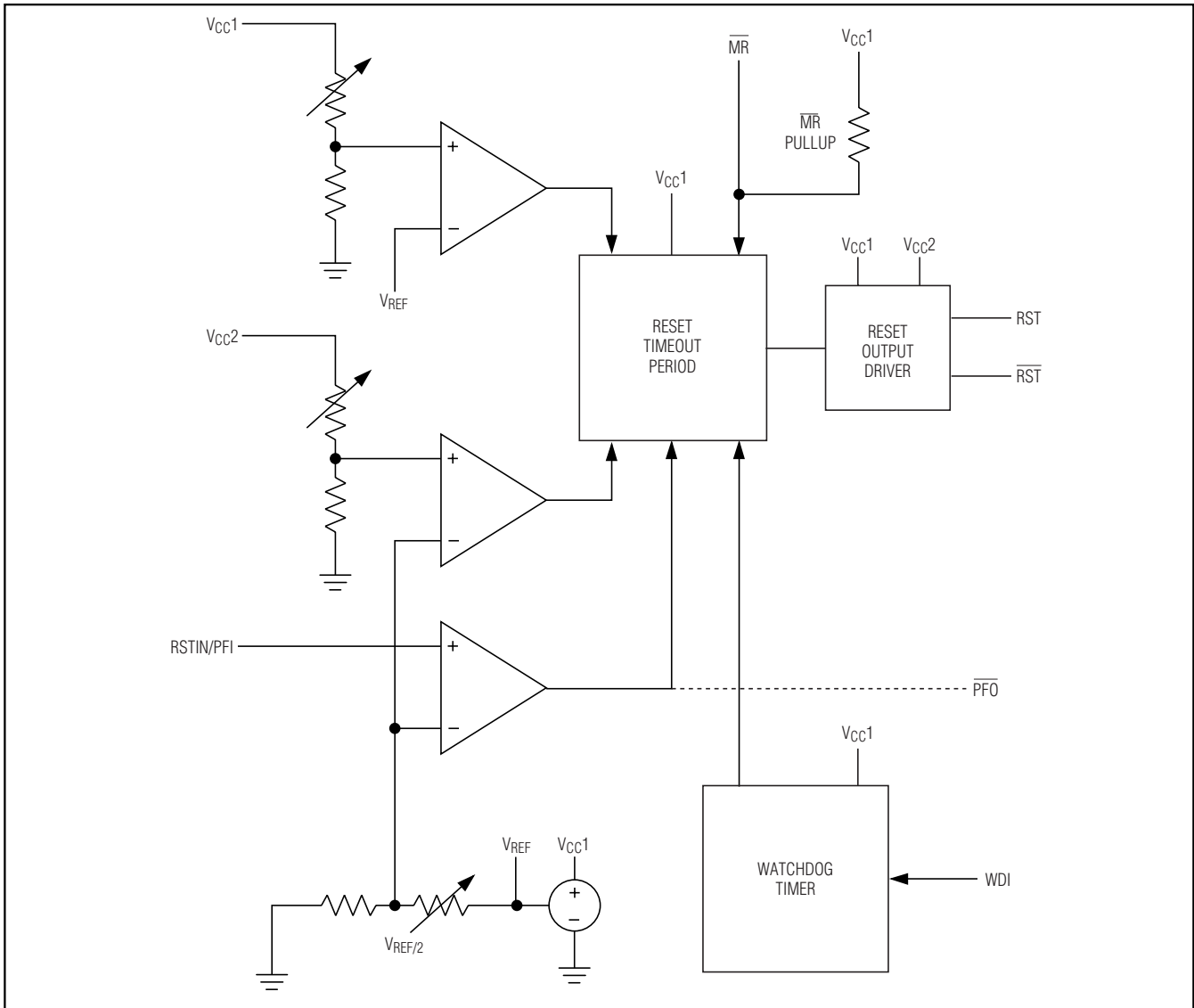
TRANSISTOR COUNT: 1072

PROCESS: BiCMOS

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Functional Diagram

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Selector Guide

| PART NUMBER | NUMBER OF VOLTAGE MONITORS | OPEN-DRAIN RESET | OPEN-DRAIN RESET | PUSH-PULL RESET | PUSH-PULL RESET | MANUAL RESET | WATCH-DOG INPUT | POWER-FAIL INPUT/OUTPUT |
|-------------|----------------------------|------------------|------------------|-----------------|-----------------|--------------|-----------------|-------------------------|
| MAX6715 | 2 | 2 | — | — | — | √ | — | — |
| MAX6716 | 2 | — | — | 2 | — | √ | — | — |
| MAX6717 | 2 | 1 | — | — | — | √ | — | — |
| MAX6718 | 2 | — | — | 1 | — | √ | — | — |
| MAX6719 | 3 | 1 | — | — | — | √ | — | — |
| MAX6720 | 3 | — | — | 1 | — | √ | — | — |
| MAX6721 | 2 | 1 | — | — | — | √ | √ | — |
| MAX6722 | 2 | — | — | 1 | — | √ | √ | — |
| MAX6723 | 3 | 1 | — | — | — | — | √ | — |
| MAX6724 | 3 | — | — | 1 | — | — | √ | — |
| MAX6725 | 3 | 1 | 1 | — | — | √ | √ | — |
| MAX6726 | 3 | — | — | 1 | 1 | √ | √ | — |
| MAX6727 | 3 | 2 | — | — | — | √ | √ | — |
| MAX6728 | 3 | 1 | — | — | — | √ | √ | √ (open drain) |
| MAX6729 | 3 | — | — | 1 | — | √ | √ | √ (push-pull) |

Ordering Information (continued)

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------------|----------------|-------------|
| MAX6721UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6722UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6723UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6724UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6725KA__D_-T | -40°C to +85°C | 8 SOT23-8 |
| MAX6726KA__D_-T | -40°C to +85°C | 8 SOT23-8 |
| MAX6727KA__D_-T | -40°C to +85°C | 8 SOT23-8 |
| MAX6728KA__D_-T | -40°C to +85°C | 8 SOT23-8 |
| MAX6729KA__D_-T | -40°C to +85°C | 8 SOT23-8 |

Note: The first “_” are placeholders for the threshold voltage levels of the devices. Desired threshold levels are set by the part number suffix found in the Reset Voltage Threshold Suffix Guide. The “_” after the D is a placeholder for the reset timeout delay time. Desired delay time is set using the timeout period suffix found in the Reset Timeout Period Suffix Guide. For example the MAX6716UTLTD3-T is a dual-voltage supervisor $V_{TH1} = 4.625V$, $V_{TH2} = 3.075V$, and 210ms (typ) timeout period.

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing “-T” with “+T” when ordering.

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Table 1. Reset Voltage Threshold Suffix Guide**

| PART NUMBER SUFFIX (_) | V _{CC1} NOMINAL VOLTAGE THRESHOLD (V) | V _{CC2} NOMINAL VOLTAGE THRESHOLD (V) |
|--------------------------|--|--|
| | | |
| MS | 4.375 | 2.925 |
| MR | 4.375 | 2.625 |
| TZ | 3.075 | 2.313 |
| SY | 2.925 | 2.188 |
| RY | 2.625 | 2.188 |
| TW | 3.075 | 1.665 |
| SV | 2.925 | 1.575 |
| RV | 2.625 | 1.575 |
| TI | 3.075 | 1.388 |
| SH | 2.925 | 1.313 |
| RH | 2.625 | 1.313 |
| TG | 3.075 | 1.110 |
| SF | 2.925 | 1.050 |
| RF | 2.625 | 1.050 |
| TE | 3.075 | 0.833 |
| SD | 2.925 | 0.788 |
| RD | 2.625 | 0.788 |
| ZW | 2.313 | 1.665 |
| YV | 2.188 | 1.575 |
| ZI | 2.313 | 1.388 |
| YH | 2.188 | 1.313 |
| ZG | 2.313 | 1.110 |
| YF | 2.188 | 1.050 |
| ZE | 2.313 | 0.833 |
| YD | 2.188 | 0.788 |
| WI | 1.665 | 1.388 |
| VH | 1.575 | 1.313 |
| WG | 1.665 | 1.110 |
| VF | 1.575 | 1.050 |
| WE | 1.665 | 0.833 |
| VD | 1.575 | 0.788 |

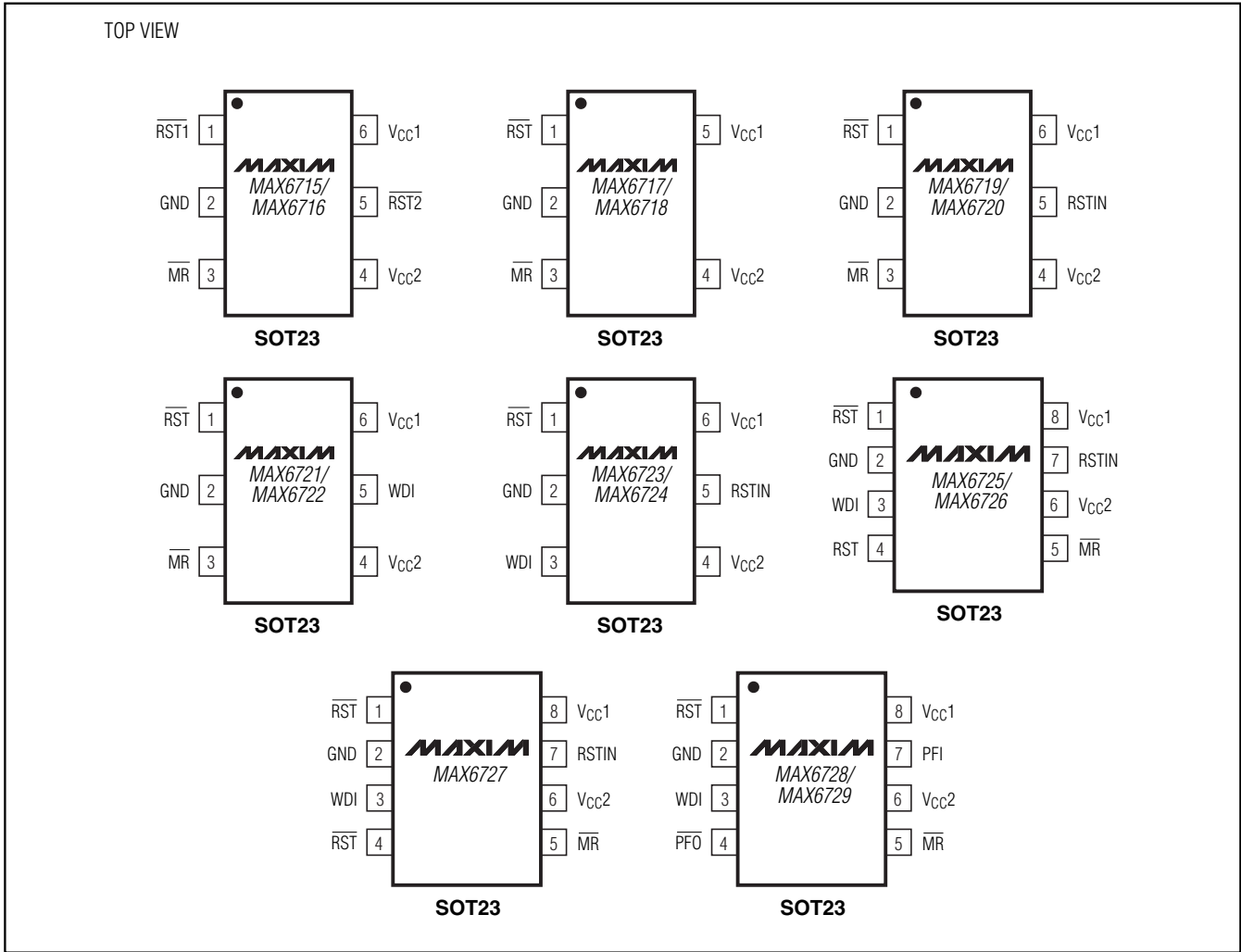
Standard versions are shown in bold and are available in a D3 timeout option only. Standard versions require 2,500 piece order increments and are typically held in sample stock. There is a 10,000 order increment on nonstandard versions. **Other threshold voltages may be available, contact factory for availability.

Table 2. Reset Timeout Period Suffix Guide

| TIMEOUT PERIOD SUFFIX | ACTIVE TIMEOUT PERIOD | |
|-----------------------|-----------------------|----------|
| | MIN [ms] | MAX [ms] |
| D1 | 1.1 | 2.2 |
| D2 | 8.8 | 17.6 |
| D3 | 140 | 280 |
| D5 | 280 | 560 |
| D6 | 560 | 1120 |
| D4 | 1120 | 2240 |

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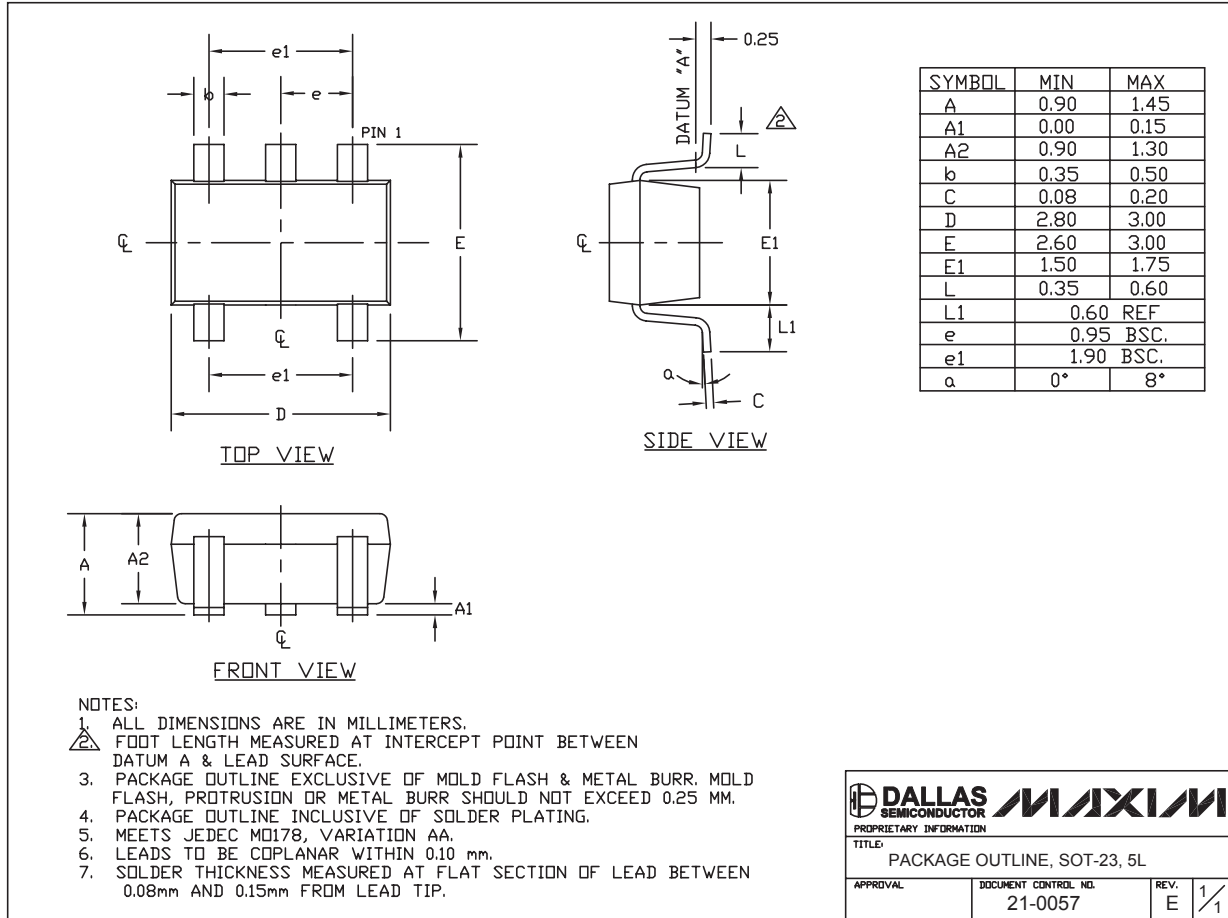
Pin Configurations



Dual/Triple Ultra-Low-Voltage SOT23 μ P Supervisory Circuits

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



SOT-23 5L .EPS

MAX6715-MAX6729

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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

| SYMBOL | MIN | MAX |
|--------|------|------|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.35 | 0.50 |
| C | 0.08 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.35 | 0.60 |
| L1 | 0.60 | REF. |
| e1 | 1.90 | BSC. |
| e | 0.95 | BSC. |
| a | 0° | 10° |

NOTES:
 1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
 3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
 4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
 5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
 6. PIN 1 I.D. DOT IS 0.3 MM ϕ MIN, LOCATED ABOVE PIN 1.
 7. MEETS JEDEC MO17B, VARIATION AB.
 8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
 9. LEAD TO BE COPLANAR WITHIN 0.1 MM.

DALLAS SEMICONDUCTOR MAXIM
 TITLE: PACKAGE OUTLINE, SOT 6L BODY
 APPROVAL: _____ DOCUMENT CONTRL. NO. 21-0058 REV. G 1/1

-DRAWING NOT TO SCALE-

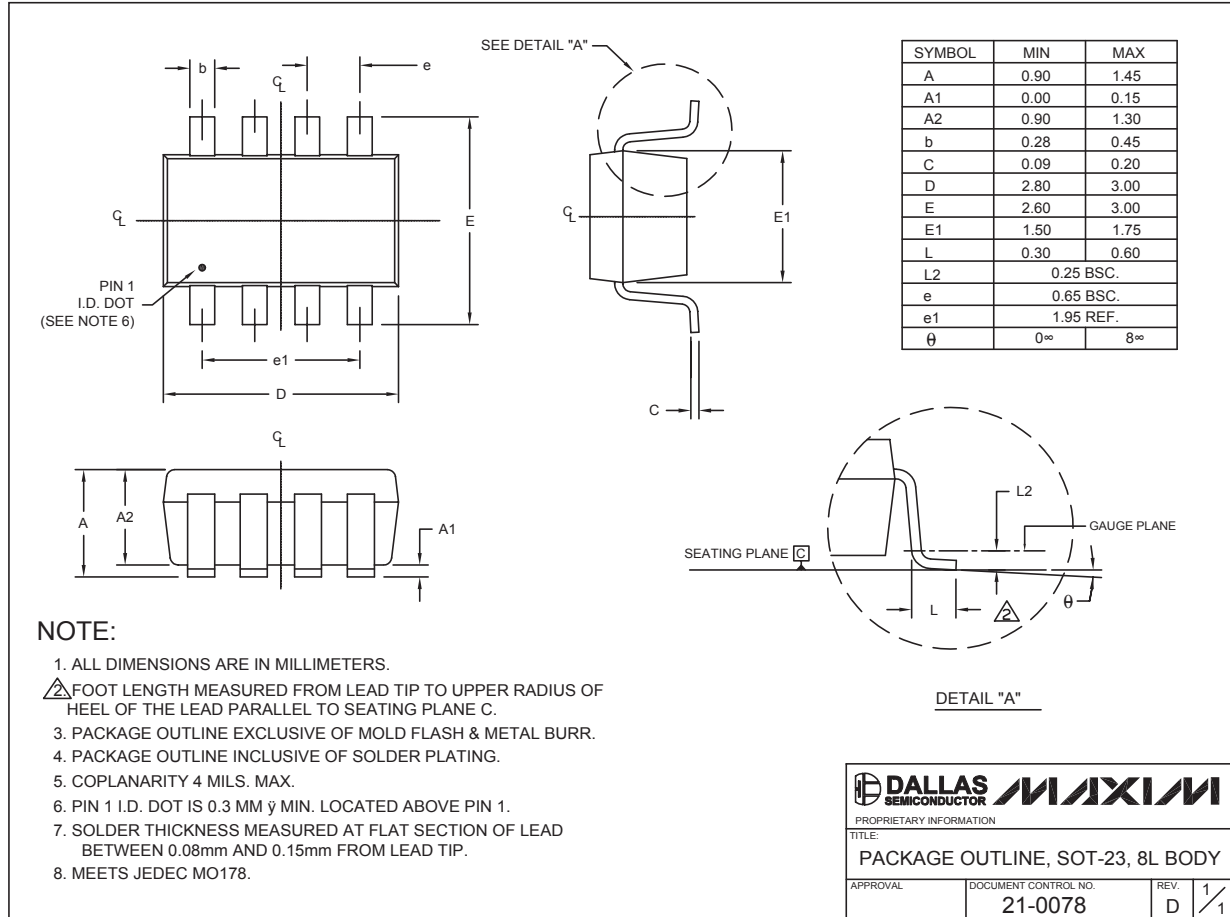
6LSOT1EPS

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Package Information (continued)

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MAX6715-MAX6729



DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SOT-23, 8L BODY

| | | | |
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