1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

ON1, $\overline{ON2}$, OUT, POUT to GND .....-0.3V, +6V
PGND to GND .....-0.3V, +0.3V
LX to PGND .....-0.3V, (V_{POUT} + 0.3V)
CLK/SEL, DATA, POKIN, REF,
AINSEL, AIN1, AIN2, FB, POK to GND .....-0.3V, (V_{OUT} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow SO (derate 8.7mW/°C above +70°C) 696mW

Operating Temperature Range
MAX848ESE/MAX849ESE .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{OUT} = 3.6V, GND = PGND = CLK/SEL = ON1 = $\overline{ON2}$ = AINSEL = AIN1 = AIN2 = FB = POKIN, POUT = OUT, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Minimum Operating Voltage (Note 1)					0.7		V
REFERENCE							
Reference Output Voltage	I_{REF} = 0mA			1.23	1.25	1.27	V
REF Load Regulation	-1µA < I_{REF} < 50µA				5	15	mV
REF Supply Rejection	2.5V < V_{OUT} < 5V				0.2	5	mV
DC-DC CONVERTER							
Output Voltage (Note 2)	V_{FB} < 0.1V, CLK/SEL = OUT			3.17	3.34	3.40	V
Output Current	V_{IN} = 1.2V	V_{OUT} = 3.3V	MAX848		110		mA
			MAX849		300		
		V_{OUT} = 5V	MAX848		70		
			MAX849		200		
	V_{IN} = 2.4V	V_{OUT} = 3.3V	MAX848		200		
			MAX849		750		
		V_{OUT} = 5V	MAX848		130		
			MAX849		500		
	V_{IN} = 2.7V	V_{OUT} = 3.3V	MAX848		250		
			MAX849		600		
		V_{OUT} = 5V	MAX848		150		
			MAX849		800		
	V_{OUT} = 5V	MAX848, V_{IN} = 3.3V			300		
		MAX849, V_{IN} = 3.6V			1000		
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT			1.215	1.240	1.265	V
FB Input Current	V_{FB} = 1.25V					200	nA
Output Voltage Adjust Range				2.7		5.5	V
Output Voltage Lockout Range	(Note 3)			2.1		2.4	V
Load Regulation (Note 4)	CLK/SEL = OUT				-1.6		%
Minimum Start-Up Voltage (Note 5)	I_{LOAD} < 1mA, T_A > +25°C				0.9	1.1	V
Frequency in Start-Up Mode	V_{OUT} = 1.5V			40		300	kHz
Operating Current in Shutdown	Current into OUT pin, $V_{\overline{ON2}}$ = 3.6V				4	20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{OUT} = 3.6V, GND = PGND = CLK/SEL = ON1 = $\overline{ON2}$ = AINSEL = AIN1 = AIN2 = FB = POKIN, POUT = OUT, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Current in Low-Power Mode (Note 6)	Current into OUT pin, CLK/SEL = GND			35	90	µA
Operating Current in Low-Noise Mode (Note 6)	Current into OUT pin, CLK/SEL = OUT, does not include switching losses			150	300	µA
DC-DC SWITCHES						
POUT Leakage Current	V_{LX} = 0V, $V_{\overline{ON2}}$ = V_{OUT} = 5.5V			0.1	20	µA
LX Leakage Current	V_{LX} = $V_{\overline{ON2}}$ = V_{OUT} = 5.5V			0.1	20	µA
Switch On-Resistance	N-channel	CLK/SEL = GND		0.3	0.6	Ω
		CLK/SEL = OUT		0.13	0.25	
	P-channel	CLK/SEL = OUT		0.25	0.5	
N-Channel Current Limit	CLK/SEL = OUT	MAX848	600	800	1000	mA
		MAX849	1100	1350	1600	
	$V_{CLK/SEL}$ = 0V (Note 7)	MAX848	120	200	300	
		MAX849	250	400	550	
ADC						
Data Output Voltage Low	I_{SINK} = 1mA				0.4	V
Data Output Voltage High	I_{SOURCE} = 1mA		V_{OUT} - 0.4			V
AIN1 Input Voltage Range	AINSEL = GND		0.625		1.875	V
AIN2 Input Voltage Range	AINSEL = OUT		0		2.5	V
AIN1, AIN2 Input Current	f_{CLK} = 400kHz, V_{AIN1} = V_{AIN2} = 2.5V			1	2	µA
Accuracy	f_{CLK} = 400kHz, 5ms conversion, monotonic to 8 bits				±4	% FSR
POWER-GOOD						
Internal Trip Level	Rising V_{OUT}, V_{POKIN} < 0.1V		2.95		3.10	V
External Trip Level	Rising V_{POKIN}		1.225		1.275	V
POK Low Voltage	I_{SINK} = 1mA, V_{OUT} = 3.6V or I_{SINK} = 20µA, V_{OUT} = 1V				0.4	V
POK High Leakage Current	V_{OUT} = V_{POK} = 5.5V			0.01	1	µA
POKIN Leakage Current	V_{POKIN} = 1.5V				50	nA
LOGIC AND CONTROL INPUTS						
Input Low Voltage	1.2V < V_{OUT} < 5.5V, ON1 and $\overline{ON2}$ (Note 8)				0.2V_{OUT}	V
	V_{OUT} = 2.7V, AINSEL and CLK/SEL				0.2V_{OUT}	
Input High Voltage	1.2V < V_{OUT} < 5.5V, ON1 and $\overline{ON2}$ (Note 8)		0.8V_{OUT}			V
	V_{OUT} = 5.5V, AINSEL and CLK/SEL		0.8V_{OUT}			
Logic Input Current	ON1, $\overline{ON2}$, AINSEL and CLK/SEL				1	µA
Internal Oscillator Frequency	CLK/SEL = OUT		260	300	340	kHz
Oscillator Maximum Duty Cycle			80	85	90	%
External Clock Frequency Range			200		400	kHz
CLK/SEL Pulse Width	Not tested		200			ns
CLK/SEL Rise/Fall Time	Not tested				100	ns

ELECTRICAL CHARACTERISTICS

(V_{OUT} = 3.6V, GND = PGND = CLK/SEL = ON1 = $\overline{ON2}$ = AINSEL = AIN1 = AIN2 = FB = POKIN, POUT = OUT, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 9)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE						
Reference Output Voltage	I_{REF} = 0mA		1.225		1.275	V
DC-DC CONVERTER						
Output Voltage (Note 3)	V_{FB} < 0.1V, CLK/SEL = OUT, includes load-regulation error		3.13		3.47	V
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT		1.21		1.27	V
Output Voltage Lockout Range	(Note 3)		2.05		2.45	V
OUT Supply Current in Shutdown	$V_{\overline{ON2}}$ = 3.6V				20	µA
OUT Supply Current in Low-Power Mode (Note 6)	CLK/SEL = GND				90	µA
OUT Supply Current in Low-Noise Mode (Note 6)	CLK/SEL = OUT, does not include switching losses				300	µA
DC-DC SWITCHES						
Switch On-Resistance	N-channel	CLK/SEL = GND			0.6	Ω
		CLK/SEL = OUT			0.25	
	P-channel	CLK/SEL = OUT			0.5	
N-Channel Current Limit	CLK/SEL = OUT	MAX848	600		1100	mA
		MAX849	1100		1800	
	CLK/SEL = GND (Note 7)	MAX848	120		300	
		MAX849	250		550	
ADC						
Accuracy	f_{CLK} = 400kHz, 5ms conversion				±4	% FSR
POWER-GOOD						
Internal Trip Level	Rising V_{OUT}, V_{POKIN} < 0.1V		2.95		3.10	V
External Trip Level	Rising V_{POKIN}		1.225		1.275	V
LOGIC CONTROL INPUTS						
Internal Oscillator Frequency	CLK/SEL = OUT		260		340	kHz
Oscillator Maximum Duty Cycle			80		90	%

Note 1: Minimum operating voltage. Because the MAX848/MAX849 are bootstrapped to the output, it will operate down to a 0.7V input.

Note 2: In low-power mode (CLK/SEL = GND), the output voltage regulates 1% higher than in low-noise mode (CLK/SEL = OUT or synchronized).

Note 3: The part is in start-up mode until it reaches this voltage level. Do not apply full-load current.

Note 4: Load regulation is measured from no load to full load, where full load is determined by the N-channel switch current limit.

Note 5: Start-up is tested with Figure 2's circuit. Output current is measured when the input and output voltages are applied.

Note 6: Supply current from the 3.34V output is measured between the 3.34V output and the OUT pin. This current correlates directly with actual battery supply current, but is reduced in value according to the step-up ratio and efficiency. V_{OUT} = 3.6V to keep the internal switch open when measuring the current into the device.

Note 7: When $V_{CLK/SEL}$ = 0V, the inductor is forced into constant-peak-current, discontinuous operation. This is guaranteed by testing in Figure 2's circuit.

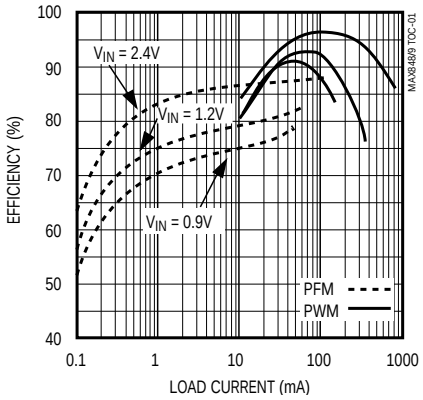
Note 8: ON1 and $\overline{ON2}$ inputs have approximately 0.15V_{OUT} hysteresis.

Note 9: Specifications to -40°C are guaranteed by design, not production tested.

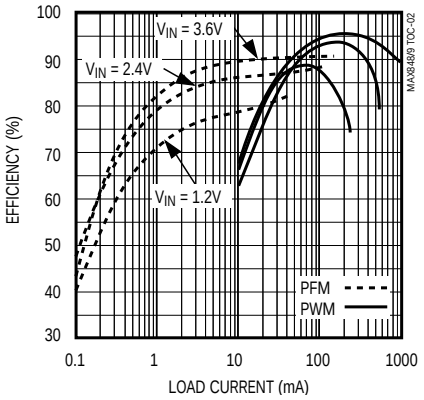
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

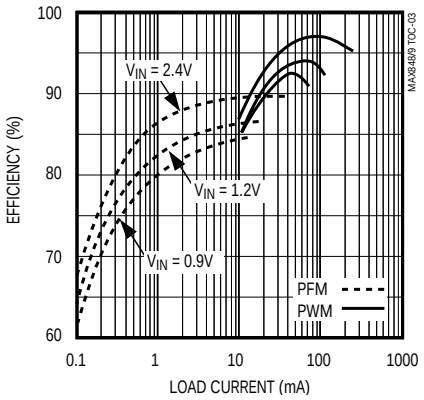
MAX849
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V)



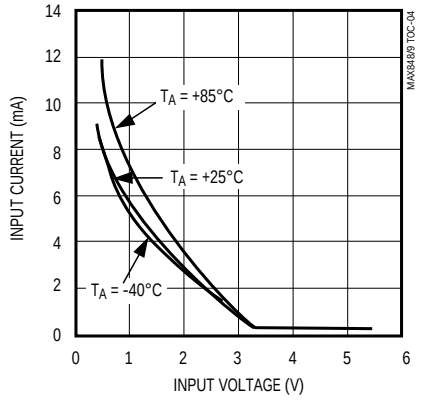
MAX849
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 5V)



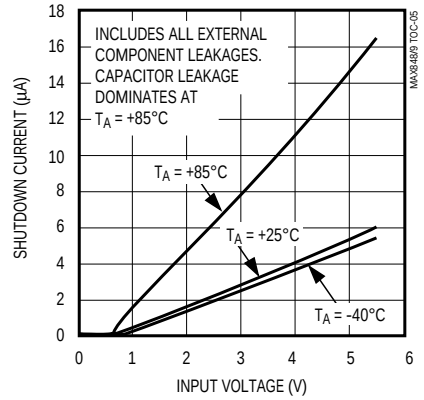
MAX848
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V)



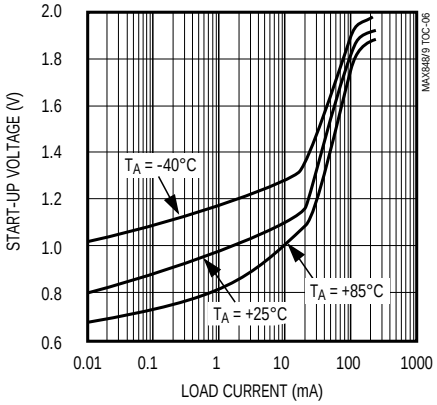
NO-LOAD BATTERY CURRENT
vs. INPUT VOLTAGE



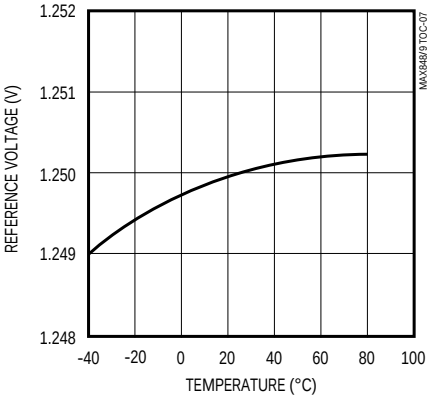
SHUTDOWN CURRENT
vs. INPUT VOLTAGE



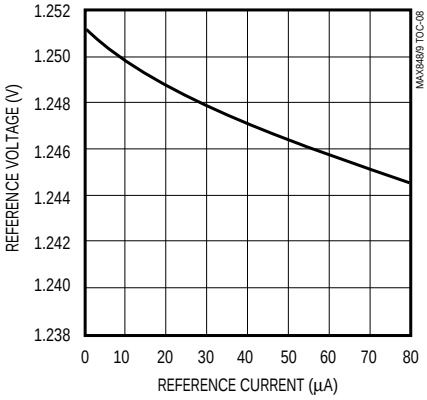
START-UP VOLTAGE vs. LOAD CURRENT
(V_{OUT} = 3.3V, PWM MODE)



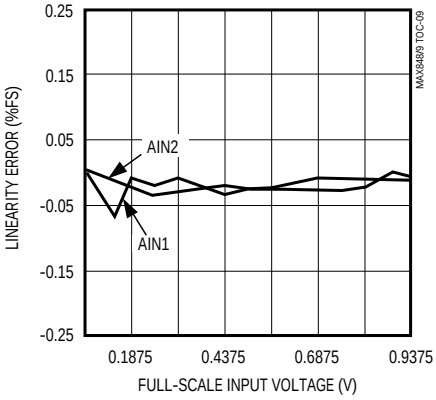
REFERENCE VOLTAGE
vs. TEMPERATURE



REFERENCE VOLTAGE
vs. REFERENCE CURRENT



ADC LINEARITY ERROR
vs. FULL-SCALE INPUT VOLTAGE

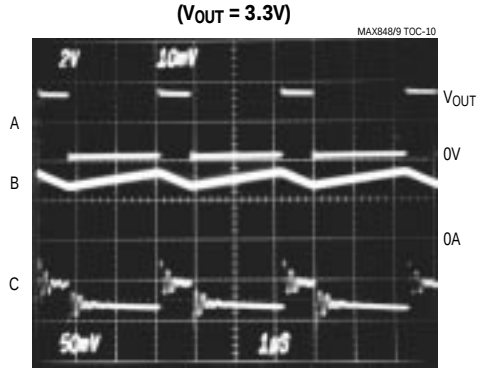


1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

HEAVY-LOAD SWITCHING WAVEFORMS (V_{OUT} = 3.3V)



1µs/div

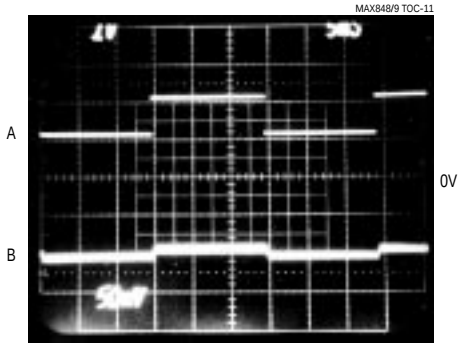
V_{IN} = 1.1V, I_{OUT} = 200mA, V_{OUT} = 3.3V

A = LX VOLTAGE, 2V/div

B = INDUCTOR CURRENT, 0.5A/div

C = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

LINE-TRANSIENT RESPONSE



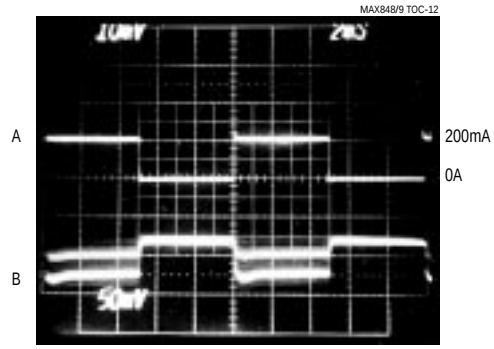
5ms/div

I_{OUT} = 0mA, V_{OUT} = 3.3V

A = V_{IN}, 1.1V TO 2.1V, 1V/div

B = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

LOAD-TRANSIENT RESPONSE



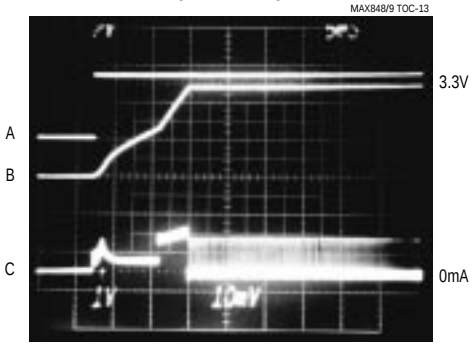
2ms/div

V_{IN} = 1.1V, V_{OUT} = 3.3V

A = LOAD CURRENT, 0mA TO 200mA, 0.2A/div

B = V_{OUT} RIPPLE, 50mV/div, AC COUPLED

POWER-ON DELAY (PFM MODE)



5ms/div

A = V_{ON1}, 2V/div

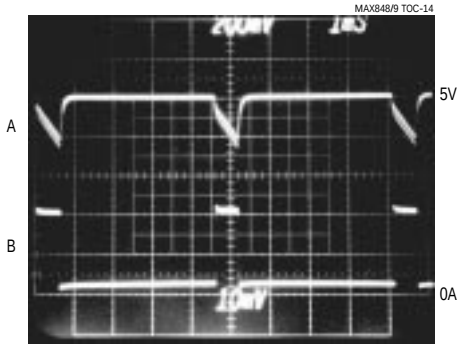
B = V_{OUT}, 1V/div

C = INPUT CURRENT, 0.2A/div

Typical Operating Characteristics (continued)

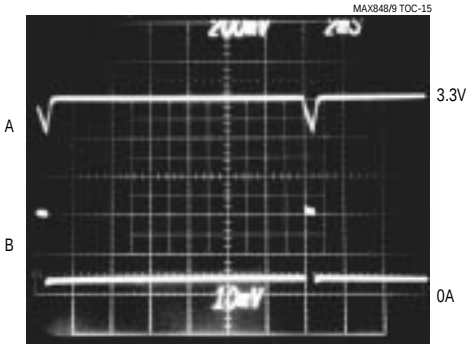
(T_A = +25°C, unless otherwise noted.)

MAX849
GSM LOAD-TRANSIENT RESPONSE



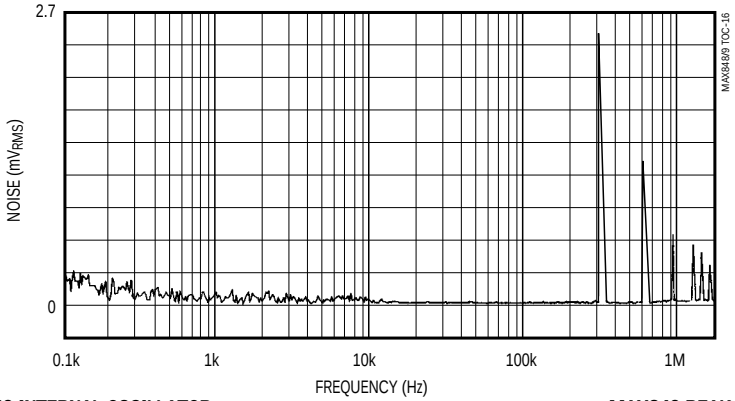
V_{IN} = 3.6V, V_{OUT} = 5V, C_{OUT} = 440µF
A = V_{OUT} RIPPLE, 200mV/div, AC COUPLED
B = LOAD CURRENT, 100mA TO 1A, 0.5A/div,
PULSE WIDTH = 577µs

MAX849
DECT LOAD-TRANSIENT RESPONSE

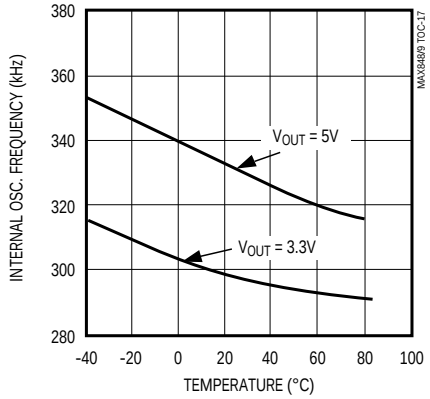


V_{IN} = 1.2V, V_{OUT} = 3.3V, C_{OUT} = 440µF
A = V_{OUT} RIPPLE, 200mV/div, AC COUPLED
B = LOAD CURRENT, 50mA TO 400mA, 0.2A/div,
PULSE WIDTH = 416µs

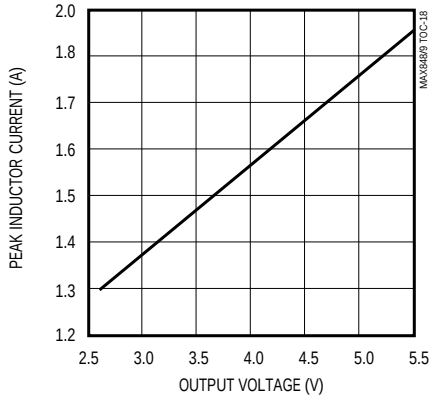
MAX849 NOISE SPECTRUM
(V_{OUT} = 3.3V, V_{IN} = 1.2V, R_{LOAD} = 50Ω)



MAX849 INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



MAX849 PEAK INDUCTOR CURRENT vs. OUTPUT VOLTAGE



1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

Pin Description

PIN	NAME	FUNCTION
1	AIN1	ADC's Channel 1 Input. Analog input voltage range is 0.625V to 1.875V.
2	AIN2	ADC's Channel 2 Input. Analog input voltage range is 0V to 2.5V.
3	REF	Reference Output. Bypass with a 0.22µF capacitor to GND.
4	GND	Ground. Use for low-current ground paths. Connect to PGND with a short trace.
5	OUT	Output Sense Input. The IC is powered from OUT. Bypass to GND with a 0.1µF ceramic capacitor. Connect OUT to POUT through a 10Ω series resistor.
6	POKIN	Power-Good Comparator Input. Connect to GND for fixed threshold (V_{OUT} x 0.9). To adjust the threshold, connect to a resistor divider from OUT to GND.
7	FB	Dual Mode DC-DC Converter Feedback Input. Connect to GND for fixed 3.3V output voltage. Connect to a resistor divider from OUT to GND to adjust the output voltage. Minimize noise coupling from switching signals to FB.
8	POK	Power-Good Output. This open-drain output is pulled low when the output voltage (V_{OUT}) drops below the internally set threshold (fixed threshold), or when the voltage at POKIN drops below V_{REF} (adjustable threshold).
9	AINSEL	ADC's Input Channel Selector. Pull low to select AIN1 and drive high to select AIN2.
10	DATA	ADC's Serial Output. Pulsed output, RZ format. Full scale is $f_{OSC}/2$ ($f_{CLK}/2$ in external sync mode). The DATA output is low when $V_{CLK/SEL}$ = 0V (PFM mode).
11	CLK/SEL	External Clock Input/Regulator's Switching Mode Selector. CLK/SEL = low: low-power, low-quiescent PFM mode. Delivers 100mW of output power. CLK/SEL = high: low-noise, high-power PWM mode, switching at a constant frequency (300kHz). CLK/SEL = driven with external clock: low-noise, high-power, synchronized PWM mode. The internal oscillator is synchronized to the external clock (200kHz ~ 400kHz). Turning the DC-DC converter on with $V_{CLK/SEL}$ = 0V also serves as a soft-start function, since the peak inductor current is limited to 30% of the nominal value.
12	PGND	Source of the Internal N-Channel Power MOSFET. Connect to high-current ground path.
13	LX	Drain of the Internal N-Channel Power MOSFET and P-Channel Synchronous Rectifier
14	POUT	Source of the Internal P-Channel Synchronous Rectifier MOSFET. Connect an external Schottky diode from LX to POUT. Bypass to PGND with a 0.1µF ceramic capacitor as close to the IC as possible.
15	$\overline{ON2}$	OFF Control Input. When ON1 = 0 and $\overline{ON2}$ = 1, the IC is off.
16	ON1	ON Control Input. When ON1 = 1 or $\overline{ON2}$ = 0, the IC is on.

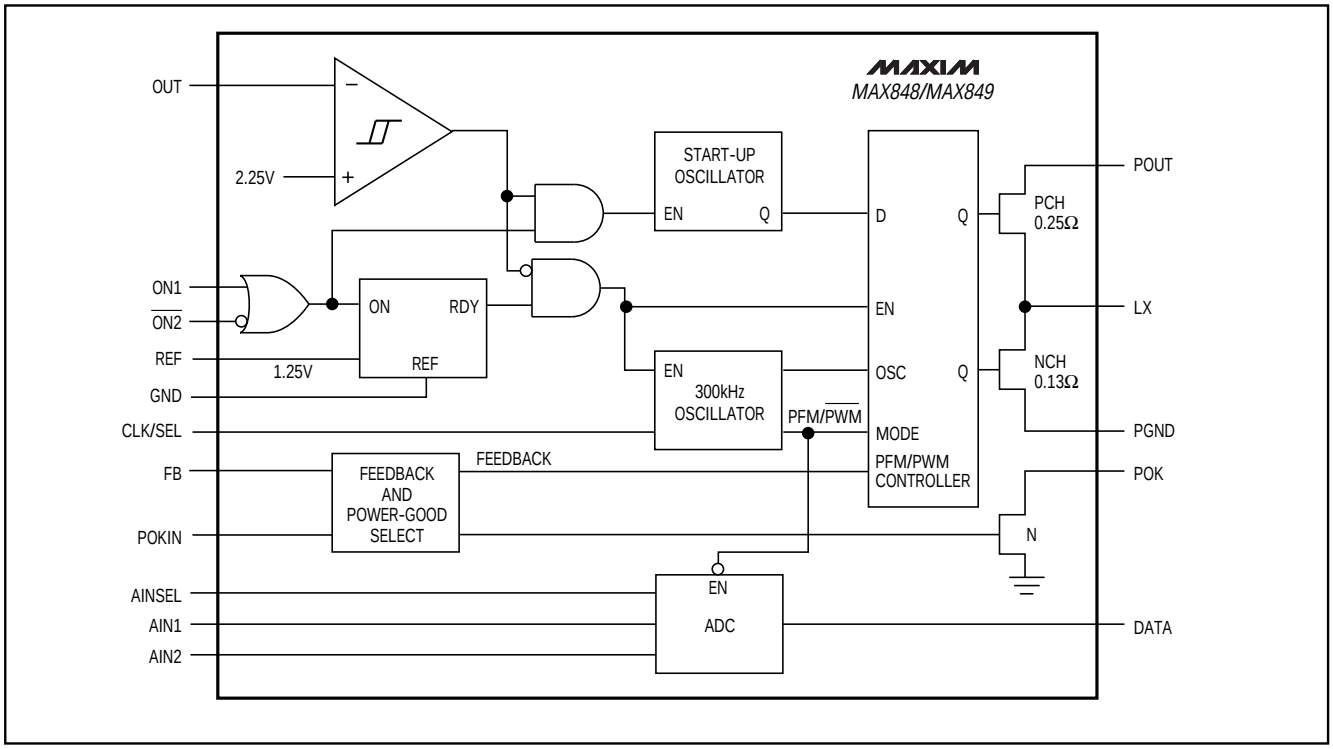


Figure 1. Functional Diagram

Detailed Description

The MAX848/MAX849 combine a switching regulator, N-channel power MOSFET, P-channel synchronous rectifier, precision reference voltage, power-good indicator, and battery voltage monitor, all in a single monolithic device. The MAX848/MAX849 are powered directly from the output. The output voltage is factory preset to 3.3V or adjustable from 2.7V to 5V with external resistors (Dual Mode™ operation). These devices start from a low 1V input voltage and remain operational down to 0.7V. The MAX848/MAX849 operate with either one to three NiCd/NiMH cells or one Li-Ion cell.

At power-up, an internal low-voltage oscillator drives the N-channel power switch, and the output voltage slowly builds up. The oscillator has a 25% nominal duty cycle to prevent current build-up in the inductor. An output voltage in excess of the nominal 2.25V lockout voltage activates the error comparator and internal timing circuitry. The device resumes operation in either pulse-frequency-modulation (PFM) low-power mode or pulse-width-modulation (PWM) low-noise mode, selected by the logic control, CLK/SEL. Figure 2 shows the standard application circuit for the MAX849 configured in the high-power PWM mode.

On/Off Control

The MAX848/MAX849 are turned on or off by logic input pins ON1 and $\overline{ON2}$ (Table 1). When ON1 = 1 or $\overline{ON2}$ = 0, the part is on. When ON1 = 0 and $\overline{ON2}$ = 1, the part is off. Both inputs have logic trip points near 0.5 x V_{OUT} with 0.15 x V_{OUT} hysteresis.

Table 1. On/Off Logic Control

ON1	$\overline{ON2}$	MAX848/MAX849
0	0	On
0	1	Off
1	0	On
1	1	On

Operating Modes

The MAX848/MAX849 operate in either PFM, PWM, or PWM synchronized to an externally applied clock signal. Table 2 lists each operating mode.

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

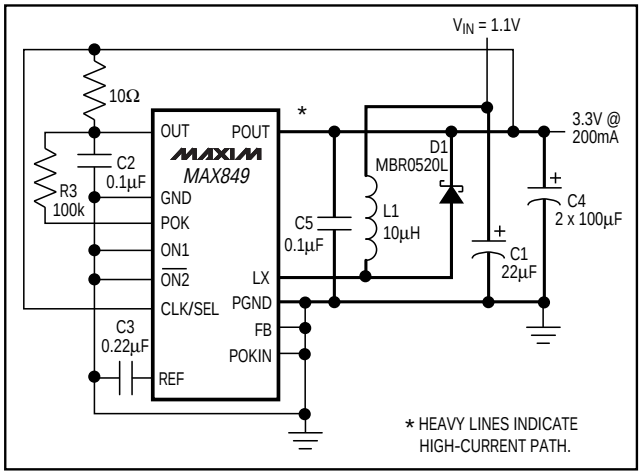


Figure 2. 3.3V Preset Output

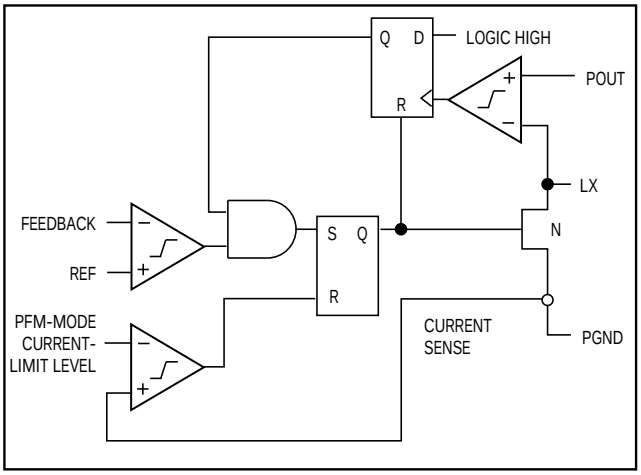


Figure 3. Controller Block Diagram in PFM Mode

Table 2. Selecting Operating Mode

CLK/SEL	MODE
0	PFM
1	PWM
External clock (200kHz ~ 400kHz)	Synchronized PWM

Low-Power PFM Mode

When CLK/SEL is pulled low, the MAX848/MAX849 operate in low-power, low-supply-current PFM mode. Pulse-frequency modulation provides the highest efficiency at light loads. The P-channel rectifier is turned off to reduce gate-charge losses, and the regulator operates in discontinuous mode. The N-channel power MOSFET is kept on until the inductor current ramps to 30% of the current limit. The inductor energy is delivered to the output capacitor when the switch turns off. A new cycle is inhibited until the inductor current crosses zero. Zero current detection is accomplished by sensing the LX voltage crossing the output voltage. Figure 3 shows the block diagram for the PFM controller.

Low-Noise PWM Mode

When CLK/SEL is pulled high, the MAX848/MAX849 operate in high-power, low-noise, current-mode PWM, switching at the 300kHz nominal internal oscillator frequency. The internal rectifier is active in this mode, and the regulator operates in continuous mode. The N-channel power MOSFET turns on until either the output voltage is in regulation or the inductor current limit is reached (0.8A for the MAX848 and 1.4A for the MAX849). The switch turns off for the remainder of the cycle and the inductor energy is delivered to the output capacitor. A new cycle is initiated on the next oscillator cycle. In low-noise applications, the fundamental and the harmonics generated by the fixed switching frequency can easily be filtered. Figure 4 shows the block diagram for the PWM controller.

The MAX848/MAX849 enter synchronized current-mode PWM when a clock signal (200kHz < f_{CLK} < 400kHz) is applied to CLK/SEL. The internal synchronous rectifier is active and the switching frequency is synchronized to the externally applied clock signal. For wireless applications, this ensures that the harmonics of the switching frequencies are predictable and can be kept outside the IF band(s). High-frequency operation permits low-magnitude output ripple voltage.

The MAX848/MAX849 are capable of providing a stable output even with a rapidly pulsing load (GSM, DECT), such as from a transmitter power amplifier in digital cordless phones (see *Typical Operating Characteristics*).

In PWM mode, the use of the synchronous rectifier ensures constant-frequency operation, regardless of the load current.

Setting the Output Voltage Externally

The MAX848/MAX849 feature Dual Mode operation. The output voltage is preset to 3.3V (FB = 0V), or it can be adjusted from 2.7V to 5.5V with external resistors R1, R2, and R3, as shown in Figure 5. To set the output voltage externally, select resistor R3 in the 10kΩ to 100kΩ range. The values for R1 and R2 are given by:

$$R2 = R3(V_{OUT} / V_{TRIP} - 1)$$

$$R1 = (R3 + R2)(V_{TRIP} / V_{REF} - 1)$$

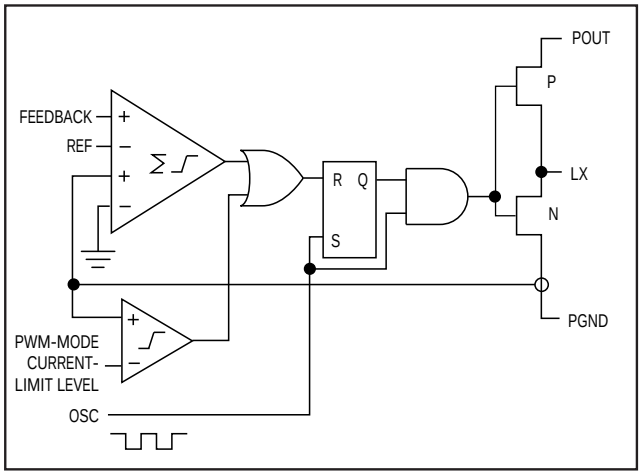


Figure 4. Controller Block Diagram in PWM Mode

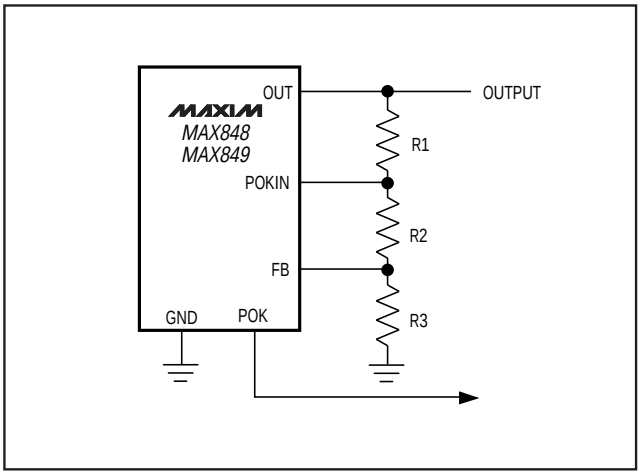


Figure 5. Adjustable Output Voltage and Power-Good Trip Level

where V_{REF} = 1.25V, V_{OUT} is the desired output voltage, and V_{TRIP} is the desired trip level for the power-good comparator.

Power-OK

The MAX848/MAX849 feature a power-good comparator. This comparator's open-drain output, POK, is pulled low when the output voltage falls below the nominal internal threshold level of 3V with POKIN = 0V. To set the power-good trip level externally, refer to the *Setting the Output Voltage Externally* section.

Analog-to-Digital Converter (ADC)

The MAX848/MAX849 have an internal, two-channel, serial ADC. The ADC converts an analog input voltage into a digital stream available at the DATA pin. The converter skips clock pulses in proportion to the input voltage. Output format is a return-to-zero bit stream with a bit duration of $1/f_{CLK}$. At zero-scale input voltage, all pulses are skipped and DATA remains low; with a positive full-scale input voltage, no pulses are skipped; and at mid-scale, every other pulse is skipped. The ADC's clock is one-half of the externally applied clock signal or one-half of the internal 300kHz clock available at LX. In PFM mode, the converter is not active and DATA is driven low.

Channel 1, AIN1, has an input voltage range of 0.625V to 1.875V and is selected when AINSEL is low. Channel 2, AIN2, accepts inputs in the 0V to 2.5V range and is selected when AINSEL is pulled high (Figure 6).

The ADC is a switched-capacitor type; therefore, an anti-aliasing filter might be required at the inputs. Insert a 1kΩ series resistor and a 0.01µF filter capacitor in noisy environments.

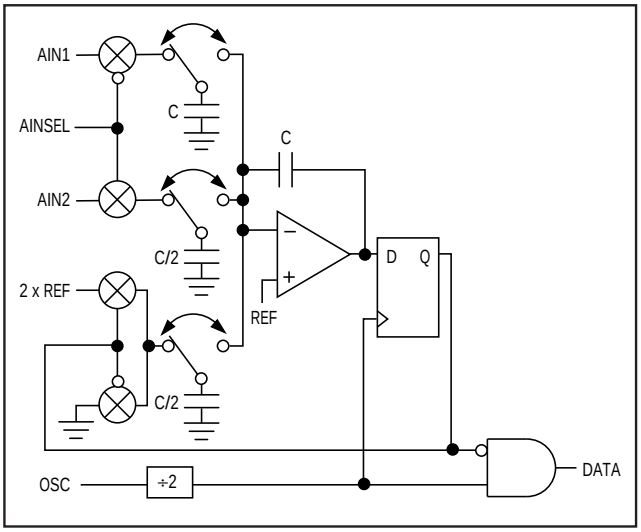


Figure 6. A/D Converter Block Diagram

Timer Function Implementation

Implement the necessary counter functions either with discrete hardware or with microcontroller (µC) implementations. The output resolution depends on how many of the ADC clock pulses are counted, as shown in Figure 7.

Hardware Implementation

A complete hardware solution can be implemented using either two counters or an ASIC. Resolution depends on how many pulses are counted. The main advantage of the discrete hardware implementation is that accuracy is not affected by interrupt latency associated with the µC solution.

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

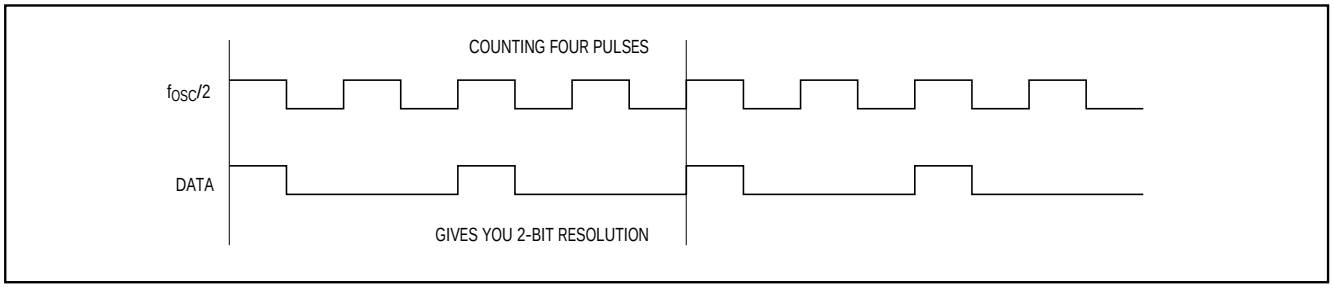


Figure 7. Bit Stream at 1/2 Full Scale

When using two counters of the same length, as shown in Figure 8, one counter (A) just counts the A/D clock pulses ($f_{OSC}/2$), and the other counter (B) counts DATA output pulses. When counter A overflows (for example, after 256 clock cycles for an 8-bit counter), counter B is disabled. The controller reads the counter B output data and calculates the analog voltage present at the ADC's input.

All µC Implementation

This implementation uses a µC timer and a counter. The timer and the counter are reset at the same time. The counter counts data-output pulses applied at its input. When the timer times out, an interrupt is asserted. The µC then reads the state of the counter register. The interrupt-handling overhead can cause the counter to count more pulses than desired. Accuracy depends on how long the µC needs to read the counter. No errors will occur if the counter is disabled within one clock period. Interrupt latency reduces accuracy. The main advantage of this implementation is that no external hardware is required.

Design Procedure

Inductor Selection

The MAX848/MAX849's high switching frequency allows the use of a small inductor. Use a 10µH inductor for the MAX849 and a 22µH inductor for the MAX848. Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. Make sure the inductor's saturation rating (the current at which the core begins to saturate and inductance starts to fall) exceeds the internal current limit: 0.8A for the MAX848 and 1.4A for the MAX849. However, it is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value). For highest efficiency, use a coil with low DC resistance, preferably under 100mΩ. To minimize radiated noise, use a toroid, pot core, or shielded inductor. See Table 5 for a list of suggested inductor suppliers.

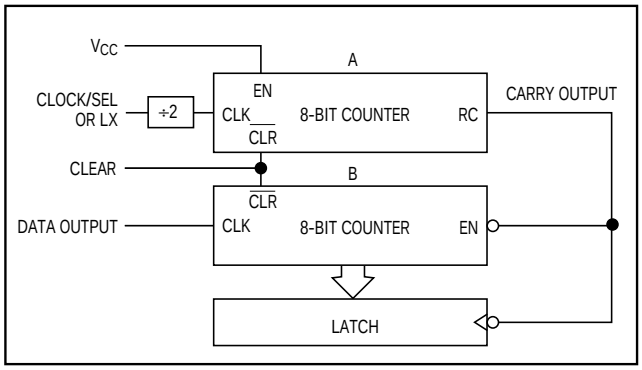


Figure 8. Discrete Hardware Solution for Counting A/D Output Data Pulses

Diode Selection

The MAX848/MAX849's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5817 or MBR0520L, are recommended. Make sure the diode's current rating exceeds the maximum load current and that its breakdown voltage exceeds V_{OUT}.

The Schottky rectifier diode carries load currents only in the PFM operating mode, since the P-channel synchronous rectifier is disabled. Therefore, the current rating need not be high (0.5A is sufficient). In PFM mode, the voltage drop across the rectifier diode causes efficiency loss. However, when operating in PWM mode, the internal P-channel synchronous rectifier is active and efficiency loss due to the rectifier diode is minimized.

For high-temperature applications, Schottky diodes may be inadequate due to their high leakage currents; use high-speed silicon diodes such as the MUR105 or EC11FS1. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantage of high leakage current. See Table 4 for a list of suggested diode suppliers.

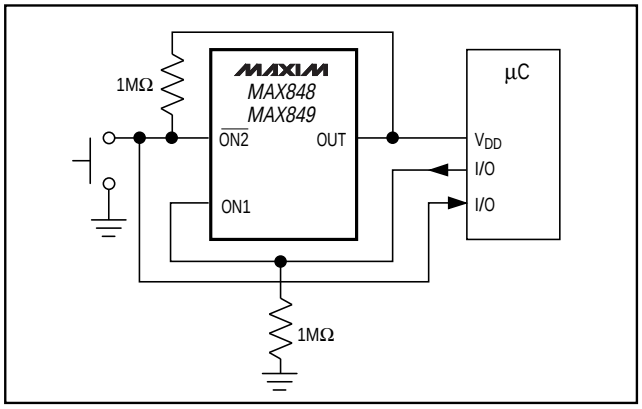


Figure 9. Momentary Pushbutton On/Off Switch

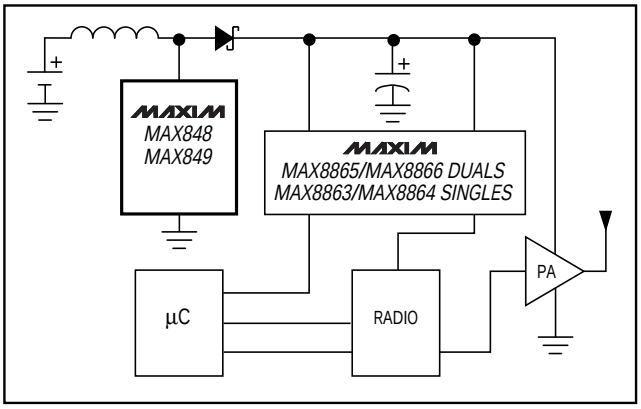


Figure 10. Typical Phone Application

Capacitor Selection

Input Bypass Capacitors

A 22µF, low-ESR input capacitor will reduce peak currents and reflected noise due to inductor current ripple. Smaller ceramic capacitors may also be used for light loads or in applications that can tolerate higher input ripple.

Output Filter Capacitors

Two 100µF (single 100µF for the MAX848), 10V, low-ESR, output filter capacitors typically exhibit 30mV ripple when stepping up from 1.2V to 3.3V at 200mA (100mA for the MAX848). Bypass the MAX848/MAX849 supply input, OUT, with a 0.1µF ceramic capacitor to GND. Also bypass POUT to PGND with a 0.1µF ceramic capacitor.

The filter capacitors' equivalent series resistance (ESR) affects efficiency and output ripple. The output voltage ripple is the product of the peak inductor current and the output capacitor's ESR. Low-ESR, surface-mount tantalum capacitors are currently available from Sprague (595D series) and AVX (TPS series). Sanyo OS-CON organic-semiconductor, through-hole capacitors also exhibit very low ESR, and are especially useful for operation at cold temperatures. See Table 5 for a list of suggested capacitor suppliers.

Applications Information

Using a Momentary On/Off Switch

A momentary pushbutton switch can be used to turn the MAX848/MAX849 on and off.

As shown in Figure 9, ON1 is pulled low and $\overline{ON2}$ is pulled high when the part is off. When the momentary switch is pressed, $\overline{ON2}$ is pulled low and the regulator turns on. The switch should be on long enough for the µC to exit reset. The controller issues a logic high to ON1, which guarantees that the part will stay on, regardless of the switch state.

To turn off the regulator, the switch is pressed and held. The controller reads the switch status and pulls ON1 low. The switch is released and $\overline{ON2}$ is pulled high.

Power Amplifier (PA) and Radio Supply in a Typical Phone Application

The MAX849 is an ideal power supply for the power amplifier (PA) and the radio used in digital cordless and PCS phones (Figure 10). The PA is directly powered by the MAX849 for maximum output swing. Post-linear regulators power the controller and the radio. In addition, they reduce switching noise and ripple. Table 3 lists the output power available when operating with one or more NiCd/NiMH cells or one Li-Ion cell.

Table 3. Available Output Power

NUMBER OF CELLS	INPUT VOLTAGE (V)	OUTPUT VOLTAGE: PA POWER SUPPLY (V)	OUTPUT POWER (W)
1 NiCd/NiMH	1.2	3.3	0.9
2 NiCd/NiMH	2.4	3.3	2.4
2 NiCd/NiMH	2.4	5.0	2.6
3 NiCd/NiMH or 1 Li-Ion	3.6	5.0	4.3

1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converters

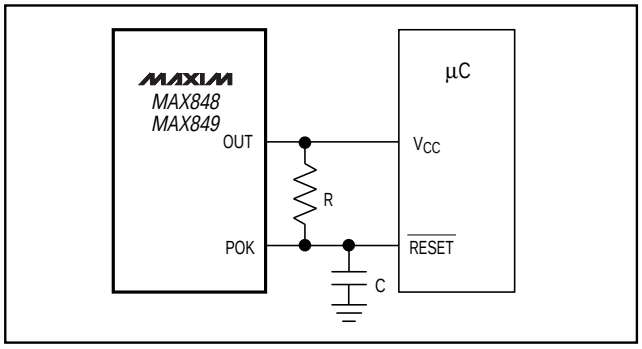


Figure 11. Power-On Reset Delay

Power-On Reset Delay

Adding a timing capacitor from POK to GND generates a power-on reset delay. The reset time constant is determined by the pull-up resistor and timing capacitor (Figure 11). When power is turned on, POK is low and the capacitor is shorted. When the output voltage reaches regulation, POK goes high and the capacitor slowly charges to the output voltage.

The timing resistor value depends on the controller's RESET input leakage current. The voltage drop across the timing resistor should not exceed the difference between the output voltage and the µC reset threshold voltage. This resistor should be large enough to minimize the shutdown current.

µC-Controlled Shutdown

The MAX848/MAX849 turn on when ON1 = 1 or $\overline{ON2}$ = 0. The µC monitors the battery voltage and turns off the device (forces ON1 low and $\overline{ON2}$ high) when the battery is weak.

Layout Considerations

Due to high inductor current levels and fast switching waveforms, which radiate noise, proper PC board layout is essential. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting PGND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Also, minimize lead lengths to reduce stray capacitance and trace resistance.

If an external resistor divider is used to set the output voltage (Figure 5), the trace from FB to the resistors must be extremely short and must be shielded from switching signals, such as CLK, DATA, or LX.

Table 4. Component Selection Guide

PRODUCTION	INDUCTORS	CAPACITORS	DIODES
Surface Mount	Sumida CDR63B, CD73, CDR73B, CD74B series Coilcraft DO1608, DO3308, DT3316 series	Matsuo 267 series Sprague 595D series AVX TPS series	Motorola MBR0520L
Through Hole	Sumida RCH654 series	Sanyo OS-CON series Nichicon PL series	Motorola 1N5817

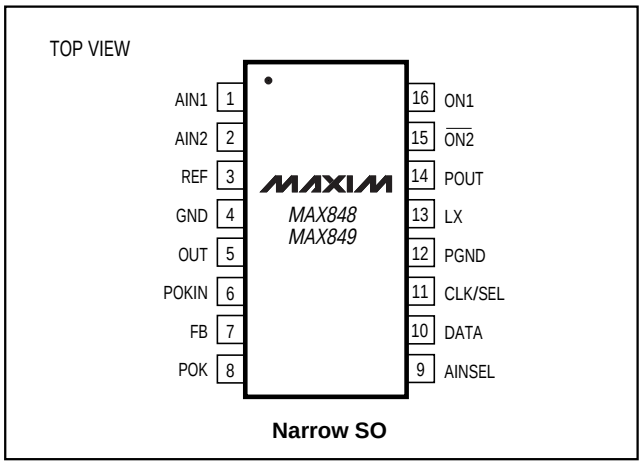
Table 5. Component Suppliers

SUPPLIER	PHONE	FAX
AVX	USA: 803-946-0690 800-282-4975	803-626-3123
Coilcraft	USA: 847-639-6400	847-639-1469
Matsuo	USA: 714-969-2491	714-960-6492
Motorola	USA: 602-303-5454	602-994-6430
Sanyo	USA: 619-661-6835 Japan: 81-7-2070-6306	619-661-1055 81-7-2070-1174
Sumida	USA: 847-956-0666 Japan: 81-3-3607-5111	847-956-0702 81-3-3607-5144

Chip Information

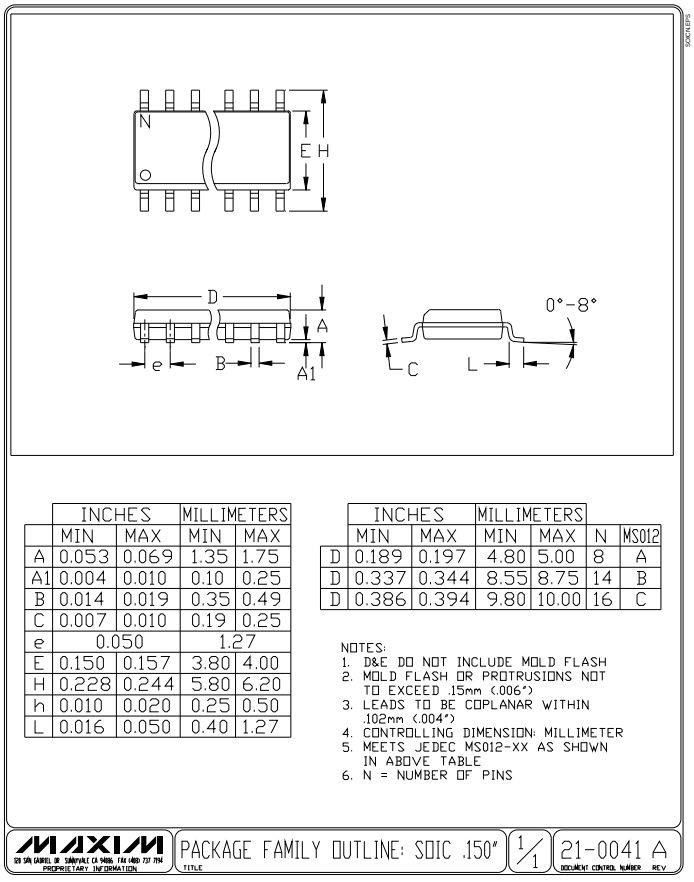
TRANSISTOR COUNT: 2059

Pin Configuration



Narrow SO

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM — PROPRIETARY INFORMATION — PACKAGE FAMILY OUTLINE: SOIC .150" — 1/1 — 21-0041 A

NOTES

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX848ESE+ MAX848ESE+T MAX849ESE+ MAX849ESE+T MAX848ESE MAX848ESE-T MAX849ESE MAX849ESE-T