ABSOLUTE MAXIMUM RATINGS

| IN to GND BAT. CHG. EN/SET. POK. SETI. | 0.3V to +30V |
|---|-------------------|
| | |
| MIN, LDO, TEST to GND | 0.3V to +6V |
| IN to BAT Continuous Current | 1A _{RMS} |
| Continuous Power Dissipation ($T_A = +70^{\circ}C$) | |
| 10-Pin (3mm x 2mm) TDFN | |
| (derate 14.9mW/°C above +70°C) | 1188.7mW |

| Operating Temperature Range | 40°C to +85°C |
|-----------------------------------|----------------|
| Junction Temperature Range | 40°C to +150°C |
| Storage Temperature Range | |
| Lead Temperature (soldering, 10s) | |
| Soldering Temperature (reflow) | |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{IN} = 5V, V_{BAT} = 4V, V_{\overline{EN}/SET} = 0V, T_A = -40^{\circ}C$ to $+85^{\circ}C$, typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | | MIN | ТҮР | MAX | UNITS |
|--|---|--|-------|-------|-------|-------|
| IN | | | | | | |
| Input Voltage Range | | | 0 | | 28 | V |
| Input Voltage Operating Range | (Note 2) | | 4.45 | | 7 | V |
| Input Undervoltage Threshold (UVLO) | V _{IN} rising, 500mV hys | steresis (typ) | 3.80 | 3.90 | 4.00 | V |
| Input Overvoltage Threshold (OVP) | V _{IN} rising, 200mV hys | steresis (typ) | 7.2 | 7.5 | 7.8 | V |
| | I _{BAT} = 0mA, charge r | node | | 700 | 1300 | |
| Input Supply Current | $V_{\overline{EN}/SET} = 5V$, standb | by mode | | 250 | 440 | μA |
| | $V_{IN} = V_{BAT}$, shutdown | n mode | | 200 | | |
| IN-to-BAT On-Resistance | V _{IN} = 4.15V, V _{BAT} = 4 | | 0.35 | | Ω | |
| IN to DAT Comporator Throubold | V _{IN} rising | | 120 | 250 | 500 | |
| IN-to-BAT Comparator Threshold | V _{IN} falling | | | 100 | | mV |
| BAT | 7 | | | | | |
| BAT Regulation Voltage | I _{BAT} = 100mA | $T_A = +25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ | 4.179 | 4.2 | 4.221 | 21 V |
| | | 4.158 | 4.2 | 4.242 | v | |
| Battery Removal Detection | V _{BAT} rising | | | 4.67 | | v |
| Threshold | Hysteresis | | 0.2 | | v | |
| | $\label{eq:BAT} \begin{array}{l} \mbox{Default fast-charge current, V}_{BAT} = 3.5V \\ \hline \hline \hline \hline \hline \hline N/SET = \mbox{one pulse with low } > 4ms, R_{SETI} = 3k\Omega, \\ \mbox{one-pulse mode, V}_{BAT} = 3.5V \end{array}$ | | 365 | 400 | 435 | |
| | | | 460 | 500 | 540 | |
| Charging Current | $\overline{\text{EN}}/\text{SET}$ = two pulses with low > 4ms, V _{BAT} = 3.5V | | 80 | 90 | 100 | mA |
| | $\overline{\text{EN}/\text{SET}}$ = three pulses with low > 4ms, V _{BAT} = 3.5V (Note 3) | | | 2350 | | |
| Soft-Start Time | Ramp time to fast-cha | | 250 | | μs | |
| BAT Precharge Threshold | V _{BAT} rising, 300mV h | ysteresis (typ) | | 2.5 | | V |
| Precharge Current | | | | 80 | | mA |
| BAT Leakage Current | $V_{IN} = 0V, V_{BAT} = 4.2$ | V | | 1 | 5 | μA |

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{IN} = 5V, V_{BAT} = 4V, V_{\overline{EN}/SET} = 0V, T_A = -40^{\circ}C$ to +85°C, typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | | CONDITION | S | MIN | ТҮР | MAX | UNITS |
|-----------------------------------|--|---|---|-----|-------|------|-------|
| LDO | 1 | | | | | | 1 |
| Minimum LDO Bypass Capacitance | | | | | 1 | | μF |
| LDO Regulated Output Voltage | $I_{LDO} = 10 \text{mA}, V_{IN}$ | _DO = 10mA, V _{IN} = 5V | | | 4.94 | | V |
| LDO Output-Current Limit | | | | | 100 | | mA |
| EN/SET | · | | | | | | |
| | Rising | | | | | 1.4 | V |
| Logic Input Thresholds | Falling | | | 0.4 | | | V |
| Program Lock Time | | | | 4 | | | ms |
| Shutdown Delay | $V_{IN} = 5V, \overline{EN}/SET$ | from low to high | | 4 | | | ms |
| tlow | (Note 4) | (Note 4) | | | | 1400 | |
| tнідн | (Note 4) | , | | | | 1400 | μs |
| Pulldown Resistor | | | | | 2 | | MΩ |
| POK, CHG | | | | | | | |
| Logic Output Voltage, Low | $I_{\overline{POK}} = I_{\overline{CHG}} = 5m$ | POK, = ICHG = 5mA | | | 0.05 | 0.2 | V |
| Logio Output Current High | | $V_{\overline{POK}} = V_{\overline{CHG}} = 5.5V, V_{IN} = 0V$ | | | 0.001 | 1 | |
| Logic Output Current, High | VPOK = VCHG = 5. | | | | 0.01 | | μA |
| CHG | | | | | | | |
| | | Default top-off (typ) = 80mA | threshold, hysteresis | 60 | 80 | 100 | |
| Top-Off Threshold | IBAT falling, battery is charged | $\overline{\text{EN}}/\text{SET} = \text{one}$ 1.875k Ω , hyste | pulse, R _{MIN} = eresis (typ) = 130mA | 60 | 80 | 100 | mA |
| | charged | $\overline{EN}/SET = two$ (typ) = 22mA | pulses, hysteresis | 50 | 60 | 70 | |
| Detection Delay | IBAT falls below to | IBAT falls below top-off threshold | | 2 | 4 | 6 | ms |
| THERMAL LOOP | | | | | | | |
| Thermal-Limit Temperature | Junction temperation reduced, TJ rising | Junction temperature when the charge current is reduced, T_J rising | | | +105 | | °C |
| Thermal-Limit Gain | Reduction of IBAT | for increase of T, | j, default mode | | -28 | | mA/°C |

Note 1: Limits are 100% production tested at $T_A = +25$ °C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 2: Guaranteed by undervoltage- and overvoltage-threshold testing. If $V_{BAT} = 4.2V$, V_{IN} needs to be > 4.2V + 250mV (typ) to start normal operation. After the MAX8922L turns on, it can operate until V_{BAT} + 100mV (typ). For complete charging, the input voltage must be > 4.45V. See the *Input Sources* section.

Note 3: Used for factory GSM RF calibration. 217Hz, 12.5% current pulse, T_A = +25°C. Not for continuous charge current.

Note 4: Not tested. Design guidance only.

SUPPLY CURRENT vs. **DISABLED SUPPLY CURRENT vs. CHARGE CURRENT vs. SUPPLY VOLTAGE BATTERY VOLTAGE** SUPPLY VOLTAGE 1.0 1.0 600 500mA SETI MODE 0.9 0.9 500 (mA) 400mA PRESET = 0.8 0.8 STANDBY SUPPLY CURRENT SUPPLY CURRENT (mA) CHARGE CURRENT (mA) 0.7 0.7 400 0.6 0.6 0.5 300 0.5 0.4 0.4 200 0.3 0.3 90mA PRESET 0.2 0.2 100 0.1 0.1 0 0 0 0 1 2 4 5 6 7 0 1 2 3 4 5 6 7 3 0 2 3 4 5 1 BATTERY VOLTAGE (V) SUPPLY VOLTAGE (V) SUPPLY VOLTAGE (V) **CHARGE CURRENT vs. CHARGE CURRENT WITH ONE CHARGE CURRENT WITH TWO** SUPPLY VOLTAGE **EN/SET PULSE EN/SET PULSES** 500 400mA DEFAULT 450 $V_{BAT} = 4V$ 5V/div 5V/div 400 0 VEN/SET 0 VFN/SFT CHARGE CURRENT (mA) 350 500mA 300 250 400mA 400mA 200 150 100 100mA/div 100mA/div 50 IBAT 0 IBAT 0 0 1ms/div 3 9 12 15 18 21 6 24 27 30 0 1ms/div SUPPLY VOLTAGE (V) **CHARGE CURRENT** vs. **GSM TRANSIENT RESPONSE INPUT VOLTAGE HEADROOM** 800 NO BATTERY C_{BAT} = 68µF 700 200mv/div VBAT 600 CHARGE CURRENT (mA) AC-COUPLED 500 400 300 1A/div IBAT 200 100 $I_{FAST-CHARGE} = 677 mA$ 0A 0 1ms/div 0 50 100 150 200 300 250

Typical Operating Characteristics

V_{IN} - V_{BAT} (mV)

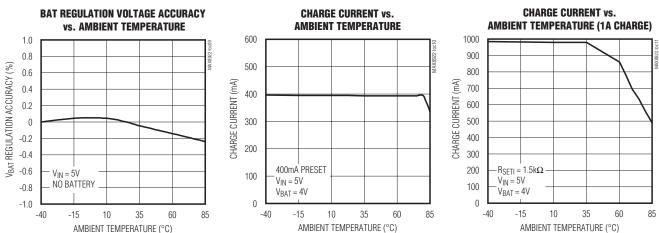
MXXIM

($V_{IN} = 5V$, $V_{\overline{EN}/SET} = 0V$. $V_{BAT} = 4V$, MAX8922L Evaluation Kit. $T_A = +25^{\circ}C$, unless otherwise noted.)

4

Typical Operating Characteristics (continued)

(V_{IN} = 5V, $V_{\overline{EN}/SET}$ = 0V. V_{BAT} = 4V, MAX8922L Evaluation Kit. T_A = +25°C, unless otherwise noted.)



Pin Description

| PIN | NAME | FUNCTION |
|-----|--------|--|
| 1 | IN | DC Input Supply. Connect IN to $V_{IN} > 4V$ and $(V_{IN} - V_{BAT}) \ge 250 \text{mV}$ up to a 7V charging source. Bypass IN to GND with a 1µF or larger ceramic capacitor. |
| 2 | SETI | Charge-Current Program and Fast-Charge Current Monitor. Output current from SETI is 1000µA per ampere of battery-charging current. Set the charging current by connecting a resistor (R _{SETI} in Figure 1) from SETI to GND. IFAST-CHARGE = 1500V/R _{SETI} . Connect to GND if pulse 1 mode (external SETI) is not used. |
| 3 | GND | Ground |
| 4 | LDO | 4.94V Regulated LDO Output with Input Overvoltage Protection. Bypass LDO to GND with a 1µF or larger ceramic capacitor. LDO can be used to supply low-voltage-rated USB systems. |
| 5 | MIN | Top-Off Current Threshold Programmable Input. I _{MIN} = 150V/R _{MIN} . Connect to GND if pulse 1 mode (external SETI) is not used. |
| 6 | ĒN/SET | Active-Low Enable Input. EN/SET is used for programming fast-charge current and GSM test mode. For detailed descriptions, see the <i>Charger-Enable and Program Input (EN/SET)</i> section. |
| 7 | TEST | Factory Test Input. Connect to GND. |
| 8 | CHG | Charging-Status Output. CHG is internally pulled low when the charger is in prequalification or fast- charge mode. CHG is high impedance when the charger is in top-off or disabled. |
| 9 | POK | Input Power-OK Monitor. $\overline{\text{POK}}$ is an open-drain output that is internally pulled low when V _{IN} is greater than V _{UVLO} and lower than V _{OVP} and V _{IN} > V _{BAT} + 250mV. $\overline{\text{POK}}$ is high impedance when V _{IN} is less than V _{UVLO} or greater than V _{OVP} or V _{IN} < V _{BAT} + 100mV. |
| 10 | BAT | Battery Connection. The IC delivers charging current and monitors battery voltage using BAT. Bypass BAT to GND with a 2.2µF or larger ceramic capacitor. BAT is high impedance when the IC is disabled. |
| | EP | Exposed Pad. Connect to the GND plane for increased thermal dissipation. |

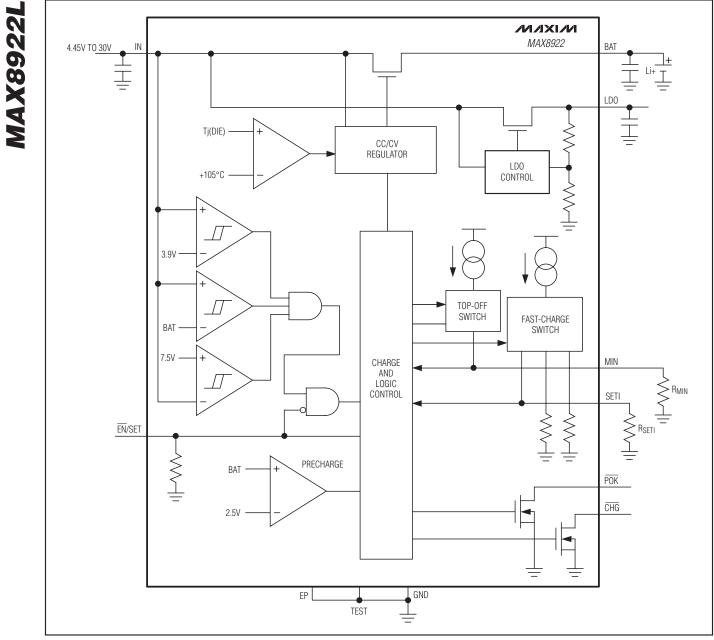


Figure 1. MAX8922L Functional Diagram

Detailed Description

The MAX8922L is designed to charge a single-cell Li+ battery from a DC source voltage between 4.45V and 7V, while V_{IN} can withstand up to 30V. The fast-charge current and top-off current thresholds are programmable with $\overline{\text{EN}}$ /SET, SETI, and MIN.

Charger-Enable and Progra<u>m I</u>nput (EN/SET)

EN/SET is an active-low logic input that enables the charger. Drive EN/SET high longer than 4ms to disable the charger-control circuitry. If EN/SET is left unconnected, an internal $2M\Omega$ pulldown resistor enables 400mA fast-charge current by default. The pulse programming scheme shown in Table 1 and Figure 3 is used to program the charge current and GSM test mode. There are four different fast-charge current states. Default fast-charge current state is 400mA mode. More than three pulses are interpreted to 90mA mode. After programming is locked, the MAX8922L ignores pulses until the IC is disabled/enabled or input power is cycled. Each fast-charge state is locked after a 4ms logic-low is asserted on EN/SET, followed by programming pulses. However, during default mode, if EN/SET does not receive any pulses, the charger stays in default mode unlocked indefinitely.

Debounce Timer

To prevent the MAX8922L from charging the battery momentarily upon IN power-up with EN/SET held low, a 2ms (typ) debounce timer delays the charging loop upon power-up. If EN/SET is logic-low or unconnected (pulled down by an internal pulldown resistor) during IN power-up, the charger starts charging the battery 2ms after VUVLO < V_{IN} < V_{OVP} and V_{BAT} + 250mV < V_{IN} . If EN/SET is logic-high during IN power-up, the charger does not charge the battery.

Soft-Start

To prevent input transients, the rate of change of the charge current is limited when the charger is turned on or changes its current compliance. It takes approximately 250µs (typ) (tSOFTSTART) for the charger to go from 0mA to the maximum fast-charge current.

Thermal-Limit Control

The MAX8922L features a thermal limit that reduces the charge current when the die temperature exceeds $+105^{\circ}$ C. As the temperature increases above $+105^{\circ}$ C, the IC decreases the charge current by 28mA/°C.

Charge-Indicator Output (CHG)

CHG is an open-drain output that indicates charger status. CHG goes low during charging in prequalification or fast-charge mode. The CHG internal open-drain MOSFET turns off when the charge current reaches the top-off threshold. The CHG status is latched after the top-off threshold is reached. The latch can be reset as follows:

- Disable and re-enable the MAX8922L.
- Input power is cycled.
- Battery-charge current increases greater than the top-off threshold + hysteresis.

When the MAX8922L is used in conjunction with a microprocessor, connect a pullup resistor between CHG and the logic I/O voltage to indicate charge status to the μ P. Alternatively, CHG can sink 5mA or more for an LED charge indicator.

| CHARGE CURRENT | DEFAULT | NUMBER OF PULSES + > 4ms LOGIG-LOW | FAST-CHARGE CURRENT SETTING | |
|-------------------------|-----------------------------|---------------------------------------|-----------------------------|--|
| | | One | SETI, resistor programmable | |
| $l_{D,r_{T}}(m\Lambda)$ | I _{BAT} (mA) 400mA | Two | 90mA | |
| IBAT (IIIA) | | Three | 2.3A (GSM test) | |
| | | Four and more | 90mA | |

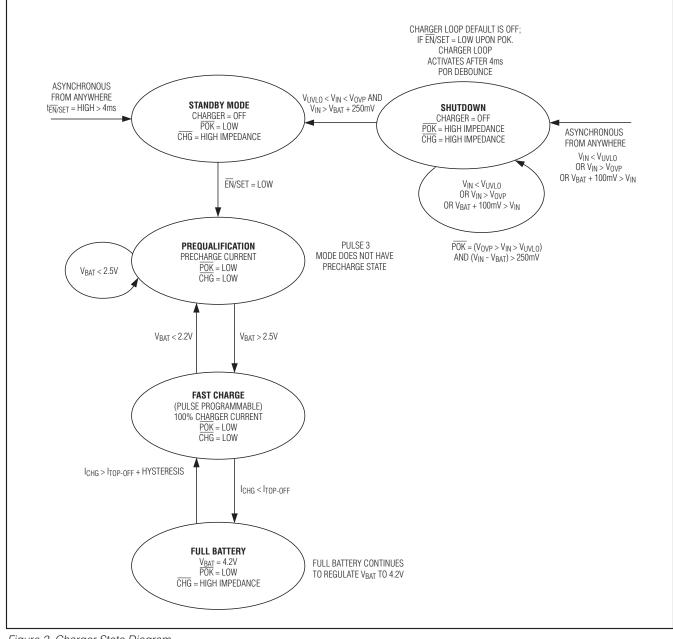


Figure 2. Charger State Diagram

Power-OK Indicator (POK)

The MAX8922L contains an open-drain $\overrightarrow{\text{POK}}$ output that goes low when V_{IN} is greater than V_{UVLO} and lower than V_{OVP} and V_{IN} exceeds the battery voltage by 250mV. Once charging has started, charging is sustained with

inputs as low as 3.5V, as long as the input voltage remains above the battery voltage by at least 100mV. \overrightarrow{POK} status should be maintained even though the charger is disabled by $\overrightarrow{EN}/\overrightarrow{SET}$. When $V_{IN} > V_{OVP}$, \overrightarrow{POK} is high impedance.



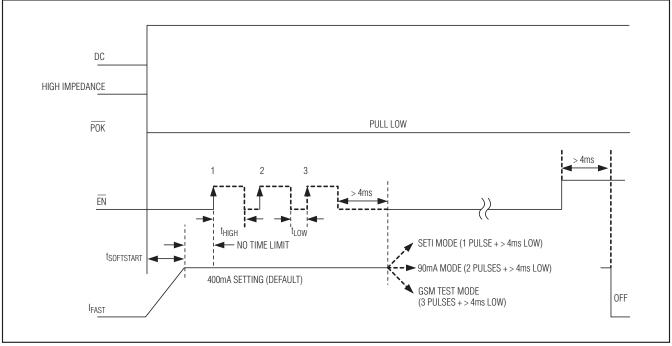


Figure 3. Charge-Current Programming

LDO Output

The LDO is preset to an output voltage of 4.94V and a 100mA current limit (typ). The LDO is powered from IN and has input overvoltage protection. The LDO is on if a valid input is present ($V_{UVLO} < V_{IN} < V_{OVP}$).

Bypass LDO to GND with a $1\mu F$ or larger ceramic capacitor. The LDO can be used to supply low-voltage-rated USB systems.

Applications Information

Fast-Charge Current Settings

In pulse 1 mode, the maximum charging current is programmed by an external resistor connected from SETI to GND (RSETI). Calculate RSETI as follows:

R_{SETI} = 1500V/I_{FAST-CHARGE}

where IFAST-CHARGE is in amperes and RSETI is in ohms. SETI can be used to monitor the fast-charge current level in the one-pulse mode (R_{SETI} mode). The output current from SETI is 1000 μ A per ampere of charging current.

The output voltage at SETI is proportional to the charging current (I_{CHARGE}) when SETI mode is used for the fast-charge current:

VSETI = ICHARGE X RSETI/1000

The voltage at ISET is nominally 1.5V at the selected fast-charge current and decreases with charging current as the cell becomes fully charged or as the thermal-regulation circuitry activates.

Top-Off Current Settings

MAX89221

The top-off charging current is programmed by an external resistor connected from MIN to GND (R_{MIN}) in the one-pulse mode (R_{SETI} mode). Calculate R_{MIN} as follows:

RMIN = 150V/IMIN

where I_{MIN} is in amperes and R_{MIN} is in ohms.

Capacitor Selection

Connect a 2.2 μ F ceramic capacitor from BAT to GND for proper stability. Connect a 1 μ F ceramic capacitor from IN to GND. Use a larger input bypass capacitor for high charging currents to reduce supply noise. All capacitors should be X5R dielectric or better. Be aware that some capacitors have large-voltage coefficients, and should be avoided.

/N/IXI/N



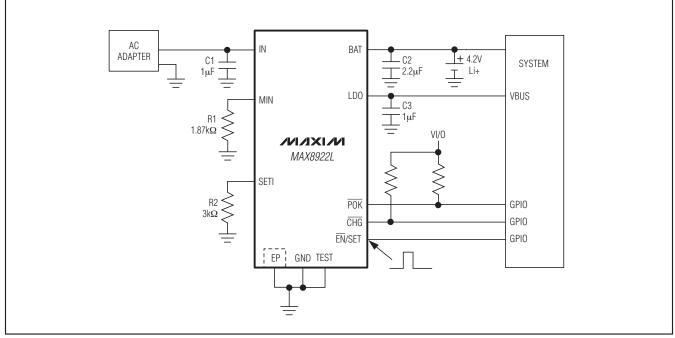


Figure 4. AC Adapter Charger Application

Thermal Considerations

The MAX8922L is in a thermally enhanced TDFN package with an exposed pad. Connect the exposed pad of the package to a large copper ground plane to provide a thermal contact between the device and the circuit board. The exposed pad transfers heat away from the device, allowing the IC to charge the battery with maximum current, while minimizing the increase in die temperature.

Input Sources

The MAX8922L operates from well-regulated DC sources. The charger input voltage range is 4.45V to 7V. The device survives input voltages up to 30V without damage to the IC. If the input voltage is greater than 7.5V (typ), the IC stops charging. An appropriate power supply must provide at least 4.2V plus the voltage drop across the internal-pass transistor when sourcing the desired peak charging current.

VIN(MIN) > 4.2V + IFAST-CHARGE(MAX) X RON

where R_{ON} is the input-to-BAT resistance. Failure to meet this requirement results in an incomplete charge or increased charge time.

Recommended PCB Layout and Routing

Place all bypass capacitors for IN and BAT as close as possible to the IC. Connect the battery to BAT as close as possible to the IC to provide accurate battery voltage sensing. Provide a large copper ground plane to allow the exposed pad to sink heat away from the device. Make all high-current traces short and wide to minimize voltage drops. A sample layout is available in the MAX8922L Evaluation Kit to speed designs.

Typical Application Circuits

AC Adapter Charge

Figure 4 shows the MAX8922L as a Li+ battery charger with an AC adapter. The MAX8922L detects the presence of an input supply resulting in POK pulled low. Once POK is pulled low, the MAX8922L begins charging the battery when EN/SET is low or unconnected. The system can program the charge current by EN/SET pulses. By monitoring CHG, the system can detect the top-off threshold and terminate the charge through EN/SET. The MAX8922L also provides an overvoltage-protected 4.94V LDO output to a low-voltage-rated USB system input.

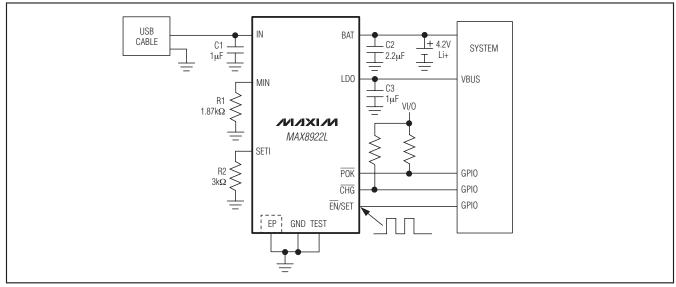


Figure 5. USB-Powered Li+ Battery-Charger Application

USB Charge

The universal serial bus (USB) provides a high-speed serial communications port as well as power for the remote device. The MAX8922L can be configured to charge a single Li+ battery at the highest current possible from the host port. Figure 5 shows the MAX8922L as a USB battery charger. The microprocessor enumerates the host to determine its current capability. The system can program the charge current to 90mA, ISETI, or 400mA by EN/SET pulses if the host port is capable. The MAX8922L also provides an overvoltage-protected 4.94V LDO output to a low-voltage-rated USB system input.

GSM Test Mode

Figure 6 shows the MAX8922L in a GSM test mode. By sending three pulses to EN/SET, the MAX8922L goes into GSM test mode. GSM PA can pull up to 2.3A for 576µs once every 217Hz from the MAX8922L's output. The configuration in Figure 6 is used for system development, testing, and calibrations in the production or design stage.

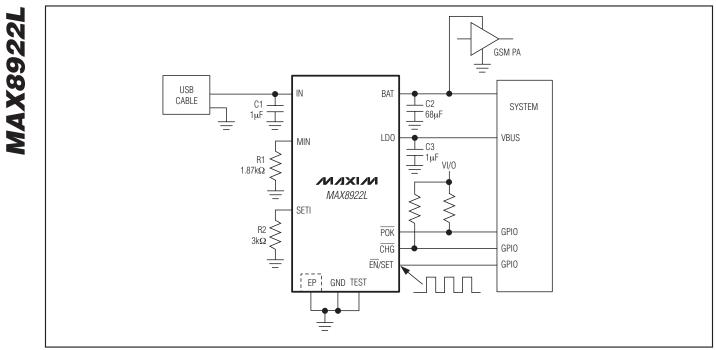


Figure 6. GSM Test Mode

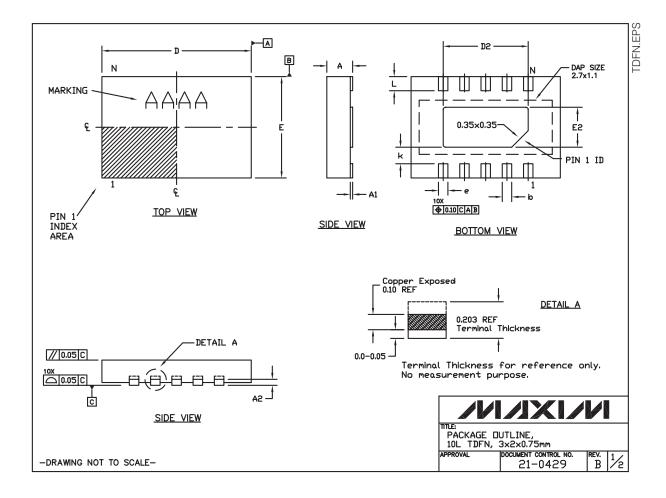
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to <u>www.maxim-ic.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. | |
|--------------|--------------|----------------|--|
| 10 TDFN-EP | T1032N+1 | <u>21-0429</u> | |



Package Information (continued)

For the latest package outline information and land patterns, go to <u>www.maxim-ic.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

NOTES:

- 1. N IS THE TOTAL NUMBER OF LEADS.
- 2. ND AND NE REFER TO THE NUMBER OF TERMINALS OF EACH D AND E SIDE RESPECTIVELY.
- 3. REFER TO JEDEC MO-229(WECD-2) WITH VARIATION OF D2, E2 & L.
- 4. WARPAGE SHALL NOT EXCEED 0.10 mm.
- 5. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
- 6. PKG. LENGTH/PKG. WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC.
- 7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- 8. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- 9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

| COMMON DIMENSIONS | | | | | |
|-------------------|---------------------|--------|----------------|--|--|
| SYMBOL | MIN. | NDM. | MAX. | | |
| Α | 0.70 | 0.75 | 0.80 | | |
| A1 | 0.0 | | 0.05 | | |
| A2 | 0 | 10 REF | . . | | |
| D | 2.90 | 3.00 | 3.10 | | |
| E | 1.90 | 2.00 | 2.10 | | |
| D2 | 1.90 | 2.00 | 2.10 | | |
| E2 | 0.80 | 0.90 | 1.00 | | |
| Ν | | 10 | | | |
| b | 0.25±0.05 | | | | |
| e | 0.50 REF | | | | |
| L | 0.20 0.30 0.40 | | | | |
| PKG. C | PKG. CODE: T1032N-1 | | | | |

| | TTLE: PACKAGE DUTLINE, 10L TDFN, 3×2×0.75mm |
|-------|---|
| CALE- | APPROVAL DOCUMENT CONTROL NO. REV. 21-0429 B 22 |

Revision History

| 1 | REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|--------------------|------------------|--|------------------|
| | 0 | 9/09 | Initial release | — |
| | 1 | 4/10 | Replaced 1-Wire references with single-pin, updated <i>Absolute Maximum Ratings</i> section, and added soldering temperature | 1, 2 |

MAX8922L

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