2

E136 Universal Up/Down Counter Logic Diagram

Note that this diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

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MC10E136 MC100E136

DC CHARACTERISTICS (V$_{EE}$ = V$_{EE}$(min) to V$_{EE}$(max); V$_{CC}$ = V$_{CCO}$ = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input HIGH Current	I$_{IH}$	—	—	150	—	—	150	—	—	150	μA	
Power Supply Current 10E 100E	I$_{EE}$	— —	125 125	150 150	— —	125 125	150 150	— —	125 140	150 170	mA	

AC CHARACTERISTICS (V$_{EE}$ = V$_{EE}$(min) to V$_{EE}$(max); V$_{CC}$ = V$_{CCO}$ = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Maximum Count Frequency	f$_{COUNT}$	550	650	—	550	650	—	550	650	—	MHz	
Propagation Delay to Output CLK to Q MR to Q CLK to $\overline{COUT}$ CLK to $\overline{CLOUT}$	t$_{PLH}$ t$_{PHL}$	850 850 800 825	1150 1150 1150 1150	1450 1450 1300 1400	850 850 800 825	1150 1150 1150 1150	1450 1450 1300 1400	850 850 800 825	1150 1150 1150 1150	1450 1450 1300 1400	ps	
Setup Time S1, S2 D $\overline{CLIN}$ $\overline{CIN}$	t$_S$	1000 800 150 800	650 400 0 400	— — — —	1000 800 150 800	650 400 0 400	— — — —	1000 800 150 800	650 400 0 400	— — — —	ps	
Hold Time S1, S2 D $\overline{CLIN}$ $\overline{CIN}$	t$_h$	150 150 300 150	−200 −250 0 −250	— — — —	150 150 300 150	−200 −250 0 −250	— — — —	150 150 300 150	−200 −250 0 −250	— — — —	ps	
Reset Recovery Time	t$_{RR}$	1000	700	—	1000	700	—	1000	700	—	ps	
Minimum Pulse Width CLK, MR	t$_{PW}$	700	400	—	700	400	—	700	400	—	ps	
Rise/Fall Times $\overline{COUT}$ Other	t$_r$ t$_f$	275 300	— —	600 700	275 300	— —	600 700	275 300	— —	600 700	ps	20% - 80%

2

6367252 0097900 T93

EXPANDED TRUTH TABLE

Function	S1	S2	MR	$\overline{\text{CIN}}$	$\overline{\text{CLIN}}$	CLK	D5	D4	D3	D2	D1	D0	Q5	Q4	Q3	Q2	Q1	Q0	COUT	$\overline{\text{CLOUT}}$
Preset	L	L	L	X	X	Z	L	L	L	L	H	H	L	L	L	L	H	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
.	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Hold	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
Hold	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
	L	H	L	H	H	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Hold	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	H	H	H
Reset	X	X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	H	H

Z = Low to High Transition

2

APPLICATIONS INFORMATION

Overview

The MC10E/100E136 is a 6-bit synchronous, presettable, cascadable universal counter. Using the S1 and S2 control pins the user can select between preset, count up, count down and hold count. The master reset pin will reset the internal counter, and set the $\overline{COUT}$, $\overline{CLOUT}$, and $\overline{CLIN}$ flip-flops. Unlike previous 136 type counters the carry out outputs will go to a high state during the preset operation. In addition since the carry out outputs are registered they will not go low if terminal count is loaded into the register. The look-ahead-carry out output functions similarly.

Note from the schematic the use of the master information from the least significant bits for control of the two carry out functions. This architecture not only reduces the carry out delay, but is essential to incorporate the registered carry out functions. In addition to being faster, because these functions are registered the resulting carry out signals are stable and glitch free.

Cascading Multiple E136 Devices

Many applications require counters significantly larger than the 6 bits available with the E136. For these applications several E136 devices can be cascaded to increase the bit width of the counter to meet the needs of the application.

In the past cascading several 136 type universal counters necessarily impacted the maximum count frequency of the resulting counter chain. This performance impact was the

result of the terminal count signal of the lower order counters having to ripple through the entire counter chain. As a result past counters of this type were not widely used in large bit counter applications.

An alternative counter architecture similar to the E016 binary counter was implemented to alleviate the need to ripple propagate the terminal count signal. Unfortunately these types of counters require external gating for cascading designs of more than two devices. In addition to requiring additional components, these external gates limit the cascaded count frequency to a value less than the free running count frequency of a single counter. Although there is a performance impact with this type of architecture it is minor compared to the impact of the ripple propagate designs. As a result the E016 type counters have been used extensively in applications requiring very high speed, wide bit width synchronous counters.

Motorola has incorporated several improvements to past universal counter designs in the E136 universal counter. These enhancements make the E136 the unparalleled leader in its class. With the addition of look-ahead-carry features on the terminal count signal, very large counter chains can be designed which function at very nearly the same clock frequency as a single free running device. More importantly these counter chains require no external gating. Figure 1 below illustrates the interconnect scheme for using the look-ahead-carry features of the E136 counter.
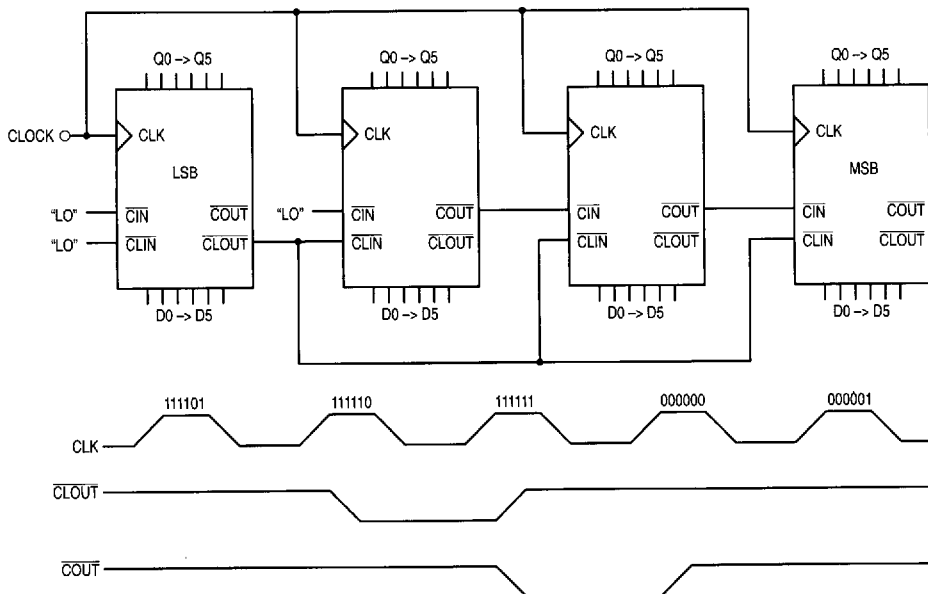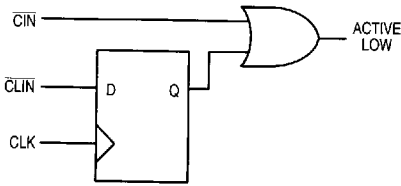

Figure 1. 24-bit Cascaded E136 Counter

Figure 2. Look-Ahead-Carry Input Structure

Note from the waveforms that the look-ahead-carry output ($\overline{\text{CLOUT}}$) pulses low one clock pulse before the counter reaches terminal count. Also note that both $\overline{\text{CLOUT}}$ and the carry out pin ($\overline{\text{COUT}}$) of the device pulse low for only one clock period. The input structure for look-ahead-carry in ($\overline{\text{CLIN}}$) and carry in ($\overline{\text{CIN}}$) is pictured in Figure 2.

The $\overline{\text{CLIN}}$ input is registered and then ORed with the $\overline{\text{CIN}}$ input. From the truth table one can see that both the $\overline{\text{CIN}}$ and the $\overline{\text{CLIN}}$ inputs must be in a LOW state for the E136 to be enabled to count (either count up or count down). The $\overline{\text{CLIN}}$ inputs are driven by the $\overline{\text{CLOUT}}$ output of the lowest order E136 and therefore are only asserted for a single clock period. Since the $\overline{\text{CLIN}}$ input is registered it must be asserted one clock period prior to the $\overline{\text{CIN}}$ input.

If the counter previous to a given counter is at terminal count its $\overline{\text{COUT}}$ output and thus the $\overline{\text{CIN}}$ input of the given counter will be in the "LOW" state. This signals the given counter that it will need to count one upon the next terminal count of the least significant counter (LSC). The $\overline{\text{CLOUT}}$ output of the LSC will pulse low one clock period before it reaches terminal count. This $\overline{\text{CLOUT}}$ signal will be clocked into the $\overline{\text{CLIN}}$ input of the higher order counters on the following positive clock transition. Since both $\overline{\text{CIN}}$ and $\overline{\text{CLIN}}$ are in the LOW state the next clock pulse will cause the least significant counter to roll over and all higher order counters, if signaled by their $\overline{\text{CIN}}$ inputs, to count by one.
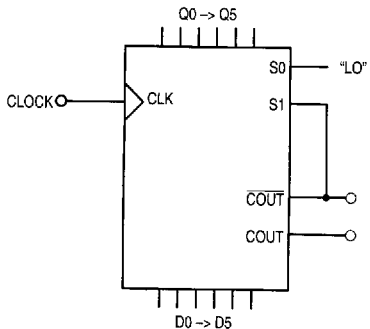
During the clock pulse in which the higher order counter is counting by one the $\overline{\text{CLIN}}$ is clocking in the high signal presented by the $\overline{\text{CLOUT}}$ of the LSC. The $\overline{\text{CIN}}$'s in the higher order counter will ripple propagate through the chain to update the count status for the next occurrence of terminal count on the LSC. This ripple propagation will not affect the count frequency as it has 2^6–1 or 63 clock pulses to ripple through without affecting the count operation of the chain.

The only limiting factor which could reduce the count frequency of the chain as compared to a free running single device will be the setup time of the $\overline{\text{CLIN}}$ input. This limit will consist of the CLK to $\overline{\text{CLOUT}}$ delay of the E136 plus the $\overline{\text{CLIN}}$ setup time plus any path length differences between the $\overline{\text{CLOUT}}$ output and the clock.

Programmable Divider

Using external feedback of the $\overline{\text{COUT}}$ pin, the E136 can be configured as a programmable divider. Figure 3 illustrates the configuration for a 6-bit count down programmable divider. If for some reason a count up divider is preferred the $\overline{\text{COUT}}$ signal is simply fed back to S2 rather than S1. Examination of the truth table for the E136 shows that when both S1 and S2 are LOW the counter will parallel load on the next positive transition of the clock. If the S2 input is low and the S1 input is high the counter will be in the count down mode and will count towards an all zero state upon successive clock pulses. Knowing this and the operation of the $\overline{\text{COUT}}$ output it becomes a trivial matter to build programmable dividers.

For a programmable divider one wants to load a predesignated number into the counter and count to terminal count. Upon terminal count the counter should automatically reload the divide number. With the architecture shown in Figure 3 when the counter reaches terminal count the $\overline{\text{COUT}}$ output and thus the S1 input will go LOW, this combined with the low on S2 will cause the counter to load the inputs present on D0-D5. Upon loading the divide value into the counter $\overline{\text{COUT}}$ will go HIGH as the counter is no longer at terminal count thereby placing the counter back into the count mode.

Figure 3. 6-bit Programmable Divider

Table 1. Preset Inputs Versus Divide Ratio

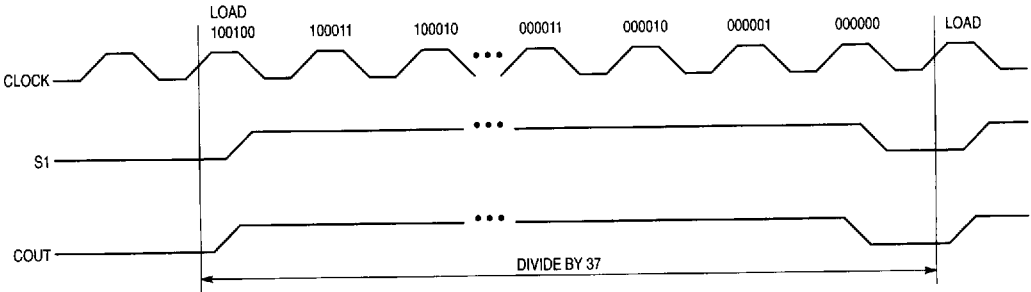| Divide	Preset Data Inputs					
Ratio	D5	D4	D3	D2	D1	D0
2	L	L	L	L	L	H
3	L	L	L	L	H	L
4	L	L	L	L	H	H
5	L	L	L	H	L	L
•	•	•	•	•	•	•
•	•	•	•	•	•	•
36	H	L	L	L	H	H
37	H	L	L	H	L	L
38	H	L	L	H	L	H
•	•	•	•	•	•	•
•	•	•	•	•	•	•
62	H	H	H	H	L	H
63	H	H	H	H	H	L
64	H	H	H	H	H	H

Figure 4. Programmable Divider Waveforms

The exercise of building a programmable divider then becomes simply determining what value to load into the counter to accomplish the desired division. Since the load operation requires a clock pulse, to divide by N, N–1 must be loaded into the counter. A single E136 device is capable of divide ratios of 2 to 64 inclusive, Table 1 outlines the load values for the various divide ratios. Figure 4 presents the waveforms resulting from a divide by 37 operation. Note that the availability of the COUT complimentary output $\overline{COUT}$ allows the user to choose the polarity of the divide by output.

For single device programmable counters the E016 counter is probably a better choice than the E136. The E016 has an internal feedback to control the reloading of the counter, this not only simplifies board design but also will result in a faster maximum count frequency.

For programmable dividers of larger than 8 bits the superiority of the E016 diminishes, and in fact for very wide dividers the E136 will provide the capability of a faster count frequency. This potential is a result of the cascading features mentioned previously in this document. Figure 5 shows the architecture of a 24-bit programmable divider implemented using E136 counters. Note the need for one external gate to control the loading of the entire counter chain. An ideal device for the external gating of this architecture would be the 4-input OR function in the 8-lead SOIC ECLinPS Lite™ family. However the final decision as to what device to use for the external gating requires a balancing of performance needs, cost and available board space. Note that because of the need for external gating the maximum count frequency of a given sized programmable divider will be less than that of a single cascaded counter.
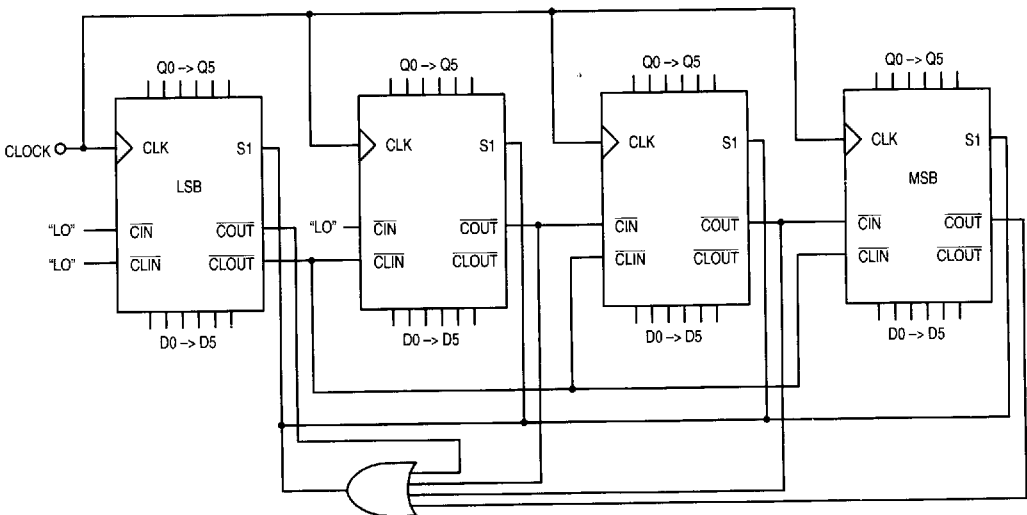

Figure 5. 24-bit Programmable Divider Architecture

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