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REVISION HISTORY

6/08—Rev. 0 to Rev. A

3/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω + 33 µH, ALC = off, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.42		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.72		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.77		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.91		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		2.53		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.27		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.16[1]		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.59		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.11[1]		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.55		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.89[1]		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.94		W
Efficiency	η	P_O = 1.4 W, 8 Ω, V_{DD} = 5.0 V		93		%
Total Harmonic Distortion + Noise	THD + N	P_O = 1 W into 8 Ω, f = 1 kHz, V_{DD} = 5.0 V		0.02		%
		P_O = 0.5 W into 8 Ω, f = 1 kHz, V_{DD} = 3.6 V		0.02		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} – 1.0	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz, output referred		57		dB
Average Switching Frequency	f_{SW}			280		kHz
Differential Output Offset Voltage	V_{OOS}	Gain = 18 dB		2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V, dc input floating	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs ac grounded, C_{IN} = 0.1 µF		60		dB
Supply Current (Typically, 170 µA Increase with ALC On)	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		3.6		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		3.2		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		2.7		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 5.0 V		3.7		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 3.6 V		3.3		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 2.5 V		2.8		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN CONTROL						
Closed-Loop Gain	Gain			18		dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = V_{DD}		10		kΩ
		$\overline{SD}$ = GND		10		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} ≥ 1 mA		1.2		V
Input Voltage Low	V_{IL}	I_{SY} ≤ 300 nA		0.5		V
Wake-Up Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		28		ms
Shutdown Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, inputs are ac grounded, gain = 18 dB, A-weighted		72		µV
Signal-to-Noise Ratio	SNR	P_O = 1.4 W, R_L = 8 Ω		93		dB

[1] Although the SSM2317 has good audio quality above 3 W, continuous output power beyond 3 W must be avoided due to device packaging limitations.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Continuous Output Power	3 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Susceptibility	4 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
9-Ball, 1.5 mm × 1.5 mm WLCSP	1S0P	162	39	°C/W
	2S0P	76	21	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

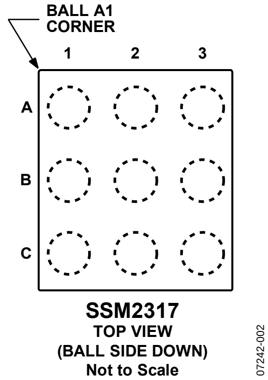

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1A	IN−	Inverting Input.
1B	IN+	Noninverting Input.
1C	GND	Ground.
2A	$\overline{\text{SD}}$	Shutdown Input. Active low digital input.
2B	ALC_EN	Automatic Level Control Enable Input. Active high digital input.
2C	VDD	Power Supply.
3A	VTH	Variable Threshold.
3B	OUT−	Inverting Output.
3C	OUT+	Noninverting Output.

TYPICAL PERFORMANCE CHARACTERISTICS

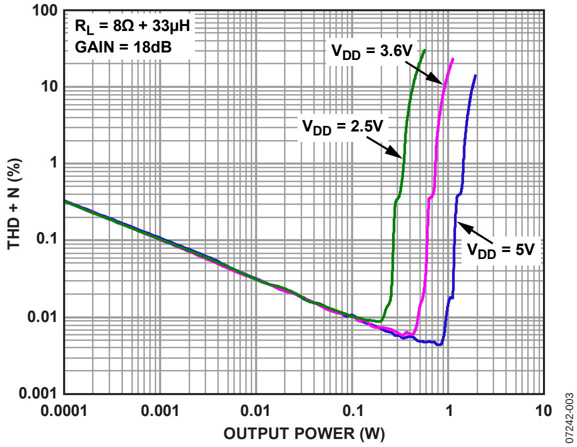

Figure 3. THD + N vs. Output Power into 8 Ω + 33 µH, Gain = 18 dB

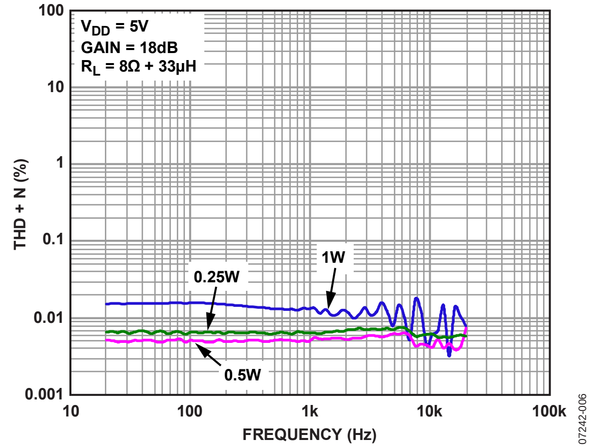

Figure 6. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω + 33 µH, Gain = 18 dB

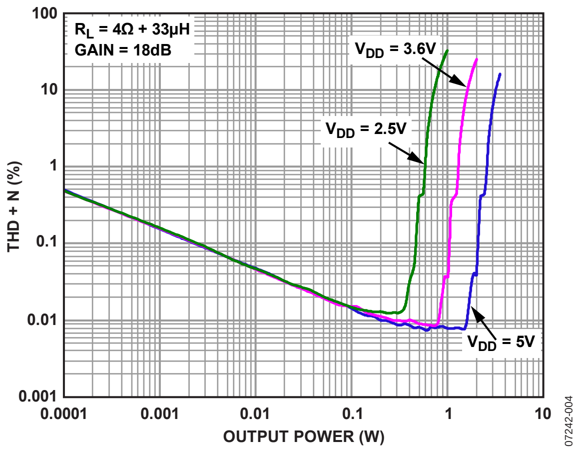

Figure 4. THD + N vs. Output Power into 4 Ω + 33 µH, Gain = 18 dB

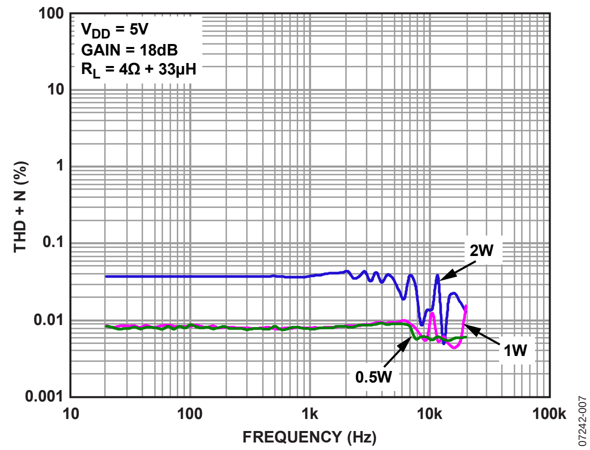

Figure 7. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω + 33 µH, Gain = 18 dB

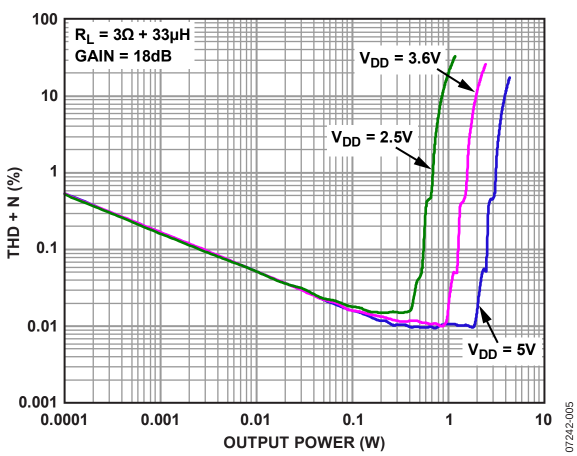

Figure 5. THD + N vs. Output Power into 3 Ω + 33 µH, Gain = 18 dB

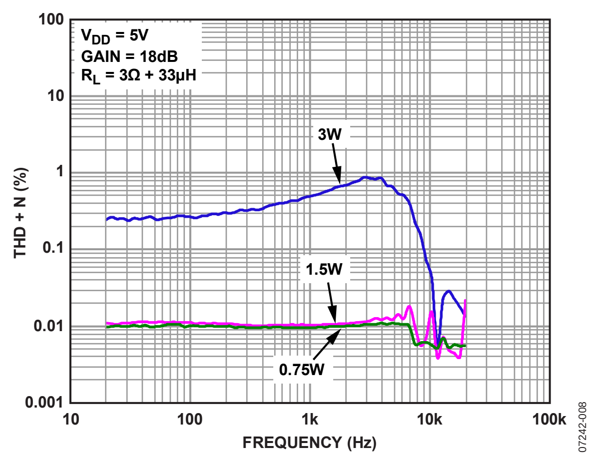

Figure 8. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 3 Ω + 33 µH, Gain = 18 dB

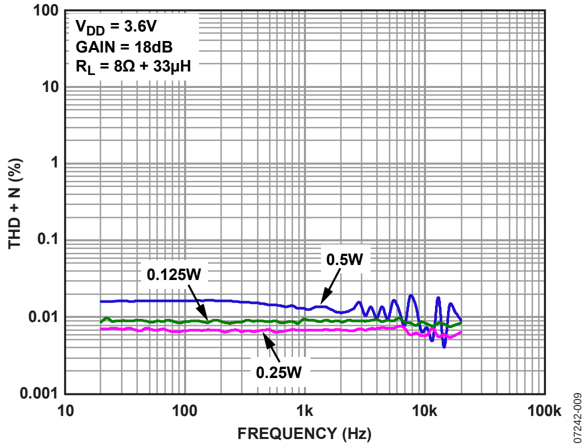

Figure 9. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω + 33 µH, Gain = 18 dB

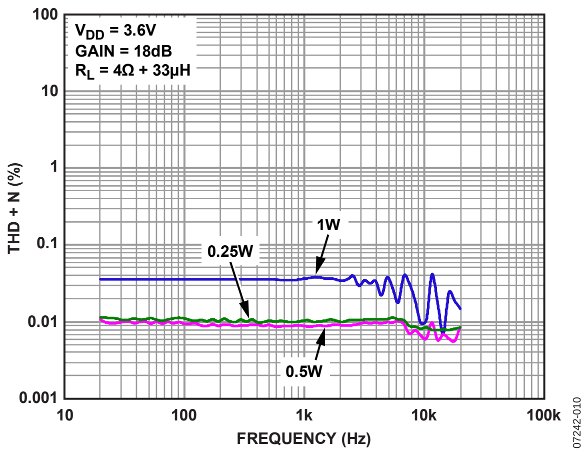

Figure 10. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω + 33 µH, Gain = 18 dB

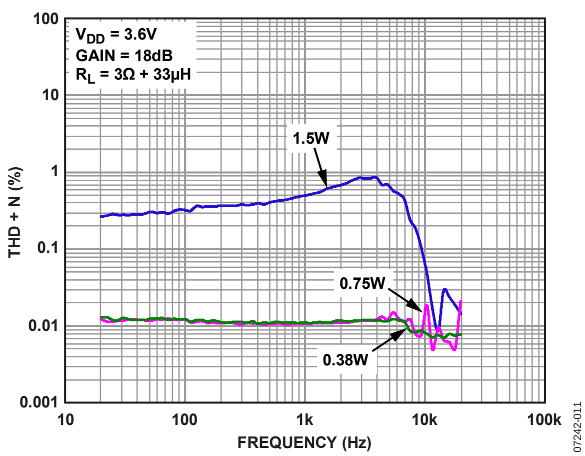

Figure 11. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 3 Ω + 33 µH, Gain = 18 dB

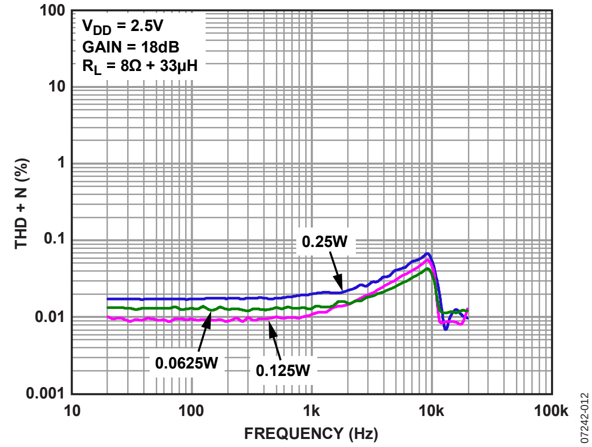

Figure 12. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω + 33 µH, Gain = 18 dB

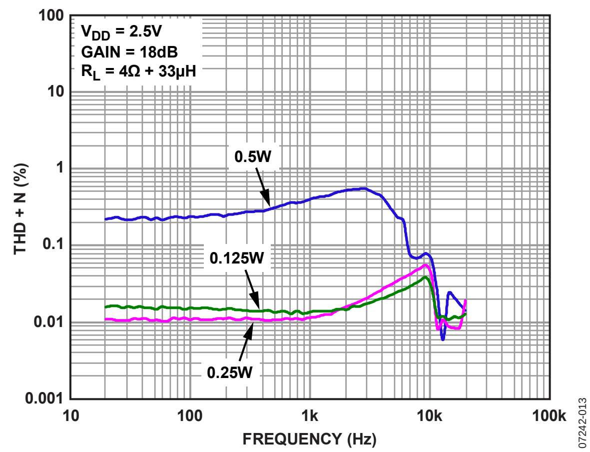

Figure 13. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω + 33 µH, Gain = 18 dB

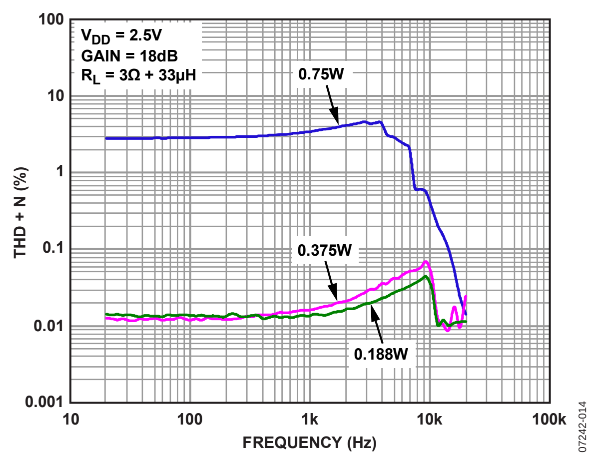

Figure 14. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 3 Ω + 33 µH, Gain = 18 dB

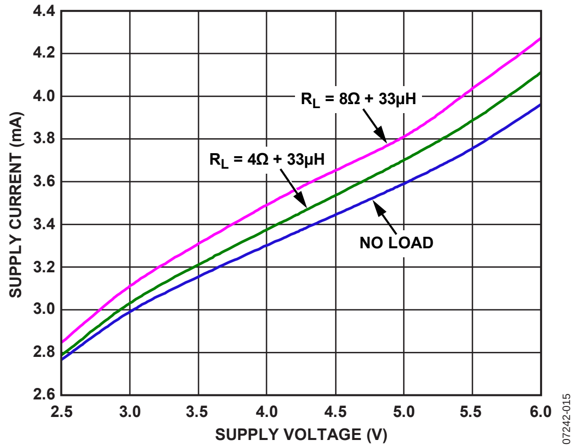

Figure 15. Supply Current vs. Supply Voltage

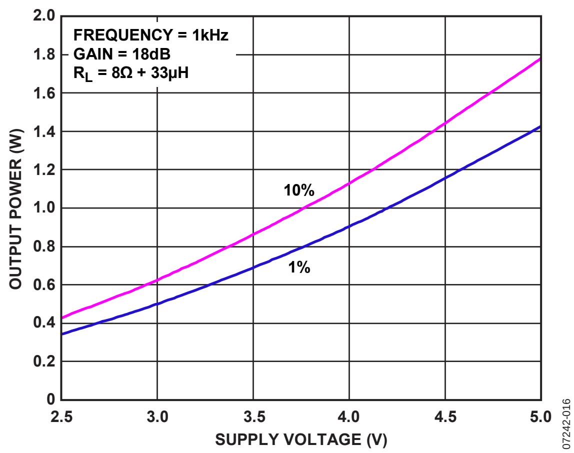

Figure 16. Maximum Output Power vs. Supply Voltage, $R_L = 8\,\Omega + 33\,\mu H$, Gain = 18 dB

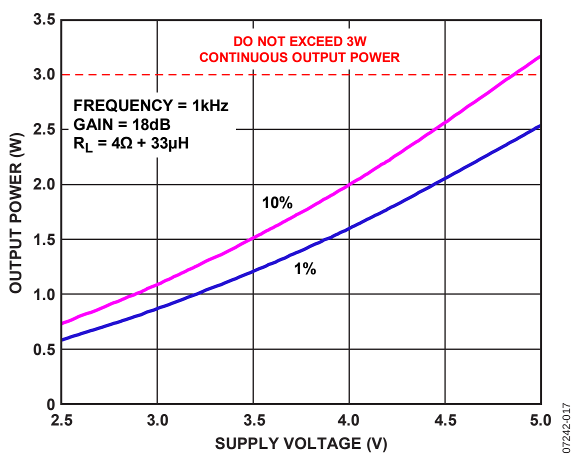

Figure 17. Maximum Output Power vs. Supply Voltage, $R_L = 4\,\Omega + 33\,\mu H$, Gain = 18 dB

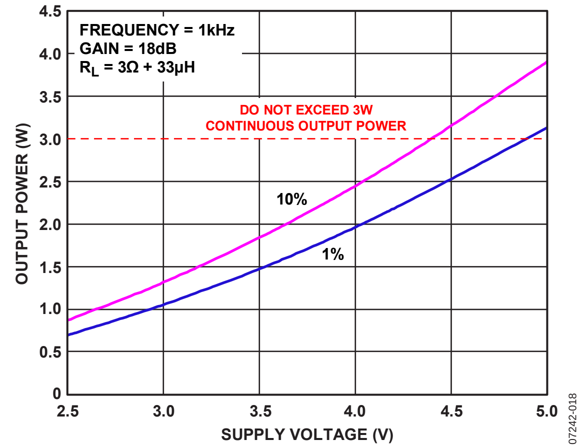

Figure 18. Maximum Output Power vs. Supply Voltage, $R_L = 3\,\Omega + 33\,\mu H$, Gain = 18 dB

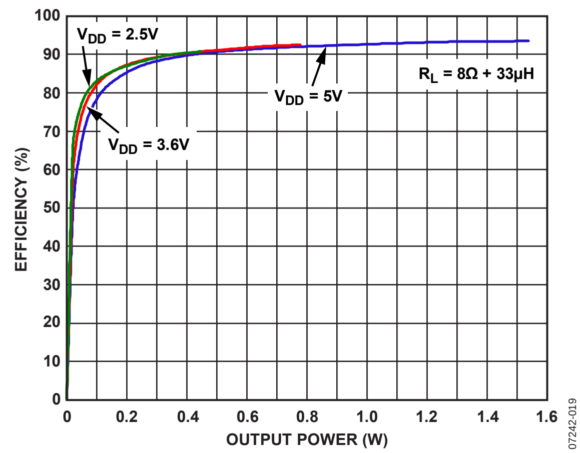

Figure 19. Efficiency vs. Output Power into $8\,\Omega + 33\,\mu H$

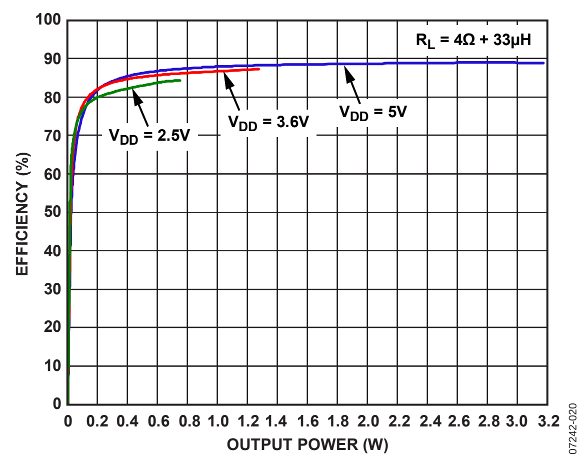

Figure 20. Efficiency vs. Output Power into $4\,\Omega + 33\,\mu H$

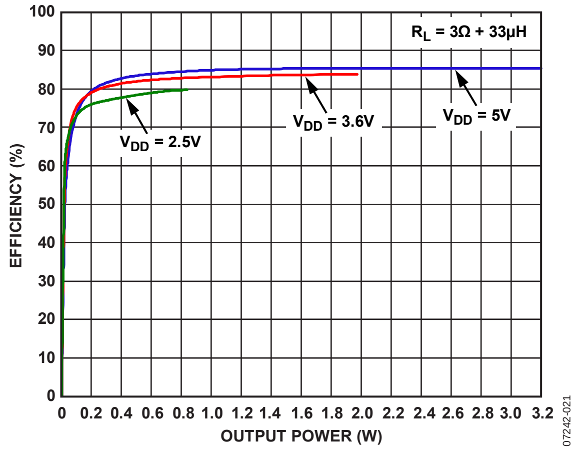

Figure 21. Efficiency vs. Output Power into 3 Ω + 33 µH

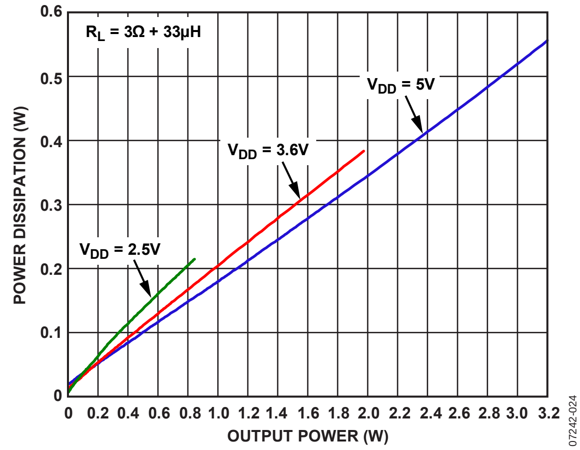

Figure 24. Power Dissipation vs. Output Power into 3 Ω + 33 µH

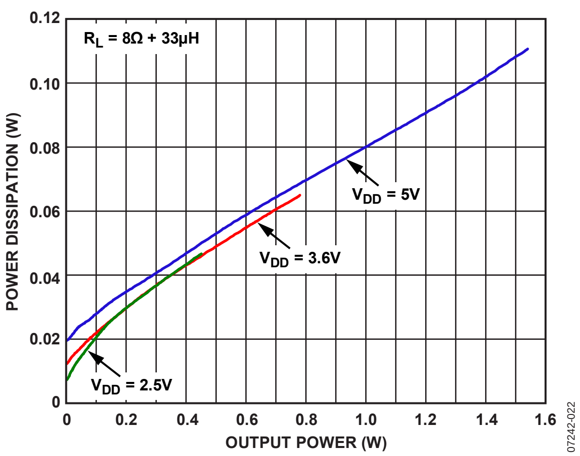

Figure 22. Power Dissipation vs. Output Power into 8 Ω + 33 µH

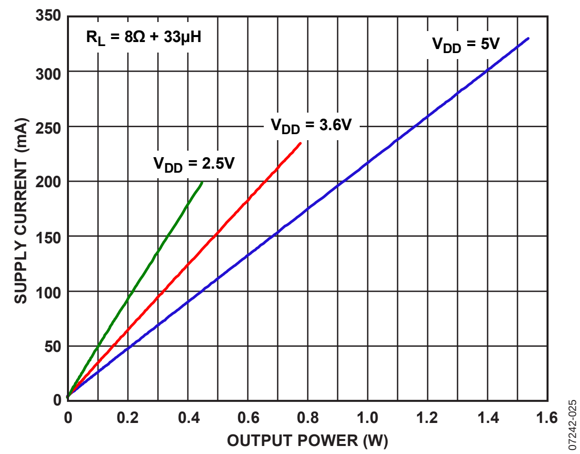

Figure 25. Supply Current vs. Output Power into 8 Ω + 33 µH

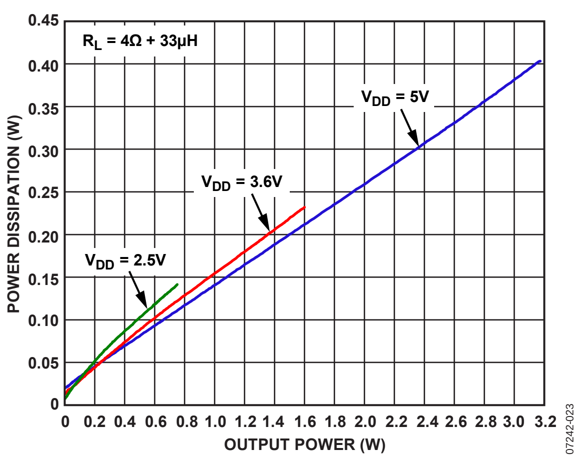

Figure 23. Power Dissipation vs. Output Power into 4 Ω + 33 µH

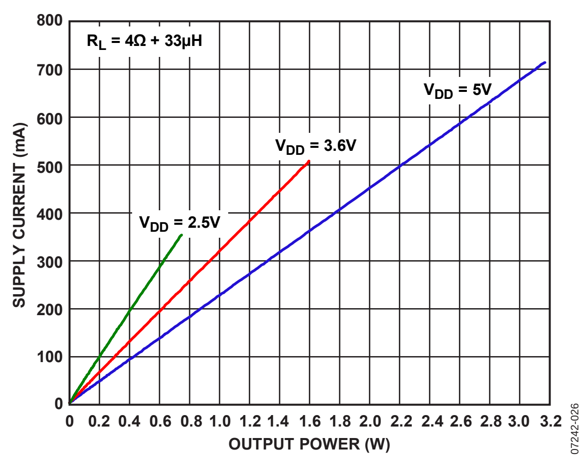

Figure 26. Supply Current vs. Output Power into 4 Ω + 33 µH

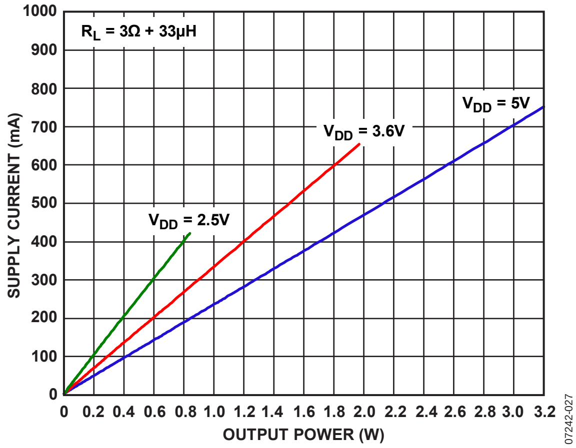

Figure 27. Supply Current vs. Output Power into 3 Ω + 33 µH

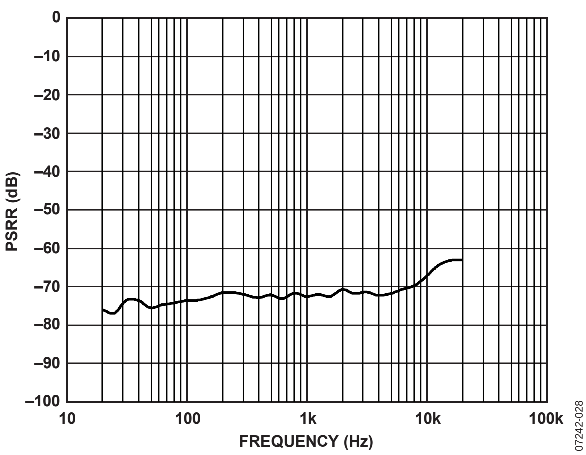

Figure 28. Power Supply Rejection Ratio vs. Frequency

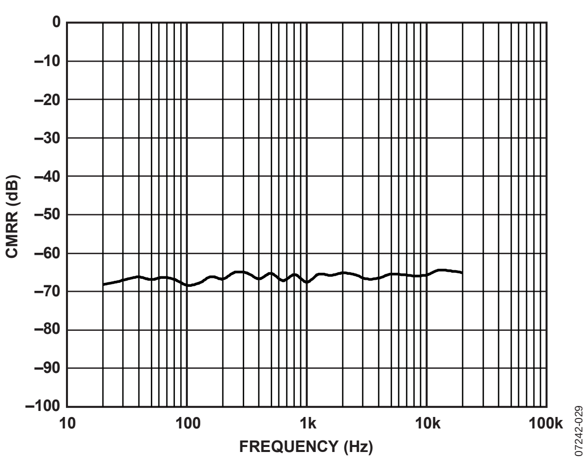

Figure 29. Common-Mode Rejection Ratio vs. Frequency

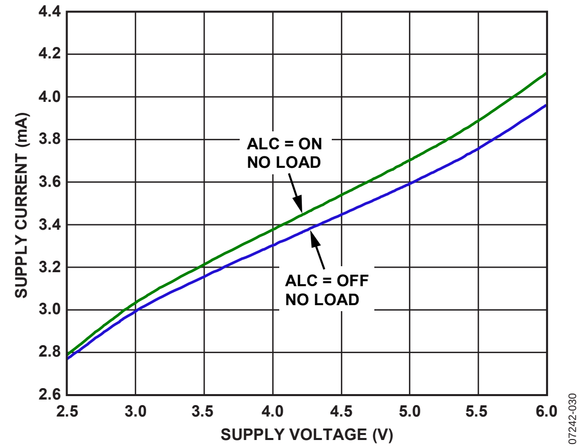

Figure 30. Supply Current vs. Supply Voltage, ALC Contribution

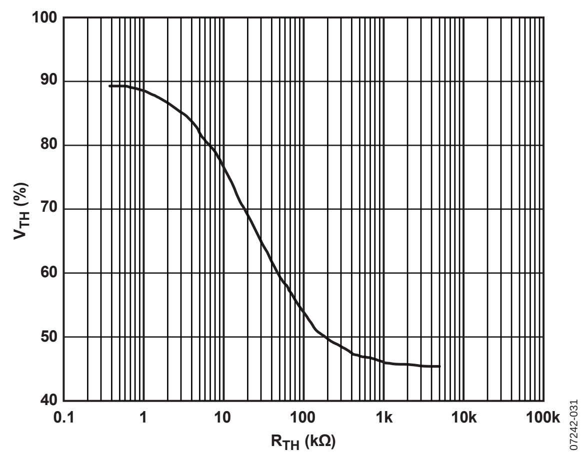

Figure 31. V_{TH} vs. R_{TH}

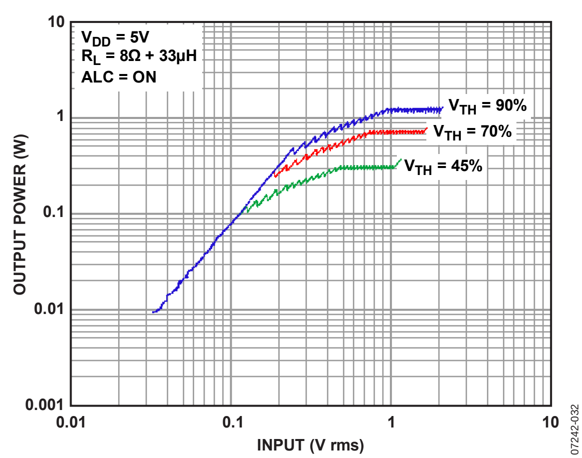

Figure 32. Input/Output Characteristic, V_{DD} = 5 V, ALC = On

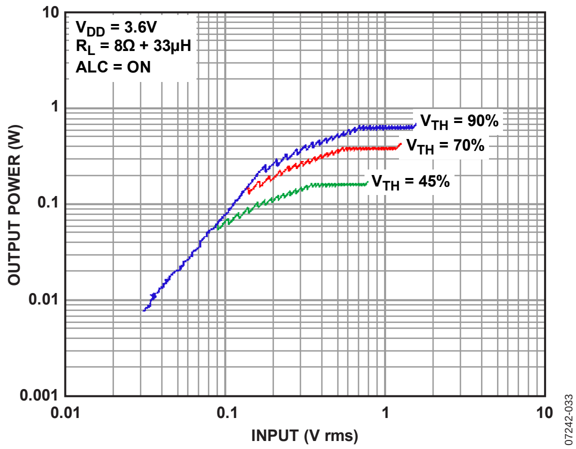

Figure 33. Input/Output Characteristic, V_{DD} = 3.6 V, ALC = On

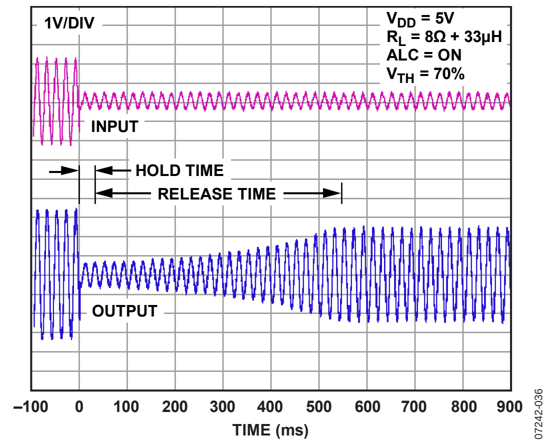

Figure 36. Release Waveform

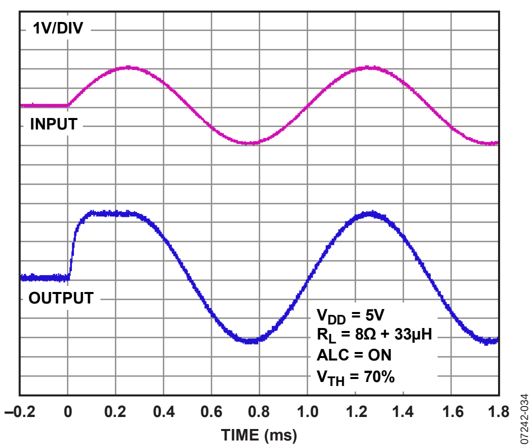

Figure 34. Attack Waveform, 1 kHz Sine Wave

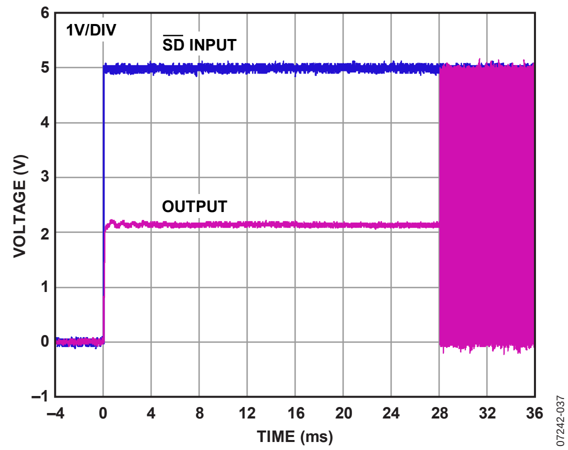

Figure 37. Turn-On Response

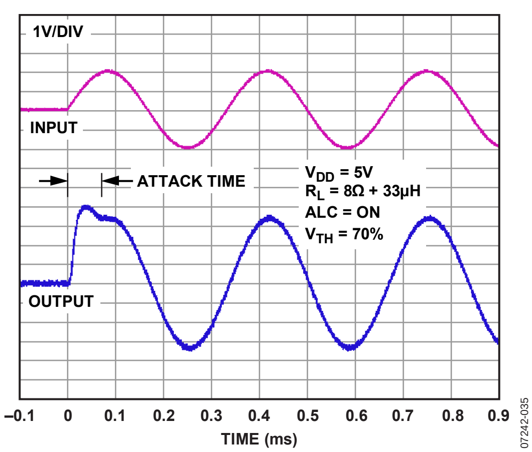

Figure 35. Attack Waveform, 3 kHz Sine Wave

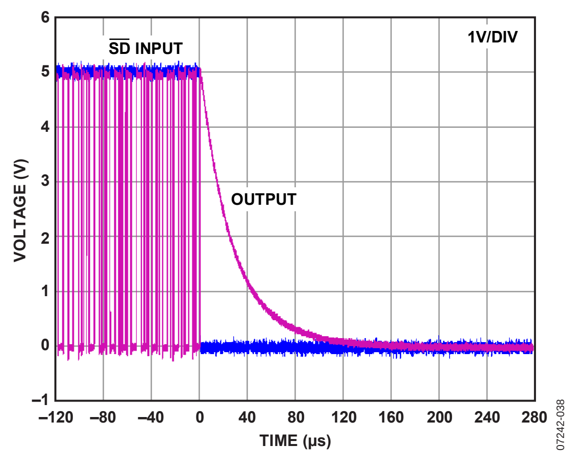

Figure 38. Turn-Off Response

TYPICAL APPLICATION CIRCUITS

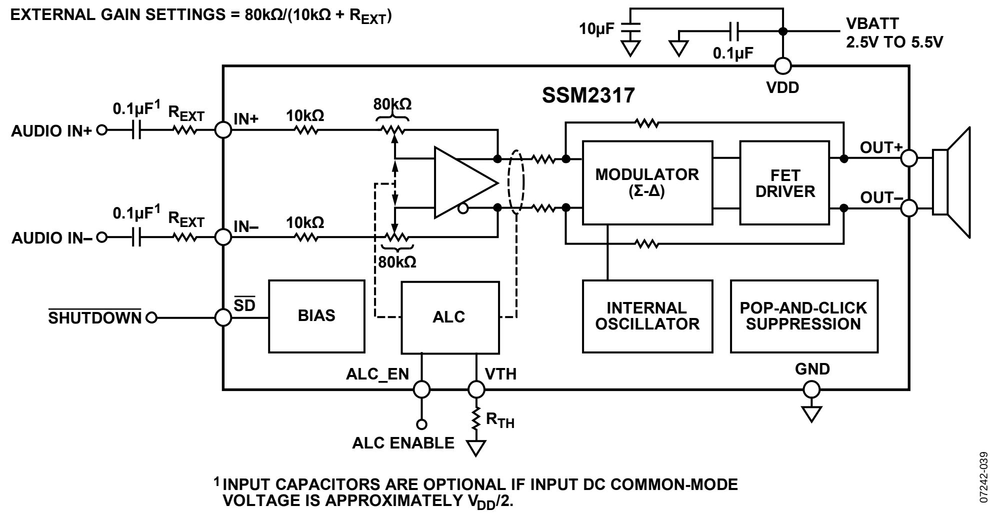

Figure 39. Differential Input Configuration, User-Adjustable Gain

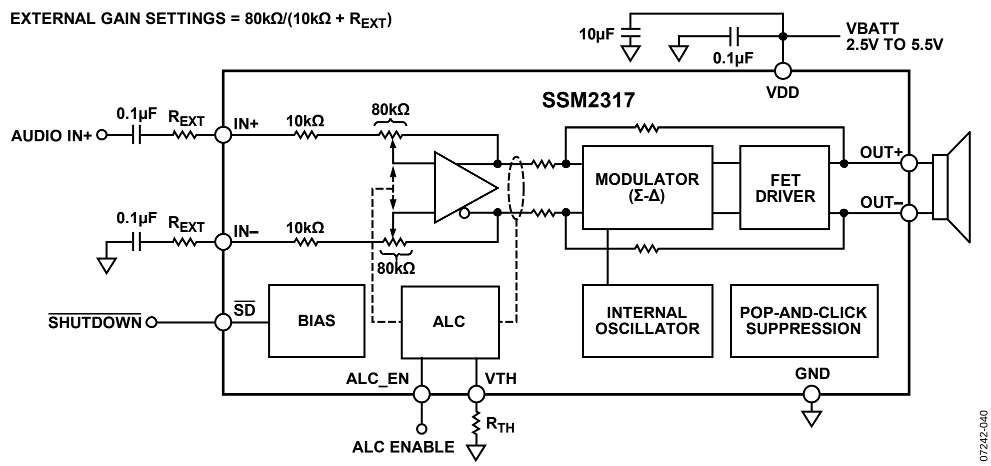

Figure 40. Single-Ended Input Configuration, User-Adjustable Gain

THEORY OF OPERATION

OVERVIEW

The SSM2317 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external components count, conserving board space and, thus, reducing systems cost. The SSM2317 does not require an output filter but instead relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output. Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2317 uses a Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emission that might otherwise be radiated by speakers and long cable traces. Due to the inherent spread spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM2317 amplifiers.

The SSM2317 also offers protection circuits for overcurrent and temperature protection.

GAIN

The SSM2317 has a default gain of 18 dB that can be reduced by using a pair of external resistors with a value calculated as follows:

$$\textit{External Gain Settings} = 80\ k\Omega/(10\ k\Omega + R_{EXT})$$

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of the audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal. Such transients can be generated when the amplifier system changes its operating mode. For example, the following can be sources of audible transients: system power-up/power-down, mute/unmute, input source change, and sample rate change. The SSM2317 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

OUTPUT MODULATION DESCRIPTION

The SSM2317 uses three-level, Σ-Δ output modulation. Each output can swing from GND to VDD and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, there are always noise sources present. Due to this constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

However, most of the time, output differential voltage is 0 V, due to the Analog Devices, Inc., patented three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 41 depicts three-level, Σ-Δ output modulation with and without input stimulus.

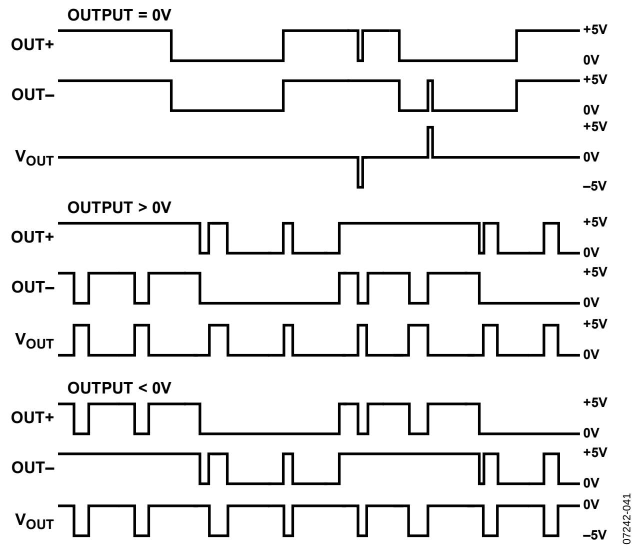

Figure 41. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

LAYOUT

As output power continues to increase, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz of copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layouts isolate critical analog paths from sources of high interference. Separate high frequency circuits (analog and digital) from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossover.

If the system has separate analog and digital ground and power planes, place the analog ground plane underneath the analog power plane, and, similarly, place the digital ground plane underneath the digital power plane. There should be no overlap between analog and digital ground planes or analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2317 does not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor and the input resistor of the SSM2317 form a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/\{2\pi \times (10\ k\Omega + R_{EXT}) \times C_{IN}\}$$

The input capacitor can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset of the amplifier and the dc PSRR performance.

PROPER POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. Although the actual switching frequency can range from 10 kHz to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input needs to be decoupled with a good quality low ESL, low ESR capacitor, usually of around 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transient noises, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2317 helps maintain efficient performance.

AUTOMATIC LEVEL CONTROL (ALC)

Automatic level control (ALC) is a function that automatically adjusts amplifier gain to generate desired output amplitude with reference to a particular input stimulus. The primary motivation for the use of ALC is to protect an audio power amplifier or speaker load from the damaging effects of clipping or current overloading. This is accomplished by limiting the amplifier's output amplitude upon reaching a preset threshold voltage. A less intuitive benefit of ALC is that it makes sound sources with a wide dynamic range more intelligible by boosting low level signals yet limits very high level signals.

Figure 42 shows input vs. output and gain characteristics of ALC that is implemented in the SSM2317.

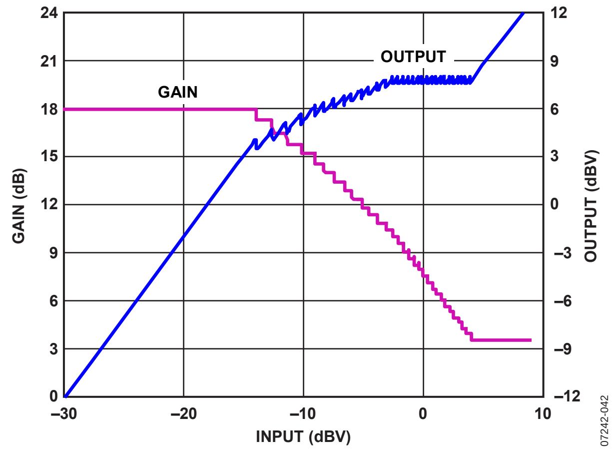

Figure 42. Input/Output Characteristic and Gain

When the input level is small and below the ALC threshold value, the gain of the amplifier stays at 18 dB. When the input exceeds the ALC threshold value, the ALC begins to gradually reduce the gain from 18 dB to 3.5 dB.

OPERATING MODES

The ALC implemented on SSM2317 has two operating modes: compression and limiting. At the time the ALC is triggered for medium level input, the ALC is in compression mode. In this mode, an increase of the output signal is 1/3 of the increase of the input signal. For example, if the input signal increases by 3 dB, the ALC reduces the amplifier gain by 2 dB and thus the output signal only increases by 1 dB.

As the input signal becomes very large, the ALC transitions into limiting operation mode. In this mode, the output stays at a given threshold level, V_{TH}, even if the input signal grows larger. For example, when a large input signal increases by 3 dB, the ALC reduces the amplifier gain by 3 dB and thus the output increases 0 dB. When the amplifier gain is reduced to 3.5 dB, ALC cannot further reduce the gain and the output increases again. To avoid potential speaker damage, the maximum input signal should not be large enough to exceed the maximum attenuation (3.5 dB) of the limiting operational mode.

ATTACK TIME, HOLD TIME, AND RELEASE TIME

When the amplifier input exceeds a preset threshold, ALC reduces amplifier gain rapidly until its output settles to a target level. This gain level is maintained for a certain period. If the input does not exceed the threshold again, ALC increases the gain gradually. The attack time is the time taken to reduce the gain from maximum to minimum. The hold time is the time to sustain the reduced gain. The release time is the time taken to increase the gain from minimum to maximum. These times are shown in Table 5.

Table 5. Attack, Hold, and Release Times

Time	Duration (ms)
Attack Time	0.1
Hold Time	35
Release Time	550

OUTPUT THRESHOLD

The maximum output amplitude threshold (V_{TH}) during the limiting mode can be changed from 90% to 45% of V_{DD} by having an external resistor, R_{TH}, between the VTH pin and GND. Shorting the VTH pin to GND sets V_{TH} to 90% of V_{DD}. Leaving the VTH pin unconnected sets V_{TH} to 45% of V_{DD}. The relation of R_{TH} to V_{TH} is shown by the following equation:

$$V_{TH} = 0.9 \times \frac{50\ \text{k}\Omega + R_{TH}}{50\ \text{k}\Omega + 2 \times R_{TH}} \times V_{DD}$$

Maximum output power is derived from V_{TH} by the following equation:

$$P_{OUT} = \frac{\left(\frac{V_{TH}}{\sqrt{2}}\right)^2}{R_{SP}}$$

where R_{SP} is the speaker impedance.

Figure 43 shows the relationship between the R_{TH} value and V_{TH}. Figure 44 shows the relationship between the maximum output power and the R_{TH} value.

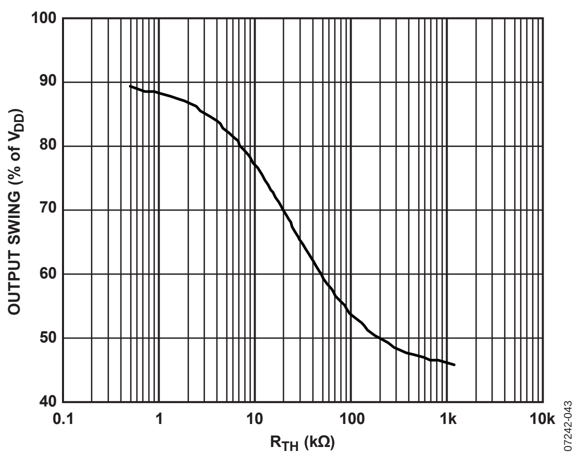

Figure 43. Output Threshold (V_{TH}) vs. R_{TH}

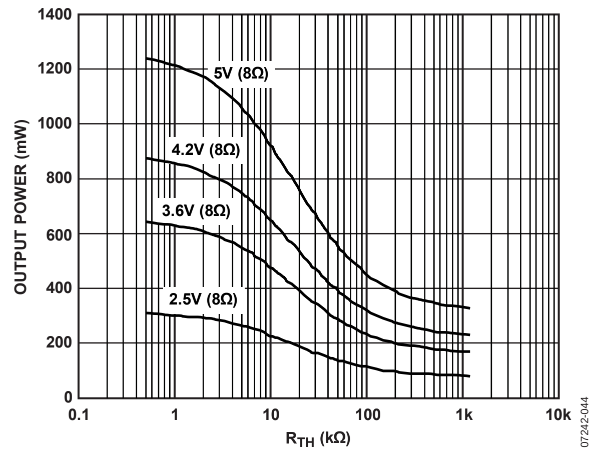

Figure 44. Maximum Output Power vs. R_{TH}

ENABLE/DISABLING ALC

The ALC function is enabled when the ALC_EN pin is set to V_{DD}. The ACL function can be enabled and disabled during amplifier operation. As a result of enabling ALC, I_{SY} increases by 100 μA and there is less than 50 μA source current from the VTH pin to GND via R_{TH}. When ALC is disabled, the source current is 0 μA and the VTH pin is tied to GND.

OUTLINE DIMENSIONS

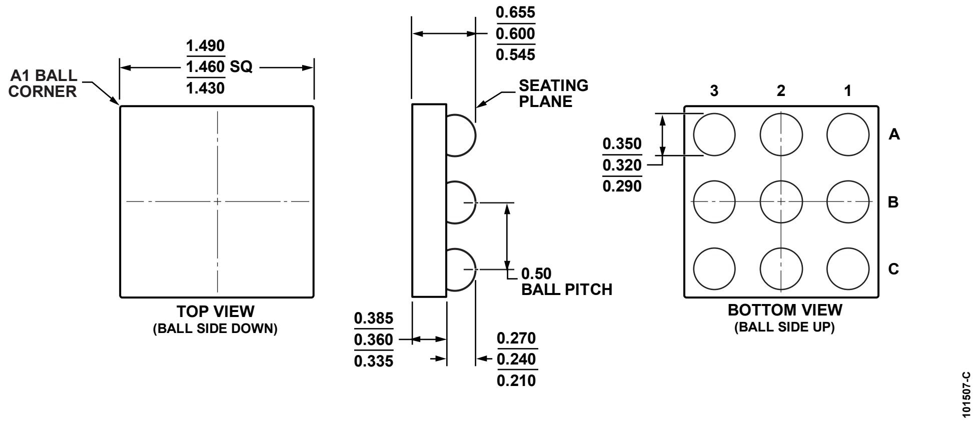

Figure 45. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-9-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
SSM2317CBZ-REEL[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2	Y0Z
SSM2317CBZ-REEL7[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2	Y0Z
SSM2317-EVALZ[1]		Evaluation Board		
SSM2317-MINI-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

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