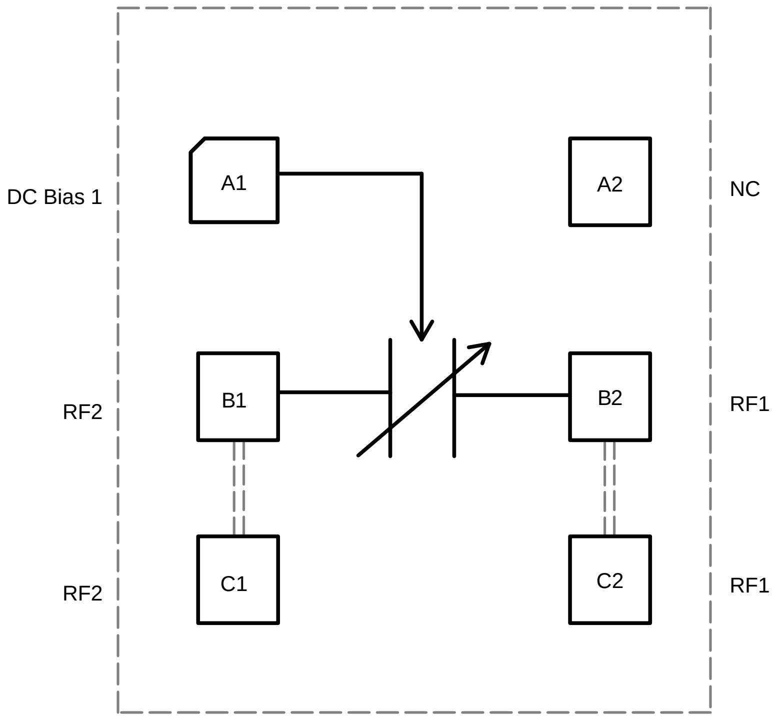


Figure 1. PTIC Functional Block Diagram (Top View)

Table 1. SIGNAL DESCRIPTIONS

Ball / Pad Number	Pin Name	Description
A1	DC Bias 1	DC Bias Voltage
B1	RF2	RF Output
C1	RF2	RF Output
A2	NC	Not Connected
B2	RF1	RF Input
C2	RF1	RF Input

TYPICAL SPECIFICATIONS

Representative Performance Data at 25°C

Table 2. PERFORMANCE DATA

Parameter	Min	Typ	Max	Unit
Operating Bias Voltage	1.0		24	V
Capacitance (V_{bias} = 2 V)	2.457	2.70	2.943	pF
Capacitance (V_{bias} = 24 V)	0.528	0.581	0.633	pF
Tuning Range (1 V − 24 V)	4.80	5.25	6.00	
Tuning Range (2 V − 24 V)	4.20	4.65	5.30	
Leakage Current (V_{bias} = 24 V)			0.1	μA
Operating Frequency	700		2700	MHz
Quality Factor @ 700 MHz, 2 V (Note 5)		65		
Quality Factor @ 700 MHz, 24 V (Note 5)		85		
Quality Factor @ 2.4 GHz, 2 V (Note 5)		40		
Quality Factor @ 2.4 GHz, 24 V (Note 5)		35		
IP3 (V_{bias} = 2 V) [1,3] (Note 5)		70		dBm
IP3 (V_{bias} = 24 V) [1,3] (Note 5)		80		dBm
2nd Harmonic (V_{bias} = 2 V) (Notes 2, 3 and 5)		−65		dBm
2nd Harmonic (V_{bias} = 24 V) (Notes 2, 3 and 5)		−75		dBm
3rd Harmonic (V_{bias} = 2 V) (Notes 2, 3 and 5)		−45		dBm
3rd Harmonic (V_{bias} = 24 V) (Notes 2, 3 and 5)		−75		dBm
Average Transition Time (Cmin → Cmax) (Notes 4 and 5)		66		μs
Average Transition Time (Cmax → Cmin) (Notes 4 and 5)		48		μs

1. f_1 = 850 MHz, f_2 = 860 MHz, Pin 25 dBm/Tone
2. 850 MHz, Pin +34 dBm
3. IP3 and Harmonics are measured in the shunt configuration in a 50 Ω environment
4. RF_{IN} and RF_{OUT} are both connected to DC ground
5. Sample testing only. Average Transition Time for all start and stop voltage combinations between 2 V and 24 V is 50 μs.

Representative performance data at 25°C for 2.7 pF WLCSP Package

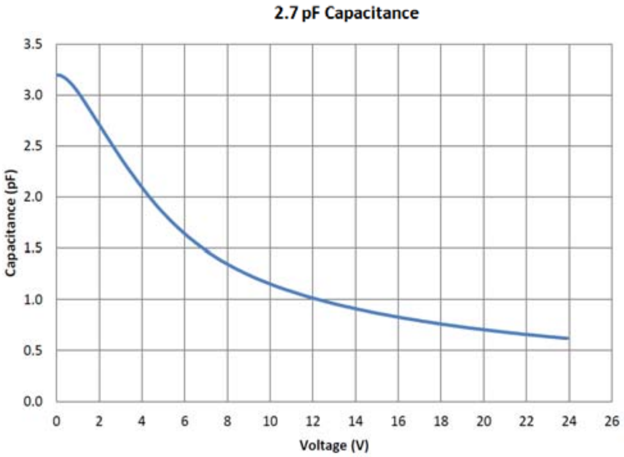


Figure 2. Capacitance

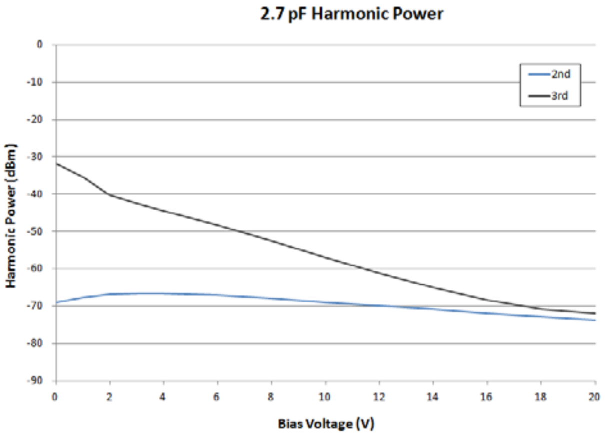


Figure 3. Harmonic Power*

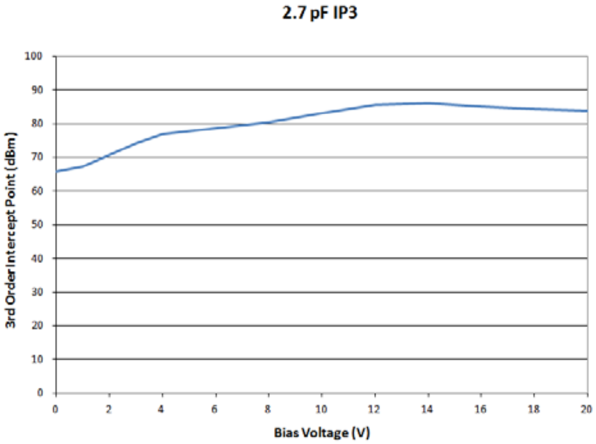


Figure 4. IP3*

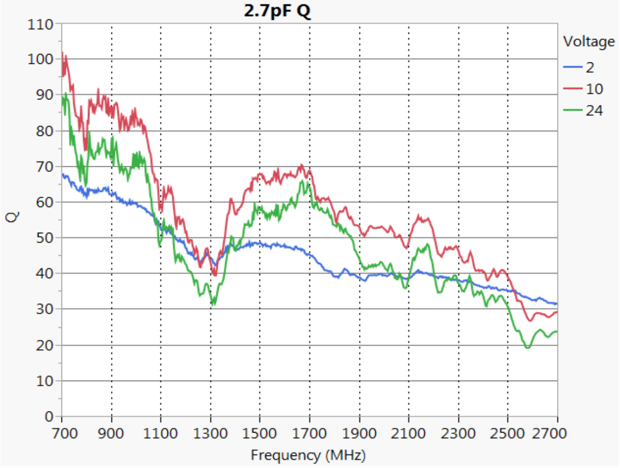


Figure 5. Q*

*Data shown is representative only.

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Input Power	+40	dBm
Bias Voltage	+30 (Note 6)	V
Operating Temperature Range	−30 to +85	°C
Storage Temperature Range	−55 to +125	°C
ESD − Human Body Model	Class 1B JEDEC HBM Standard (Note 7)	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. WLCSP: Recommended Bias Voltage not to exceed 24 V.
7. Class 1B defined as passing 500 V, but may fail after exposure to 1000 V ESD pulse.

ASSEMBLY CONSIDERATIONS AND REFLOW PROFILE

The following assembly considerations should be observed:

Cleanliness

These chips should be handled in a clean environment.

Electro−static Sensitivity

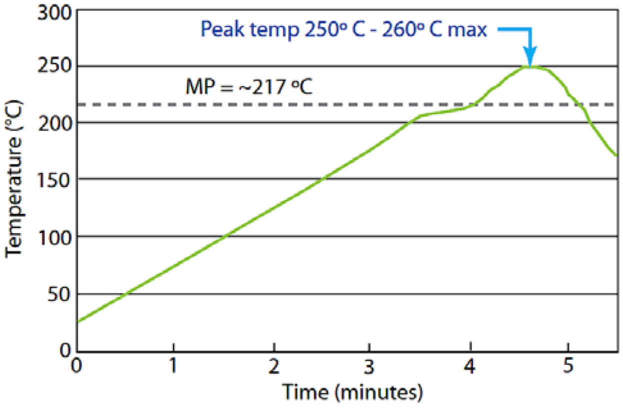
ON Semiconductor’s PTICs are ESD Class 1B sensitive. The proper ESD handling procedures should be used.

Mounting

The WLCSP PTIC is fabricated for Flip Chip solder mounting. Connectivity to the RF and Bias terminations on the PTIC die is established through SAC305 solder balls with 90 μm nominal height (65 μm to 115 μm height variation). The PTIC die is RoHS−compliant and compatible with lead−free soldering profile.

Molding

The PTIC die is compatible for over−molding or under−fill.



This reflow profile is a guideline for Pb-free solder materials. Adjustments to this profile are necessary based on specific process requirements and board size, thickness and density. ***Not to exceed 260° C for 5 seconds.***

Figure 6. Reflow Profile

ORIENTATION OF THE PTIC FOR OPTIMUM LOSSES

When configuring the PTIC in your specific circuit design, at least one of the RF terminals must be connected to DC ground. If minimum transition times are required, DC ground on both RF terminals is recommended. To minimize losses, the PTIC should be oriented such that RF2 is at the lower RF impedance of the two RF nodes. A shunt PTIC, for example, should have RF2 connected to RF ground.

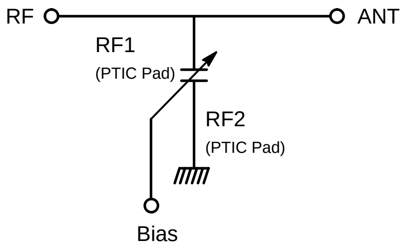


Figure 7. PTIC Orientation Functional Block Diagram

PART NUMBER DEFINITION

Table 4. PART NUMBERS

Part Number	Capacitance		Marking		Package*
	2 V	24 V	Device ID	Trace Code	
TCP−5027UB−DT	2.70	0.581	C	YW**	6−bump WLCSP

*See PTIC package dimensions on following page.
**Refer to table below (Table 5) for YW trace code.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

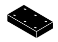
Table 5. Two Digits Year and Work Week Date coding (YW) − In Process Product / Traceability Date Code Marking

Code	Term	Definition								
YW	**Year and Work Week**	**Two−character Alpha Code. Example: 2005, workweek 10 = GJ**								
		YEAR	WORK WEEK	CODE	YEAR	WORK WEEK	CODE	YEAR	WORK WEEK	CODE
		2003	1 26 27 52	CA CZ DA DZ	2004	1 26 27 52	EA EZ FA FZ	2005	1 26 27 52	GA GZ HA HZ
		2006	1 26 27 52	IA IZ JA JZ	2007	1 26 27 52	KA KZ LA LZ	2008	1 26 27 52	MA MZ NA NZ
		2009	1 26 27 52	PA PZ RA RZ	2010	1 26 27 52	SA SZ TA TZ	2011	1 26 27 52	UA UZ VA VZ
		2012	1 26 27 52	WA WZ XA XZ	2013	1 26 27 52	YA YZ ZA ZZ	2014	1 26 27 52	AA AZ BA BZ
		2015	1 26 27 52	CA CZ DA DZ	2016	1 26 27 52	EA EZ FA FZ	2017	1 26 27 52	GA GZ HA HZ

For dates outside of the table: the first character of the code is incremented at the start of workweek 01 and workweek 27 each year. The second character begins with “A” in workweek 01 of each year and increments weekly. “A” follows “Z” to make the code continuous.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

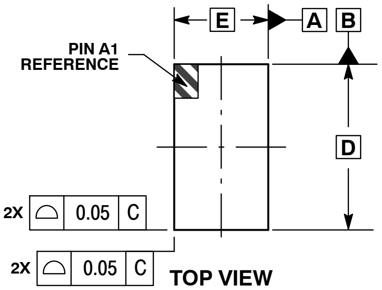
ON Semiconductor®



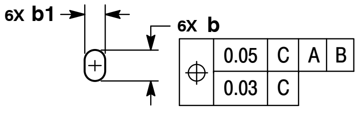
SCALE 4:1

WLCSP6, 1.097x0.622
CASE 567NZ
ISSUE A

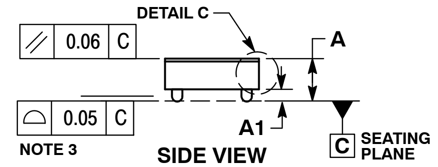
DATE 27 SEP 2016



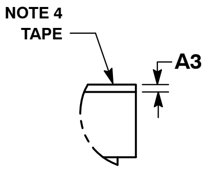
TOP VIEW



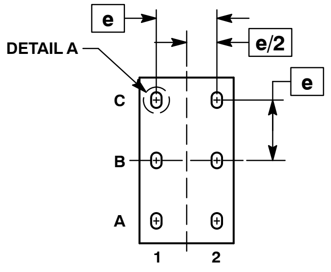
DETAIL A



SIDE VIEW



DETAIL C



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. BACKSIDE TAPE APPLIED TO IMPROVE PIN 1 MARKING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.295	0.335	0.375
A1	0.065	0.090	0.115
A3	0.025 REF		
b	0.125	0.150	0.175
b1	0.075	0.100	0.125
D	1.047	1.097	1.147
E	0.572	0.622	0.672
e	0.40 BSC		

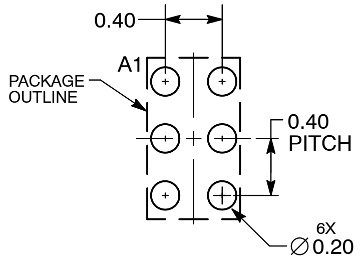
GENERIC MARKING DIAGRAM*

XYW
∘

X = Specific Device Code
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP6, 1.097X0.622**	**PAGE 1 OF 1**

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