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TDA7802

1 Block diagram and pins description

1.1 Block diagram



1.2 Pins description







Table 2.	Flexiwatt27	pins	description
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N°	Pin	Function		
1	ТАВ	TAB connection	Ground	
2	PLLen	PII loop filter / ENABLE	Input	
3	PWGND2	Power ground channel 2	Power Ground	
4	OUT 2-	Channel 2 (Left Rear) negative output	Power Output	
5	WS	Word select (I2S bus)	Logic Input	
6	OUT 2+	Channel 2 (Left Rear) positive output	Power Output	
7	VCC12	Channel 1 and 2 positive supply	Battery	
8	OUT 1-	Channel 1 (Left Front) negative output	Power Output	
9	PWGND1	Power ground channel 1	Power Ground	
10	OUT 1+	Channel 1 (Left Front) positive output	Power Output	
11	SCK	Serial clock (I2S bus)	Logic Input	
12	SD24	Serial data channels 2 and 4 (I2S bus)	Logic Input	
13	SD13	Serial data channels 1 and 3 (I2S bus) Logic Inpu		
14	DGND	Digital ground Signal Gro		
15	AGND	Analog ground	Signal Ground	
16	D3V3	Digital 3.3 V supply filter	Digital Regulator	
17	A3V3	Analog 3.3 V supply filter	Analog Regulator	
18	OUT3+	Channel 3 (right front) positive output	Power Output	
19	PWGND3	Power ground channel 3	Power Ground	
20	OUT3-	Channel 3 (right front) negative output	Power Output	
21	VCC34	Channels 3 and 4 positive supply	Battery	
22	OUT4+	Channel 4 (right rear) positive output	Power Output	
23 CDdiag		Clip detector and diagnostic output: Overcurrent protection intervention Thermal warning POR Output DC offset Output short to VCC/GND	Open Drain Output	
24	OUT4-	Channel 4 (right rear) negative output Power Output		
25	PWGND4	Power ground channel 4	Power Ground	
26	SDAIm	I ² C data/legacy mode mute	Signal Input/Output	
27	SCLlen	I ² C clock/enable legacy mode	Signal Input	



Table 3.	PowerSO36	pins	description	ı
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N°	Pin	Function	
1	TAB	TAB TAB connection	
2 CDdiag		Clip detector and diagnostic output: Overcurrent protection intervention Thermal warning POR	Open Drain Output
3	OUT4-	Channel 4 (right rear) negative output	Power Output
4	VCC34	Channels 3 and 4 positive supply	Battery
5	PWGND4	Power ground channel 4	Power Ground
6	VCC34	Channels 3 and 4 positive supply	Battery
7	OUT4+	Channel 4 (right rear) positive output	Power Output
8	SDAIm	I ² C data/legacy mode mute	Signal Input/Output
9	SCLlen	I ² C clock/enable legacy mode	Signal Input
10	ADD1	I2C Address - First Pin	Logic Input
11	PLLen	PII loop filter / ENABLE	Input
12	OUT 2+	Channel 2 (Left Rear) positive output	Power Output
13	VCC12	Channel 1 and 2 positive supply	Battery
14	14 NC Not Connected -		-
15	PWGND2	VGND2 Power ground channel 2 Power G	
16	VCC12	Channel 1 and 2 positive supply	Battery
17	OUT 2-	Channel 2 (Left Rear) negative output	Power Output
18	WS	Word select (I2S bus)	Logic Input
19	OUT 1-	Channel 1 (Left Front) negative output	Power Output
20	LOAD1A	Load Selection (channels 1 and 2)	Logic Input
21	LOAD1B	Load Selection (channels 3 and 4)	Logic Input
22	PWGND1	Power ground channel 1	Power Ground
23	OUT 1+	Channel 1 (Left Front) positive output	Power Output
24	NC	Not Connected	-
25	SCK	Serial clock (I2S bus)	Logic Input
26	SD24	Serial data channels 2 and 4 (I2S bus)	Logic Input
27	SD13	Serial data channels 1 and 3 (I2S bus)	Logic Input
28	DGND	Digital ground	Signal Ground
29	AGND	ND Analog ground Signal Ground	
30	D3V3	Digital 3.3 V supply filter	Digital Regulator
31	A3V3	Analog 3.3 V supply filter	Analog Regulator
32	OUT3+	Channel 3 (right front) positive output Power Output	
33	PWGND3	Power ground channel 3	Power Ground
34	UNMUTEhw	Unmute Hardware	Logic input
35	ADD2	I2C Address - Second Pin	Logic Input
36	OUT3-	Channel 3 (right front) negative output	Power Output



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*.

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Figure 3. PowerSO36 (slug up) mechanical data and package dimensions

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Figure 4. Flexiwatt27 (vertical) mechanical data and package dimensions





Figure 5. Flexiwatt27 (SMD) mechanical data and package dimensions



3 Revision history

Date	Revision	Changes	
18-Jul-2013	1	Initial release.	
18-Sep-2013	2	Updated Disclaimer.	
24-Oct-2014	3	Added 'AEC Q100 rev. G compliant' in <i>Features</i> list.	
27-Oct-2014	4	Modified in cover page the feature 'AEC Q100 rev. G compliant' in 'Qualification in accordance to AEC Q100 rev. G standard'.	

Table 4. Document revision history



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