ADMCF326–SPECIFICATIONS (V_{DD} = 5 V ± 5%, GND = 0 V, T_A = –40°C to +85°C, CLKIN = 10 MHz, unless otherwise noted.)

ANALOG-TO-DIGITAL CONVERTER

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Signal Input	0.3		3.5	V	V1, V2, V3, VAUX0, VAUX1, VAUX2
Resolution[1]			12	Bits	
Linearity Error[2]		2	4	Bits	
Zero Offset[2]	–20	0	+20	mV	
Channel-to-Channel Comparator Match[2]			20	mV	
Comparator Delay		600		ns	
ADC High Level Input Current[2]			10	µA	V_{IN} = 3.5 V
ADC Low Level Input Current[2]	–10			µA	V_{IN} = 0.0 V

NOTES
[1]Resolution varies with PWM switching frequency (double update mode) 78.1 kHz = 8 bits, 4.9 kHz = 12 bits.
[2]2.44 kHz sample frequency, V1, V2, V3, VAUX0, VAUX1, VAUX2

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Parameter		Min	Typ	Max	Unit	Conditions/Comments
V_{IL}	Low Level Input Voltage			0.8	V	
V_{IH}	High Level Input Voltage	2			V	
V_{OL}	Low Level Output Voltage[1]			0.4	V	I_{OL} = 2 mA
V_{OL}	Low Level Output Voltage[2]			0.8	V	I_{OL} = 2 mA
V_{OH}	High Level Output Voltage	4			V	I_{OH} = –0.5 mA
I_{IL}	Low Level Input Current[3]	–120			µA	V_{IN} = 0 V
I_{IL}	Low Level Input Current	–10			µA	V_{IN} = 0 V
I_{IH}	High Level Input Current[4]			90	µA	V_{IN} = V_{DD}
I_{IH}	High Level Input Current			10	µA	V_{IN} = V_{DD}
I_{OZH}	High Level Three-State Leakage Current[5]			90	µA	V_{IN} = V_{DD}
I_{OZL}	Low Level Three-State Leakage Current[5]	–10			µA	V_{IN} = 0
I_{IL}	Low Level $\overline{\text{PWMTRIP}}$ Current	–10			µA	@ V_{DD} = Max, V_{IN} = 0 V
I_{DD}	Supply Current (Idle)[6]			41	mA	
I_{DD}	Supply Current (Dynamic)[6]			108	mA	
	Supply Current Programming[6]			123	mA	

NOTES
[1]Output Pins PIO0–PIO8, AH, AL, BH, BL, CH, CL
[2]XTAL Pin
[3]Internal Pull-Up, $\overline{\text{RESET}}$
[4]Internal Pull-Down, $\overline{\text{PWMTRIP}}$, PIO0–PIO8
[5]Three stateable pins DT1, RFS1, TFS1, SCLK1
[6]Outputs not switching

Specifications subject to change without notice.

CURRENT SOURCE[1]

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Programming Resolution			3	Bits	
Default Current[2]	65	83	95	µA	ICONST_TRIM = 0x00
Tuned Current	95	100	105	µA	

NOTES
[1]For ADC Calibration
[2]0.3 V to 3.5 V ICONST Voltage

Specifications subject to change without notice.

VOLTAGE REFERENCE

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Voltage Level (V_{REF})	2.40	2.50	2.60	V	
	2.45	2.50	2.55	V	T_A = 25°C to 85°C SOIC
Output Voltage Drift		35		ppm/°C	

Specifications subject to change without notice.

POWER-ON RESET

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Reset Threshold (V_{RST})	3.2	3.7	4.2	V	
Hysteresis (V_{HYST})		100		mV	
Reset Active Timeout Period (t_{RST})		3.2*		ms	

*2^{16} CLKOUT Cycles.

Specifications subject to change without notice.

FLASH MEMORY

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Endurance	10,000			Cycles	Cycle = Erase/Program/Verify
Data Retention	15			Years	
Program and Erase Operating Temperature	0		85	°C	
Read Operating Temperature	–40		+85	°C	

Specifications subject to change without notice.

TIMING PARAMETERS

Parameter		Min	Max	Unit
Clock Signals				
Signal t_{CK} is defined as 0.5 t_{CKIN}. The ADMCF326 uses an input clock with a frequency equal to half the instruction rate; a 10 MHz input clock (equivalent to 100 ns) yields a 50 ns processor cycle (equivalent to 20 MHz). When t_{CK} values are within the range of 0.5 t_{CKIN} period, they should be substituted for all relevant timing parameters to obtain specification value. Example: t_{CKH} = 0.5 t_{CK} – 10 ns = 0.5 (50 ns) – 10 ns = 15 ns.				
Timing Requirements:				
t_{CKIN}	CLKIN Period	100	150	ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	0.5 t_{CK} – 10		ns
t_{CKH}	CLKOUT Width High	0.5 t_{CK} – 10		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	5 t_{CK}*		ns
PWM Shutdown Signals				
Timing Requirement:				
t_{PWMTPW}	$\overline{\text{PWMTRIP}}$ Width Low	t_{CK}		ns

*Applies after Power-Up Sequence is Complete

Specifications subject to change without notice.

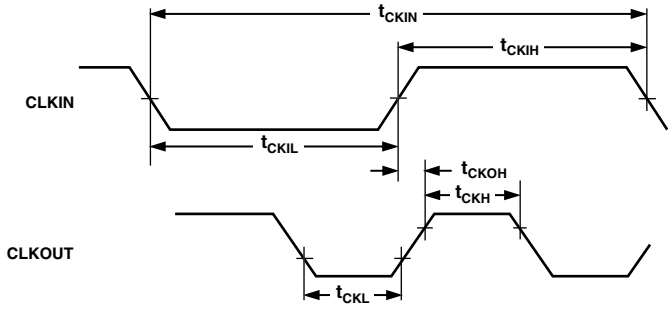


Figure 1. Clock Signals

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	100		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	15		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	20		ns
t_{SCP}	$SCLK_{IN}$ Width	40		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	0.25 t_{CK}	0.25 t_{CK} + 20	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		30	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		30	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{SCDD}	SCLK High to DT Disable		30	ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		25	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		30	ns

Specifications subject to change without notice.

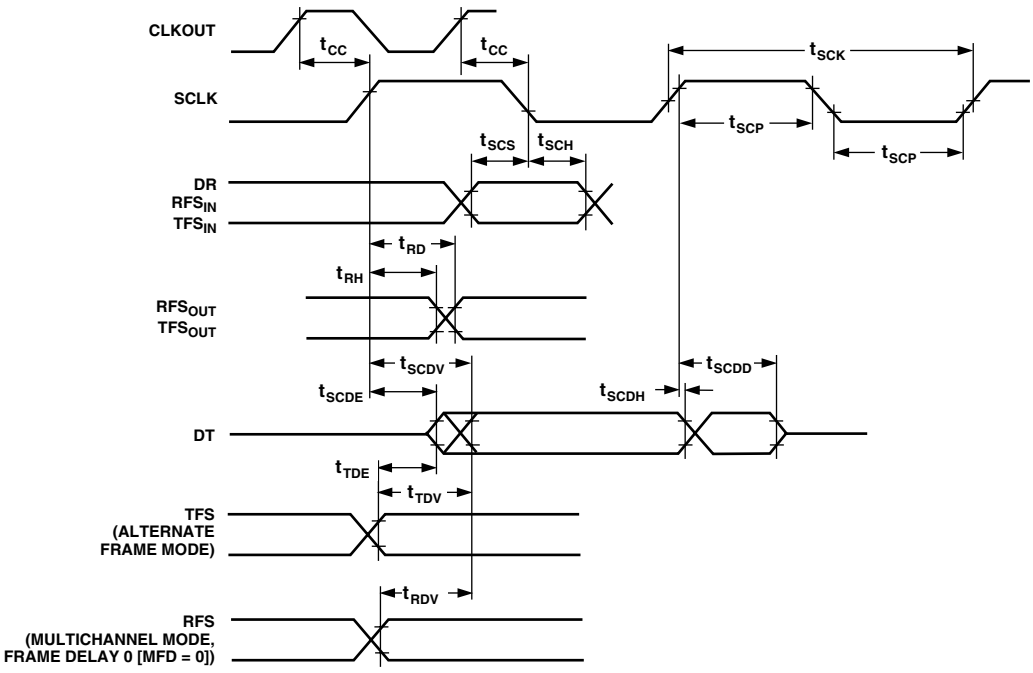


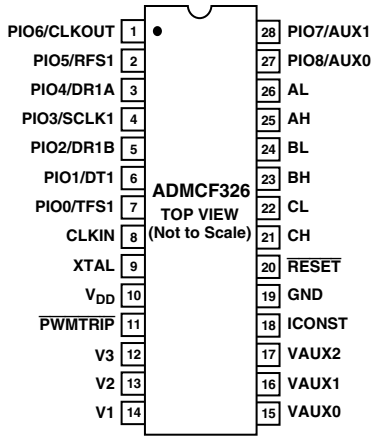
Figure 2. Serial Port Timing

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) . . . . . –0.3 V to +7.0 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Flash Memory Erase or Program
Temperature Range (Ambient) . . . . . 0°C to 85°C
Operating Temperature Range (Ambient) . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) . . . . . 280°C
Storage Temperature Range for SOIC Package . . –65°C to +150°C
Storage Temperature Range for PDIP Package . . –40°C to +125°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Name	Pin Type
1	PIO6/CLKOUT	I/O
2	PIO5/RFS1	I/O
3	PIO4/DR1A	I/O
4	PIO3/SCLK1	I/O
5	PIO2/DR1B	I/O
6	PIO1/DT1	I/O
7	PIO0/TFS1	I/O
8	CLKIN	I
9	XTAL	O
10	V_{DD}	SUP
11	$\overline{\text{PWMTRIP}}$	I
12	V3	I
13	V2	I
14	V1	I
15	VAUX0	I
16	VAUX1	I
17	VAUX2	I
18	ICONST	O
19	GND	GND
20	$\overline{\text{RESET}}$	I
21	CH	O
22	CL	O
23	BH	O
24	BL	O
25	AH	O
26	AL	O
27	PIO8/AUX0	I/O
28	PIO7/AUX1	I/O

ORDERING GUIDE

Model	Temperature Range	Instruction Rate	Package Description	Package Option
ADMCF326BR	–40°C to +85°C	20 MHz	28-Lead Wide Body (SOIC)	SO-28
ADMCF326BN	–40°C to +85°C	20 MHz	28-Lead PDIP	N-28
ADMCF326-EVALKIT			Development Tool Kit	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADMCF326 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

GENERAL DESCRIPTION

The ADMCF326 is a low cost, single-chip DSP-based controller, suitable for permanent magnet synchronous motors, ac induction motors, and brushless dc motors. The ADMCF326 integrates a 20 MIPS, fixed-point DSP core with a complete set of motor control and system peripherals that permits fast, efficient development of motor controllers.

The DSP core of the ADMCF326 is the ADSP-2171, which is completely code-compatible with the ADSP-21xx DSP family and combines three computational units, data address generators and a program sequencer. The computational units comprise an ALU, a multiplier/accumulator (MAC), and a barrel shifter. The ADSP-2171 adds new instructions for bit manipulation, multiplication (× squared), biased rounding, and global interrupt masking.

The system peripherals are the power-on reset circuit (POR), the watchdog timer and a synchronous serial port. The serial port is configurable and double buffered, with hardware support for UART and SCI port emulation.

The ADMCF326 provides 512 × 24-bit program memory RAM, 4K × 24-bit program memory ROM, 4K × 24-bit program FLASH memory, and 512 × 16-bit data memory RAM. The user code will be stored and executed from the flash memory. The program and data memory RAM can be used for dynamic data storage or can be loaded through the serial port from an external device as in other ADMCxxx family parts. The program memory ROM contains a monitor function as well as useful routines for erasing, programming, and verifying the flash memory.

The motor control peripherals of the ADMCF326 provide a 12-bit analog data acquisition system with six analog input channels, and an internal voltage reference. In addition, a three-phase, 16-bit, center-based PWM generation unit can be used to produce high accuracy PWM signals with minimal processor overhead. The ADMCF326 also contains two auxiliary PWM outputs and nine lines of digital I/O.

Because the ADMCF326 has a limited number of pins, functions such as the auxiliary PWM and the serial communication port are multiplexed with the nine programmable input/output (PIO) pins. The pin functions can be independently selected to allow maximum flexibility for different applications.

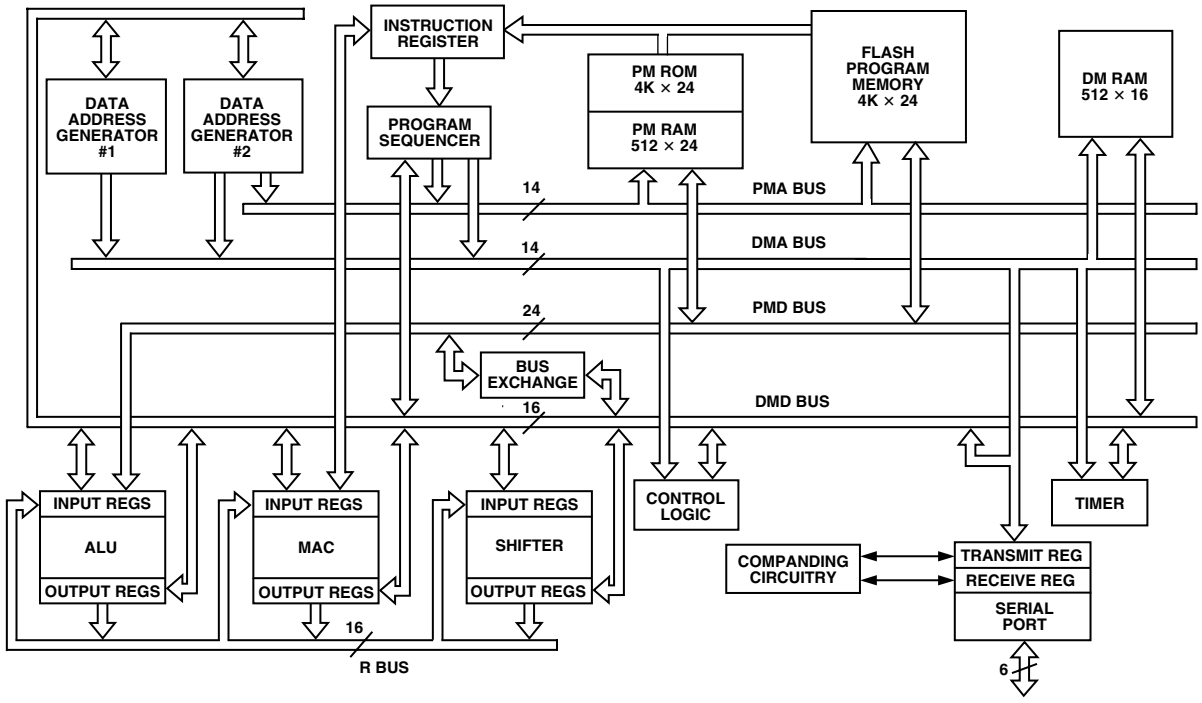


Figure 3. DSP Core Block Diagram

DSP CORE ARCHITECTURE OVERVIEW

Figure 3 is an overall block diagram of the DSP core of the ADMCF326, which is based on the fixed-point ADSP-2171. The flexible architecture and comprehensive instruction set of the ADSP-2171 allow the processor to perform multiple operations in parallel. In one processor cycle (50 ns with a 10 MHz CLKIN), the DSP core can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This all takes place while the processor continues to:

- Receive and transmit through the serial port
- Decrement the interval timer
- Generate three-phase PWM waveforms for a power inverter
- Generate two signals using the 8-bit auxiliary PWM timers
- Acquire four analog signals
- Decrement the watchdog timer

The processor contains three independent computational units: the arithmetic and logic unit (ALU), the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations as well as provides support for division primitives. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive-exponent operations. The shifter can be used to efficiently implement numeric format control, including floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps and subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADMCF326 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from data memory and program memory. Each DAG maintains and updates four address pointers (I registers). Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value in one of four modify (M registers). A length value may be associated with each pointer (L registers) to implement automatic modulo addressing for circular buffers. The circular buffering feature is also used by the serial ports for automatic data transfers to and from on-chip memory. DAG1 generates only data memory addresses and provides an optional bit-reversal capability. DAG2 may generate either program or data memory addresses but has no bit-reversal capability.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

Program Memory on the ADMCF326 can either be internal (on-chip RAM) or external (Flash). Internal program memory can store both instructions and data, permitting the ADMCF326 to fetch two operands in a single instruction cycle—one from program memory and one from data memory. Operation from external program memory is described in detail in the *ADSP-2100 Family User's Manual,* Third Edition.

The ADMCF326 writes data from its 16-bit registers to the 24-bit program memory using the PX Register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX Register.

The ADMCF326 can respond to a number of distinct DSP core and peripheral interrupts. The DSP interrupts comprise a serial port receive interrupt, a serial port transmit interrupt, a timer interrupt, and two software interrupts. Additionally, the motor control peripherals include two PWM interrupts and a PIO interrupt.

The serial port (SPORT1) provides a complete synchronous serial interface with optional companding in hardware, and a wide variety of framed and unframed data transmit and receive modes of operation. SPORT1 can generate an internal programmable serial clock or accept an external serial clock.

A programmable interval counter is also included in the DSP core and can be used to generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycles, where n–1 is a scaling value stored in the 8-bit TSCALE register. When the value of the counter reaches zero, an interrupt is generated, and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADMCF326 instruction set provides flexible data moves and multifunction instructions (one or two data moves within a computation) that will execute from internal program memory RAM. The ADMCF326 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development. For further information on the DSP core, refer to the *ADSP-2100 Family User's Manual,* Third Edition, with particular reference to the ADSP-2171.

Serial Port

The ADMCF326 incorporates a complete synchronous serial port (SPORT1) for serial communication and multiprocessor communication. The following is a brief list of capabilities of the ADMCF326 SPORT1. Refer to the *ADSP-2100 Family User's Manual,* Third Edition, for further details.

- SPORT1 is bidirectional and has a separate, double-buffered transmit and receive section.
- SPORT1 can use an external serial clock or generate its own serial clock internally.
- SPORT1 has independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame synchronization signals are active high or inverted, with either of two pulsewidths and timings.
- SPORT1 supports serial data-word lengths from three bits to 16 bits and provides optional A-law and μ-law companding according to ITU (formerly CCITT) recommendation G.711.
- SPORT1 receive and transmit sections can generate unique interrupts on completing a data-word transfer.
- SPORT1 can receive and transmit an entire circular buffer of data with only one overhead cycle per data-word. An interrupt is generated after a data buffer transfer.
- SPORT1 can be configured to have two external interrupts (IRQ0 and IRQ1), and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.
- SPORT1 has two data receive pins (DR1A and DR1B), which are internally multiplexed onto the one DR1 port of the SPORT1. The particular data receive pin selected is determined by a bit in the MODECTRL register.

PIN FUNCTION DESCRIPTION

The ADMCF326 is available in both 28-lead SOIC and PDIP packages. Table I describes the pins.

Table I. Pin List

Pin Group Name	No. of Pins	Input/ Output	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
SPORT1*	6	I/O	Serial Port 1 Pins (TFS1, RFS1, DT1, DR1A, DR1B, SCLK1)
CLKOUT*	1	O	Processor Clock Output
CLKIN, XTAL	2	I, O	External Clock or Quartz Crystal Connection Point
PIO0–PIO8*	9	I/O	Digital I/O Port Pins
AUX0–AUX1*	2	O	Auxiliary PWM Outputs
AH–CL	6	O	PWM Outputs
$\overline{\text{PWMTRIP}}$	1	I	PWM Trip Signal
V1, V2, V3	3	I	Analog Inputs
VAUX0–VAUX2	3	I	Auxiliary Analog Input
ICONST	1	O	ADC Constant Current Source
V_{DD}	1		Power Supply
GND	1		Ground

*Multiplexed pins, individually selectable through PIOSELECT and PIODATA1 Registers.

INTERRUPT OVERVIEW

The ADMCF326 can respond to 16 different interrupt sources with minimal overhead, five of which are internal DSP core interrupts and 11 are from the motor control peripherals. The five DSP core interrupts are SPORT1 receive (or $\overline{\text{IRQ0}}$) and transmit (or $\overline{\text{IRQ1}}$), the internal timer, and two software interrupts. The motor control peripheral interrupts are the nine programmable I/Os and two from the PWM (PWMSYNC pulse and $\overline{\text{PWMTRIP}}$). All motor control interrupts are multiplexed into the DSP core through the peripheral $\overline{\text{IRQ2}}$ interrupt. The interrupts are internally prioritized and individually maskable. A detailed description of the entire interrupt system of the ADMCF326 is presented later, following a more detailed description of each peripheral block.

MEMORY MAP

The ADMCF326 has two distinct memory types: program memory and data memory. In general, program memory contains user code and coefficients, while the data memory is used to store variables and data during program execution. Three kinds of program memory are provided on the ADMCF326: RAM, ROM, and flash memory. The motor control peripherals are memory mapped into a region of the data memory space starting at 0x2000. The complete program and data memory maps are given in Tables II and III, respectively.

Table II. Program Memory Map

Address Range	Memory Type	Function
0x0000–0x002F	RAM	Internal Vector Table
0x0030–0x01FF	RAM	User Program Memory
0x0200–0x07FF		Reserved
0x0800–0x17FF	ROM	Reserved Program Memory
0x1800–0x1FFF		Reserved
0x2000–0x20FF	FLASH	User Program Memory Sector 0
0x2100–0x21FF	FLASH	User Program Memory Sector 1
0x2200–0x2FFF	FLASH	User Program Memory Sector 2
0x3000–0x3FFF		Reserved

Table III. Data Memory Map

Address Range	Memory Type	Function
0x0000–0x1FFF		Reserved
0x2000–0x20FF		Memory Mapped Registers
0x2100–0x37FF		Reserved
0x3800–0x39FF	RAM	User Data Memory
0x3A00–0x3BFF	RAM	Reserved
0x3C00–0x3FFF		Memory Mapped Registers

FLASH MEMORY SUBSYSTEM

The ADMCF326 has 4K × 24-bit of user-programmable, nonvolatile flash memory. A flash programming utility is provided with the development tools, which performs the basic device programming operations: erase, program, and verify.

The flash memory array is partitioned into three asymmetrically sized sectors of 256 words, 256 words, and 3584 words, labeled Sector 0, Sector 1, and Sector 2, respectively. These sectors are mapped into external program memory address space.

Four flash memory interface registers are connected to the DSP. These 16-bit registers are mapped into the register area of data memory space. They are named Flash Memory Control Register (FMCR), Flash Memory Address Register (FMAR), Flash Memory Data Register Low (FMDRL), and Flash Memory Data Register High (FMDRH). These registers are diagrammed later in this data sheet. They are used by the flash memory programming utility. The user program may read these registers, but should not modify them directly. The flash programming utility provides a complete interface to the flash memory.

Special Flash Registers

The flash module has four nonvolatile 8-bit registers called Special Flash Registers (SFRs) that are accessible independently of the main flash array via the flash programming utility. These registers are for general-purpose, nonvolatile storage. When erased, the Special Flash Registers contain all 0s. To read Special Flash Registers from the user program, call the read_reg routine contained in ROM. Refer to the *ADMCF32x DSP Motor Controller Developer's Reference Manual* for an example.

Boot-from-Flash Code

A security feature is available in the form of a code that, when set, causes the processor to execute the program in flash memory upon power-up or reset. In this mode, the flash programming utility and debugger are unable to communicate with the ADMCF326. Consequently, the contents of the flash memory can neither be programmed nor read.

The boot-from-flash code may be set via the flash programming utility, when the user's program is thoroughly tested and loaded into flash program memory at address 0x2200. The user's program must contain a mechanism for clearing the boot-from-flash code if reprogramming the flash memory is desired. The only way to clear boot-from-flash is from within the user program, by calling the flash_init or auto_erase_reg routines that are included in the ROM. The user program must be signaled in some way to call the necessary routine to clear the boot-from-flash code. An example would be to detect a high level on a PIO pin during start-up initialization and then call the flash_init or auto_erase_routine. The flash_init routine will erase the entire user program in flash memory before clearing the boot-from-flash code, thus ensuring the security of the user program. If security is not a concern, the auto_erase_reg routine can be used to clear the boot-from-flash code while leaving the user program intact.

Refer to the *ADMCF32x DSP Motor Controller Developer's Reference Manual* for further instructions and an example of using the boot-from-flash code.

FLASH PROGRAM BOOT SEQUENCE

On power-up or reset, the processor begins instruction execution at address 0x0800 of internal program ROM. The ROM monitor program that is located there checks the boot-from-flash code. If that code is set, the processor jumps to location 0x2200 in external flash program memory, where it expects to find the user's application program.

If the boot-from-flash code is not set, the monitor attempts to boot from an external device as described in the *ADMCF32x DSP Motor Controller Developer's Reference Manual*

SYSTEM INTERFACE

Figure 4 shows a basic system configuration for the ADMCF326 with an external crystal.

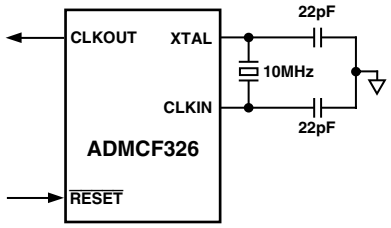


Figure 4. Basic System Configuration

Clock Signals

The ADMCF326 can be clocked either by a crystal or a TTL-compatible clock signal. For normal operation, the CLKIN input cannot be halted, changed during operation, or operated below the specified minimum frequency. If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the CLKIN pin of the ADMCF326. In this mode, with an external clock signal, the XTAL pin must be left unconnected. The ADMCF326 uses an input clock with a frequency equal to half the instruction rate; a 10 MHz input clock yields a 50 ns processor cycle (which is equivalent to 20 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction rate, which is indicated by the CLKOUT signal when enabled.

Because the ADMCF326 includes an on-chip oscillator feedback circuit, an external crystal may be used instead of a clock source, as shown in Figure 4. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors as shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used. A clock output signal (CLKOUT) is generated by the processor at the processor's cycle rate of twice the input frequency.

Reset

The ADMCF326 DSP core and peripherals must be correctly reset when the device is powered up to assure proper initialization. The ADMCF326 contains an integrated power-on reset (POR) circuit that provides a complete system reset on power-up and power-down. The POR circuit monitors the voltage on the ADMCF326 V_{DD} pin and holds the DSP core and peripherals in reset while V_{DD} is less than the threshold voltage level, V_{RST}. When this voltage is exceeded, the ADMCF326 is held in reset for an additional 2^{16} DSP clock cycles (t_{RST} in Figure 5). On power-down, when the voltage on the V_{DD} pin falls below $V_{RST}–V_{HYST}$, the ADMCF326 will be reset. Also, if the external $\overline{\text{RESET}}$ pin is actively pulled low at any time after power-up, a complete hardware reset of the ADMCF326 is initiated.

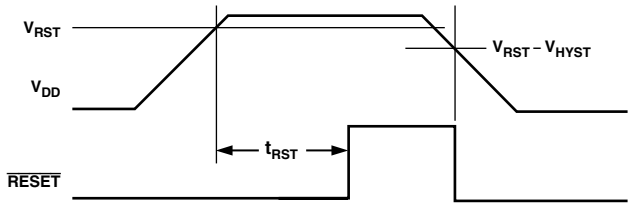


Figure 5. Power-On Reset Operation

The ADMCF326 reset sets all internal stack pointers to the empty stack condition, masks all interrupts, clears the MSTAT Register and performs a full reset of all of the motor control peripherals. Following a power-up, it is possible to initiate a DSP core and motor control peripheral reset by pulling the $\overline{RESET}$ pin low. The $\overline{RESET}$ signal must meet the minimum pulsewidth specification, t_{RSP}. Following the reset sequence, the DSP core starts executing code from the internal PM ROM located at 0x0800.

DSP Control Registers

The DSP core has a system control register, SYSCNTL, memory mapped at DM (0x3FFF). SPORT1 is configured as a serial port when Bit 10 is set, or as flags and interrupt lines when this bit is cleared. For proper operation of the ADMCF326, all other bits in this register must be cleared.

The DSP core has a wait state control register, MEMWAIT, memory mapped at DM (0x3FFE). The default value of this resister is 0xFFFF. For proper operation of the ADMCF326, this register must always contain the value 0x8000.

The configuration of both the SYSCNTL and MEMWAIT Registers of the ADMCF326 are shown at the end of the data sheet.

THREE-PHASE PWM CONTROLLER

Overview

The PWM generator block of the ADMCF326 is a flexible, programmable, three-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a three-phase voltage source inverter for ac induction motors (ACIM) or permanent magnet synchronous motors (PMSM). In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of electronically commutated motors (ECM) or brushless dc motors (BDCM).

The PWM generator produces three pairs of active high PWM signals on the six PWM output pins (AH, AL, BH, BL, CH, and CL). The six PWM output signals consist of three high side drive signals (AH, BH, and CH) and three low side drive signals (AL, BL, and CL). The switching frequency, dead time, and minimum pulsewidths of the generated PWM patterns are programmable using, respectively, the PWMTM, PWMDT, and PWMPD Registers. In addition, three registers (PWMCHA, PWMCHB, and PWMCHC) control the duty cycles of the three pairs of PWM signals.

Each of the six PWM output signals can be enabled or disabled by separate output enable bits of the PWMSEG Register. In addition, three control bits of the PWMSEG register permit crossover of the two signals of a PWM pair for easy control of ECM or BDCM. In crossover mode, the PWM signal destined for the high side switch is diverted to the complementary low side output, and the signal destined for the low side switch is diverted to the corresponding high side output signal.

In many applications, there is a need to provide an isolation barrier in the gate-drive circuits that turn on the power devices of the inverter. In general, there are two common isolation techniques: optical isolation using optocouplers, and transformer isolation using pulse transformers. The PWM controller of the ADMCF326 permits mixing of the output PWM signals with a high frequency chopping signal to permit an easy interface to such pulse transformers. The features of this gate-drive chopping mode can be controlled by the PWMGATE Register. There is an 8-bit value within the PWMGATE Register that directly controls the chopping frequency. In addition, high frequency chopping can be independently enabled for the high side and the low side outputs using separate control bits in the PWMGATE Register.

The PWM generator is capable of operating in two distinct modes: Single Update Mode or Double Update Mode. In Single Update mode, the duty cycle values are programmable only once per PWM period, so that the resultant PWM patterns are symmetrical about the midpoint of the PWM period. In the Double Update Mode, a second updating of the PWM duty cycle values is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters. This technique also permits the closed-loop controller to change the average voltage applied to the machine winding at a faster rate, allowing wider closed-loop bandwidths to be achieved. The operating mode of the PWM block (Single or Double Update Mode) is selected by a control bit in MODECTRL Register.

The PWM generator of the ADMCF326 also provides an internal signal that synchronizes the PWM switching frequency to the A/D operation. In Single Update Mode, a PWMSYNC pulse is produced at the start of each PWM period. In Double Update Mode, an additional PWMSYNC pulse is produced at the midpoint of each PWM period. The width of the PWMSYNC pulse is programmable through the PWMSYNCWT Register.

The PWM signals produced by the ADMCF326 can be shut off in a number of different ways. First, there is a dedicated asynchronous PWM shutdown pin, $\overline{PWMTRIP}$, which, when brought LO, instantaneously places all six PWM outputs in the LO state. Because this hardware shutdown mechanism is asynchronous, and the associated PWM disable circuitry does not use clocked logic, the PWM will shut down even if the DSP clock is not running. The PWM system may also be shut down from software by writing to the PWMSWT Register.

Status information about the PWM system of the ADMCF326 is available to the user in the SYSSTAT Register. In particular, the state of $\overline{PWMTRIP}$ is available, as well as a status bit that indicates whether operation is in the first half or the second half of the PWM period.

A functional block diagram of the PWM controller is shown in Figure 6. The generation of the six output PWM signals on pins AH to CL is controlled by four important blocks:

- The three-phase PWM timing unit, which is the core of the PWM controller, generates three pairs of complemented and dead-time-adjusted center-based PWM signals.
- The output control unit allows the redirection of the outputs of the three-phase timing unit for each channel to either the high side or low side output. In addition, the output control unit allows individual enabling/disabling of each of the six PWM output signals.
- The GATE drive unit provides the high chopping frequency and its subsequent mixing with the PWM signals.
- The PWM shutdown controller manages the two PWM shutdown modes (via the $\overline{\text{PWMTRIP}}$ pin, and the PWMSWT Register) and generates the correct $\overline{\text{RESET}}$ signal for the Timing Unit.
- The PWM controller is driven by a clock at the same frequency as the DSP instruction rate, CLKOUT, and is capable of generating two interrupts to the DSP core. One interrupt is generated on the occurrence of a PWMSYNC pulse, and the other is generated on the occurrence of any PWM shutdown action.

Three-Phase Timing Unit

The 16-bit three-phase timing unit is the core of the PWM controller and produces three pairs of pulsewidth modulated signals with high resolution and minimal processor overhead. There are four main configuration registers (PWMTM, PWMDT, PWMPD, and PWMSYNCWT) that determine the fundamental characteristics of the PWM outputs. In addition, the operating mode of the PWM (Single or Double Update Mode) is selected by Bit 6 of the MODECTRL Register. These registers, in conjunction with the three 16-bit duty cycle registers (PWMCHA, PWMCHB, and PWMCHC), control the output of the three-phase timing unit.

PWM Switching Frequency: PWMTM Register

The PWM switching frequency is controlled by the PWM period register, PWMTM. The fundamental timing unit of the PWM controller is $t_{CK} = 1/f_{CLKOUT,}$ where $f_{CLKOUT,}$ is the CLKOUT frequency (DSP instruction rate). Therefore, for a 20 MHz CLKOUT, the fundamental time increment is 50 ns. The value written to the PWMTM Register is effectively the number of t_{CK} clock increments in half a PWM period. The required PWMTM value is a function of the desired PWM switching frequency (f_{PWM}) and is given by:

$$PWMTM = \frac{f_{CLKOUT}}{2 \times f_{PWM}} = \frac{f_{CLKIN}}{f_{PWM}}$$

Therefore, the *PWM* switching period, T_S, can be written as:

$$T_S = 2 \times PWMTM \times t_{CK}$$

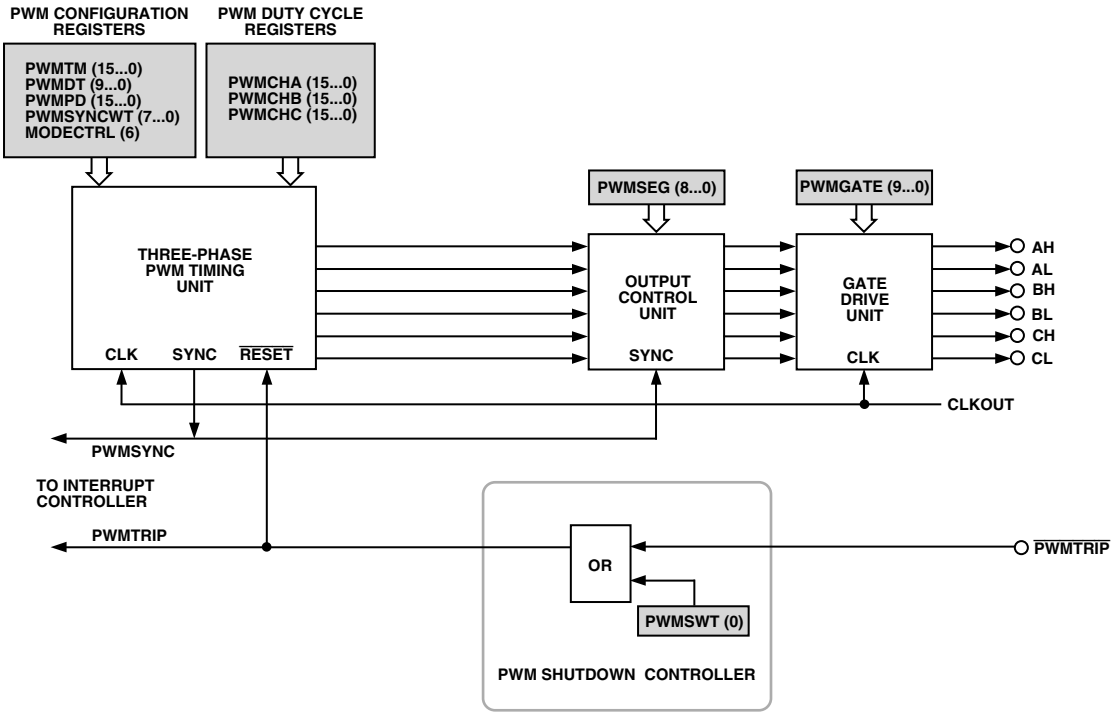


Figure 6. Overview of the PWM Controller of the ADMCF326

For example, for a 20 MHz CLKOUT and a desired PWM switching frequency of 10 kHz (T_S = 100 μs), the correct value to load into the PWMTM Register is:

$$PWMTM = \frac{20 \times 10^6}{2 \times 10 \times 10^3} 1000 = 0x3E8$$

The largest value that can be written to the 16-bit PWMTM Register is 0xFFFF = 65,535, which corresponds to a minimum PWM switching frequency of:

$$f_{PWM,\min} = \frac{20 \times 10^6}{2 \times 65,535} = 153\ Hz$$

for a CLKOUT frequency of 20 MHz.

PWM Switching Dead Time: PWMDT Register

The second important PWM block parameter that must be initialized is the switching dead time. This is a short delay time introduced between turning off one PWM signal (for example AH) and turning on its complementary signal (AL). This short time delay is introduced to permit the power switch being turned off to completely recover its blocking capability before the complementary switch is turned on. This time delay prevents a potentially destructive short circuit condition from developing across the dc link capacitor of a typical voltage source inverter.

Dead time is controlled by the PWMDT Register. The dead time is inserted into the three pairs of PWM output signals. The dead time, T_D, is related to the value in the PWMDT Register by:

$$T_D = PWMDT \times 2 \times t_{CK} = 2 \times \frac{PWMDT}{f_{CLKOUT}}$$

Therefore, a *PWMDT* value of 0x00A (= 10), introduces a 1 μs delay between the turn-off of any PWM signal (for example AH) and the turn-on of its complementary signal (AL). The amount of the dead time can therefore be programmed in increments of 2 t_{CK} (or 100 ns for a 20 MHz CLKOUT). The PWMDT Register is a 10-bit Register. For a CLKOUT rate of 20 MHz, its maximum value of 0x3FF (= 1023) corresponds to a maximum programmed dead time of:

$$\begin{aligned} T_{Dmax} &= 1023 \times 2 \times t_{CK} \\ &= 1023 \times 2 \times 50 \times 10^{-9}\ sec \\ &= 102\ \mu s \end{aligned}$$

The dead time can be programmed to zero by writing 0 to the PWMDT Register.

PWM Operating Mode: MODECTRL and SYSSTAT Registers

The PWM controller of the ADMCF326 can operate in two distinct modes: Single Update Mode and Double Update Mode. The operating mode of the PWM controller is determined by the state of Bit 6 of the MODECTRL Register. If this bit is cleared, the PWM operates in the Single Update Mode. Setting Bit 6 places the PWM in the Double Update Mode. By default, following either a peripheral reset or power-on, Bit 6 of the MODECTRL Register is cleared. This means that the default operating mode is Single Update Mode.

In Single Update Mode, a single PWMSYNC pulse is produced in each PWM period. The rising edge of this signal marks the start of a new PWM cycle and is used to latch new values from the PWM configuration registers (PWMTM, PWMDT, PWMPD, and PWMSYNCWT) and the PWM duty cycle registers (PWMCHA, PWMCHB, and PWMCHC) into the three-phase timing unit. The PWMSEG Register is also latched into the output control unit on the rising edge of the PWMSYNC pulse. In effect, this means that the parameters of the PWM signals can be updated only once per PWM period at the start of each cycle. Thus, the generated PWM patterns are symmetrical about the midpoint of the switching period.

In Double Update Mode, there is an additional PWMSYNC pulse produced at the midpoint of each PWM period. The rising edge of this new PWMSYNC pulse is again used to latch new values of the PWM configuration Registers, duty cycle registers, and the PWMSEG Register. As a result, it is possible to alter both the characteristics (switching frequency, dead time, minimum pulsewidth and PWMSYNC pulsewidth) and the output duty cycles at the midpoint of each PWM cycle. Consequently, it is possible to produce PWM switching patterns that are no longer symmetrical about the midpoint of the period (asymmetrical PWM patterns).

In the Double Update Mode, operation in the first half or the second half of the PWM cycle is indicated by Bit 3 of the SYSSTAT Register. In Double Update Mode, this bit is cleared during operation in the first half of each PWM period (between the rising edge of the original PWMSYNC pulse and the rising edge of the new PWMSYNC pulse, which is introduced in Double Update Mode). Bit 3 of the SYSSTAT Register is set during the second half of each PWM period. If required, a user may determine the status of this bit during a PWMSYNC interrupt service routine.

The advantages of the Double Update Mode are that lower harmonic voltages can be produced by the PWM process and wider control bandwidths are possible. However, for a given PWM switching frequency, the PWMSYNC pulses occur at twice the rate in the Double Update Mode. Because new duty cycle values must be computed in each PWMSYNC interrupt service routine, there is a larger computational burden on the DSP in the Double Update Mode.

Width of the PWMSYNC Pulse: PWMSYNCWT Register

The PWM controller of the ADMCF326 produces an internal PWM synchronization pulse at a rate equal to the PWM switching frequency in Single Update Mode, and at twice the PWM frequency in the Double Update Mode. This PWMSYNC synchronizes the operation of the PWM unit with the A/D converter system. The width of this PWMSYNC pulse is programmable by the PWMSYNCWT Register. The width of the PWMSYNC pulse, $T_{PWMSYNC}$, is given by:

$$T_{PWMSYNC} = t_{CK} \times \left(PWMSYNCWT + 1\right)$$

which means that the width of the pulse is programmable from t_{CK} to 256 t_{CK} (corresponding to 50 ns to 12.8 μs for a CLKOUT rate of 20 MHz). Following a reset, the PWMSYNCWT Register contains 0x27 (= 39) so that the default PWMSYNC width is 2.0 μs.

PWM Duty Cycles: PWMCHA, PWMCHB, PWMCHC Registers

The duty cycles of the six PWM output signals are controlled by the three duty cycle registers, PWMCHA, PWMCHB, and PWMCHC. The integer value in the register PWMCHA controls the duty cycle of the signals on AH and AL. PWMCHB controls the duty cycle of the signals on BH and BL, and PWMCHC controls the duty cycle of the signals on CH and CL. The duty cycle registers are programmed in integer counts of the fundamental time unit, t_{CK}, and define the desired on-time of the high side PWM signal produced by the three-phase timing unit

over half the PWM period. The switching signals produced by the three-phase timing unit are also adjusted to incorporate the programmed dead time value in the PWMDT Register.

The PWM is center-based. This means that in Single Update Mode the resulting output waveforms are symmetrical and centered in the PWMSYNC period. Figure 7 presents a typical PWM timing diagram illustrating the PWM-related registers' (PWMCHA, PWMTM, PWMDT, and PWMSYNCWT) control over the waveform timing in both half cycles of the PWM period. The magnitude of each parameter in the timing diagram is determined by multiplying the integer value in each register by t_{CK} (typically 50 ns). It may be seen in the timing diagram how dead time is incorporated into the waveforms by moving the switching edges away from the instants set by the PWMCHA Register.

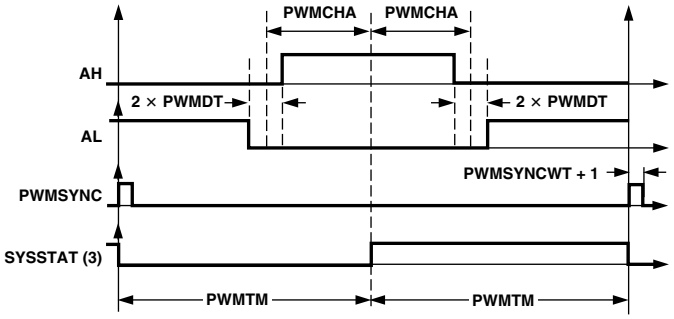


Figure 7. Typical PWM Outputs of Three-Phase Timing Unit in Single Update Mode

Each switching edge is moved by an equal amount (PWMDT $\times t_{CK}$) to preserve the symmetrical output patterns. The PWMSYNC pulse, whose width is set by the PWMSYNCWT Register, is also shown. Bit 3 of the SYSSTAT Register indicates which half cycle is active. This can be useful in Double Update Mode, as will be discussed later.

The resultant on-times of the PWM signals shown in Figure 7 may be written as:

$$T_{AH} = 2 \times (PWMCHA - PWMDT) \times t_{CK}$$

$$T_{AL} = 2 \times (PWMTM - PWMCHA - PWMDT) \times t_{CK}$$

The corresponding duty cycles are:

$$d_{AH} = \frac{T_{AH}}{T_S} = \frac{PWMCHA - PWMDT}{PWMTM}$$

$$d_{AL} = \frac{T_{AL}}{T_S} = \frac{PWMTM - PWMCHA - PWMDT}{PWMTM}$$

Obviously, negative values of T_{AH} and T_{AL} are not permitted because the minimum permissible value is zero, corresponding to a 0% duty cycle. In a similar fashion, the maximum value is T_S, corresponding to a 100% duty cycle.

The output signals from the timing unit for operation in Double Update Mode are shown in Figure 8. This illustrates a completely general case where the switching frequency, dead time, and duty cycle are all changed in the second half of the PWM period. Of course, the same value for any or all of these quantities could be used in both halves of the PWM cycle. However, it can be seen that there is no guarantee that symmetrical PWM signals will be produced by the timing unit in this Double Update Mode.

Additionally, it is seen that the dead time is inserted into the PWM signals in the same way as in the Single Update Mode.

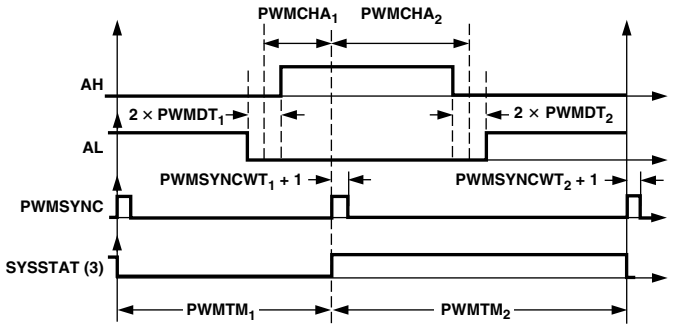


Figure 8. Typical PWM Outputs of Three-Phase Timing Unit in Double Update Mode

In general, the on-times of the PWM signals in Double Update Mode are defined by:

$$T_{AH} = \left(PWMCHA_1 + PWMCHA_2 - PWMDT_1 - PWMDT_2\right) \times t_{CK}$$

$$T_{AL} = \begin{pmatrix} PWMTM_1 + PWMTM_2 - PWMCHA_1 - \\ PWMCHA_2 - PWMDT_1 - PWMDT_2 \end{pmatrix} \times t_{CK}$$

where the subscript 1 refers to the value of that register during the first half cycle and the subscript 2 refers to the value during the second half cycle. The corresponding duty cycles are:

$$d_{AH} = \frac{T_{AH}}{T_S}$$

$$= \frac{PWMCHA_1 + PWMCHA_2}{PWMTM_1 + PWMTM_2}$$

$$- \frac{PWMDT_1 + PWMDT_2}{PWMTM_1 + PWMTM_2}$$

$$d_{AL} = \frac{T_{AL}}{T_S}$$

$$= \frac{\left(PWMTM_1 + PWMTM_2 + PWMCHA_1\right)}{PWMTM_1 + PWMTM_2}$$

$$- \frac{\left(PWMCHA_2 + PWMDT_1 + PWMDT_2\right)}{PWMTM_1 + PWMTM_2}$$

because for the completely general case in Double Update Mode, the switching period is given by:

$$T_S = \left(PWMTM_1 + PWMTM_2\right) \times t_{CK}$$

Again, the values of T_{AH} and T_{AL} are constrained to lie between zero and T_S.

PWM signals similar to those illustrated in Figure 7 and Figure 8 can be produced on the BH, BL, CH, and CL outputs by programming the PWMCHB and PWMCHC Registers in a manner identical to that described for PWMCHA.

The PWM controller does not produce any PWM outputs until all of the PWMTM, PWMCHA, PWMCHB, and PWMCHC Registers have been written to at least once. After these registers have been written, the counters in the three-phase timing unit

are enabled. Writing to these registers also starts the main PWM timer. If during initialization, the PWMTM Register is written before the PWMCHA, PWMCHB, and PWMCHC Registers, the first PWMSYNC pulse (and interrupt if enabled) will be generated ($1.5 \times t_{CK} \times$ PWMTM) seconds after the initial write to the PWMTM Register in Single Update Mode. In Double Update Mode, the first PWMSYNC pulse will be generated ($t_{CK} \times$ PWMTM) seconds after the initial write to the PWMTM Register in Single Update Mode.

Effective PWM Resolution

In Single Update Mode, the same values of PWMCHA, PWMCHB, and PWMCHC are used to define the on-times in both half cycles of the PWM period. As a result, the effective resolution of the PWM generation process is 2 t_{CK} (or 100 ns for a 20 MHz CLKOUT) since incrementing one of the duty cycle registers by one changes the resultant on-time of the associated PWM signals by t_{CK} in each half period (or 2 t_{CK} for the full period).

In Double Update Mode, improved resolution is possible since different values of the duty cycle registers are used to define the on-times in both the first and second halves of the PWM period. As a result, it is possible to adjust the on-time over the whole period in increments of t_{CK}. This corresponds to an effective PWM resolution of t_{CK} in Double Update Mode (or 50 ns for a 20 MHz CLKOUT).

The achievable PWM switching frequency at a given PWM resolution is tabulated in Table IV.

Table IV. Achievable PWM Resolution in Single and Double Update Modes

Resolution (Bit)	Single Update Mode PWM Frequency (kHz)	Double Update Mode PWM Frequency (kHz)
8	39.1	78.1
9	19.5	39.1
10	9.8	19.5
11	4.9	9.8
12	2.4	4.9

Minimum Pulsewidth: PWMPD Register

In many power converter switching applications, it is desirable to eliminate PWM switching pulses shorter than a certain width. It takes a finite time to both turn on and turn off modern power semiconductor devices. Therefore, if the width of any of the PWM pulses is shorter than some minimum value, it may be desirable to completely eliminate the PWM switching for that particular cycle.

The allowable minimum on-time for any of the six PWM outputs for half a PWM period that can be produced by the PWM controller may be programmed using the PWMPD register. The minimum on-time is programmed in increments of t_{CK} so that the minimum on-time produced for any half PWM period, T_{MIN}, is related to the value in the PWMPD Register by:

$$T_{MIN} = PWMPD \times t_{CK}$$

A *PWMPD* value of 0x002 defines a permissible minimum on-time of 100 ns for a 20 MHz CLKOUT.

In each half cycle of the PWM, the timing unit checks the on-time of each of the six PWM signals. If any of the times is found to be less than the value specified by the PWMPD Register, the corresponding PWM signal is turned OFF for the entire half period, and its complementary signal is turned completely ON.

Consider the example where PWMTM = 200, PWMCHA = 5, PWMDT = 3, and PWMPD = 10 with a CLKOUT of 20 MHz, while operating in single update mode. For this case, the PWM switching frequency is 50 kHz and the dead time is 300 ns. The minimum permissible on-time of any PWM signal over one-half of any period is 500 ns. Clearly, for this example, the dead-time adjusted on-time of the AH signal for one-half a PWM period is $(5–3) \times 50$ ns = 100 ns. Because this is less than the minimum permissible value, output AH of the timing unit will remain OFF (0% duty cycle). Additionally, the AL signal will be turned ON for the entire half period (100% duty cycle).

Output Control Unit: PWMSEG Register

The operation of the output control unit is managed by the 9-bit read/write PWMSEG Register. This register sets two distinct features of the output control unit that are directly useful in the control of ECM or BDCM.

The PWMSEG Register contains three crossover bits, one for each pair of PWM outputs. Setting Bit 8 of the PWMSEG Register enables the Crossover Mode for the AH/AL pair of PWM signals; setting Bit 7 enables crossover on the BH/BL pair of PWM signals; and setting Bit 6 enables crossover on the CH/CL pair of PWM signals. If Crossover Mode is enabled for any pair of PWM signals, the high side PWM signal from the timing unit (for example AH) is diverted to the associated low side output of the output control unit so that the signal will ultimately appear at the AL pin. Of course, the corresponding low side output of the timing unit is also diverted to the complementary high side output of the output control unit so that the signal appears at Pin AH. Following a reset, the three crossover bits are cleared so that the Crossover Mode is disabled on all three pairs of PWM signals.

The PWMSEG Register also contains six bits (Bits 0 to 5) that can be used to individually enable or disable each of the six PWM outputs. If the associated bit of the PWMSEG Register is set, the corresponding PWM output is disabled regardless of the value of the corresponding duty cycle register. This PWM output signal will remain in the OFF state as long as the corresponding enable/disable bit of the PWMSEG Register is set. The PWM output enable function gates the crossover function. After a reset, all six enable bits of the PWMSEG Register are cleared, thereby enabling all PWM outputs by default.

In a manner identical to the duty cycle registers, the PWMSEG is latched on the rising edge of the PWMSYNC signal so that changes to this register only become effective at the start of each PWM cycle in Single Update Mode. In Double Update Mode, the PWMSEG Register can also be updated at the midpoint of the PWM cycle.

In the control of an ECM, only two inverter legs are switched at any time, and often the high side device in one leg must be switched ON at the same time as the low side driver in a second leg. Therefore, by programming identical duty cycles for two PWM channels (for example, let PWMCHA = PWMCHB) and setting Bit 7 of the PWMSEG Register to crossover the BH/BL pair of PWM signals, it is possible to turn ON the high side switch of Phase A and the low side switch of Phase B at the

same time. In the control of an ECM, one inverter leg (Phase C in this example) is disabled for a number of PWM cycles. This disable may be implemented by disabling both the CH and CL PWM outputs by setting Bits 0 and 1 of the PWMSEG Register. This is illustrated in Figure 9, where it can be seen that both the AH and BL signals are identical, because PWMCHA = PWMCHB, and the crossover bit for Phase B is set. In addition, the other four signals (AL, BH, CH, and CL) have been disabled by setting the appropriate enable/disable bits of the PWMSEG Register. For the situation illustrated in Figure 9, the appropriate value for the PWMSEG Register is 0x00A7. In ECM operation, because each inverter leg is disabled for certain periods of time, the PWMSEG Register is changed based upon the position of the rotor shaft (motor commutation).

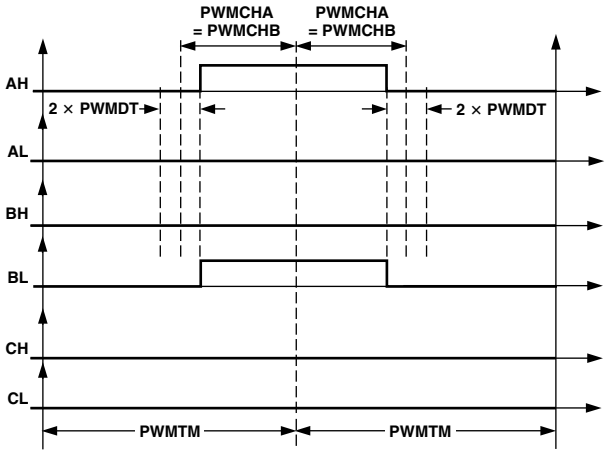


Figure 9. An example of PWM signals suitable for ECM control. PWMCHA = PWMCHB, BH/BL are a crossover pair. AL, BH, CH, and CL outputs are disabled. Operation is in Single Update Mode.

Gate Drive Unit: PWMGATE Register

The gate drive unit of the PWM controller adds features that simplify the design of isolated gate drive circuits for PWM inverters. If a transformer-coupled power device gate drive amplifier is used, the active PWM signal must be chopped at a high frequency. The PWMGATE Register allows the programming of this high frequency chopping mode. The chopped active PWM signals may be required for the high side drivers only, for the low side drivers only, or for both the high side and low side switches. Therefore, independent control of this mode for both high and low side switches is included with two separate control bits in the PWMGATE Register.

Typical PWM output signals with high frequency chopping enabled on both high side and low side signals are shown in Figure 10. Chopping of the high side PWM outputs (AH, BH, and CH) is enabled by setting Bit 8 of the PWMGATE Register. Chopping of the low side PWM outputs (AL, BL, and CL) is enabled by setting Bit 9 of the PWMGATE Register. The high chopping frequency is controlled by the 8-bit word (GDCLK) written to Bits 0 to 7 of the PWMGATE Register. The period and the frequency of this high frequency carrier are:

$$T_{CHOP} = \left[4 \times \left(GDCLK + 1\right)\right] \times t_{CK}$$

$$f_{CHOP} = \frac{f_{CLKOUT}}{\left[4 \times \left(GDCLK + 1\right)\right]}$$

The *GDCLK* value may range from 0 to 255, corresponding to a programmable chopping frequency rate from 19.5 kHz to 5 MHz for a 20 MHz CLKOUT rate. The gate drive features must be programmed before operation of the PWM controller and typically are not changed during normal operation of the PWM controller. Following a reset, by default, all bits of the PWMGATE Register are cleared so that high frequency chopping is disabled.

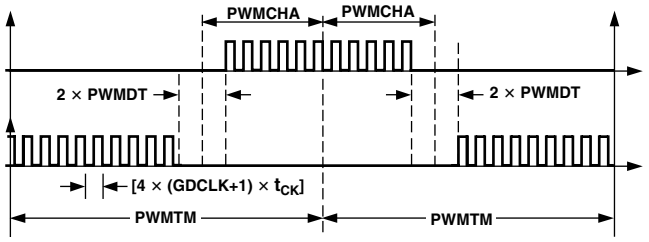


Figure 10. Typical PWM signals with high frequency gate chopping enabled on both high side and low side switches (GDCLK is the integer equivalent of the value in Bits 0 to 7 of the PWMGATE Register.)

PWM Shutdown

In the event of external fault conditions, it is essential that the PWM system be instantaneously shut down. Two methods of sensing a fault condition are provided by the ADMCF326. For the first method, a low level on the $\overline{\text{PWMTRIP}}$ pin initiates an instantaneous, asynchronous (independent of DSP clock) shutdown of the PWM controller. This places all six PWM outputs in the OFF state, disables the PWMSYNC pulse and associated interrupt signal, and generates a $\overline{\text{PWMTRIP}}$ interrupt signal. The $\overline{\text{PWMTRIP}}$ pin has an internal pull-down resistor so that even if the pin becomes disconnected, the PWM outputs will be disabled. The state of the $\overline{\text{PWMTRIP}}$ pin can be read from Bit 0 of the SYSSTAT Register.

It is possible through software to initiate a PWM shutdown by writing to the 1-bit read/write PWMSWT Register (0x2061). Writing to this bit generates a PWM shutdown in a manner identical to the $\overline{\text{PWMTRIP}}$ pin. Following a PWM shutdown, it is possible to determine if the shutdown was generated from hardware or software by reading the same PWMSWT Register. Reading this register also clears it.

Table V. Fundamental Characteristics of PWM Generation Unit of ADMCF326

16-BIT PWM TIMER

Parameter	Min	Typ	Max	Unit
Counter Resolution		16		Bits
Edge Resolution (Single Update Mode)		100		ns
Edge Resolution (Double Update Mode)		50		ns
Programmable Dead Time Range	0		100	µs
Programmable Dead Time Increments		100		ns
Programmable Pulse Deletion Range		0	100	µs
Programmable Pulse Deletion Increments		100		ns
PWM Frequency Range	150			Hz
PWMSYNC Pulsewidth (T_{CRST})	0.05		12.5	µs
Gate Drive Chop Frequency Range	0.02		5	MHz

Restarting the PWM after a fault condition is detected requires clearing the fault and reinitializing the PWM. Clearing the fault requires that $\overline{\text{PWMTRIP}}$ returns to a HI state. After the fault has been cleared, the PWM can be restarted by writing to registers PWMTM, PWMCHA, PWMCHB, and PWMCHC. After the fault is cleared and the PWM registers are initialized, internal timing of the three-phase timing unit will resume, and the new duty cycle values will be latched on the next rising edge of PWMSYNC.

PWM Registers

The configuration of the PWM registers is described at the end of the data sheet. The parameters of the PWM block are tabulated in Table V.

ADC OVERVIEW

The ADC of the ADMCF326 is based upon the single slope conversion technique. This approach offers an inherently monotonic conversion process within the noise and stability of its components, and there will be no missing codes.

Table VI. ADC Auxiliary Channel Selection

Select	MODECTRL (1) ADCMUX1	MODECTRL (0) ADCMUX0
VAUX0	0	0
VAUX1	0	1
VAUX2	1	0
Calibration (V_{REF})	1	1

The single slope technique has been adapted on the ADMCF326 for four channels that are simultaneously converted. Refer to Figure 11 for the functional schematic of the ADC. Three of the main inputs (V1, V2, and V3) are directly connected as high impedance voltage inputs. The fourth channel has been configured with a serially-connected 4-to-1 multiplexer. Table VI shows the multiplexer input selection codes. One of these auxiliary multiplexed channels is used to calibrate the ramp against the internal voltage reference (V_{REF}).

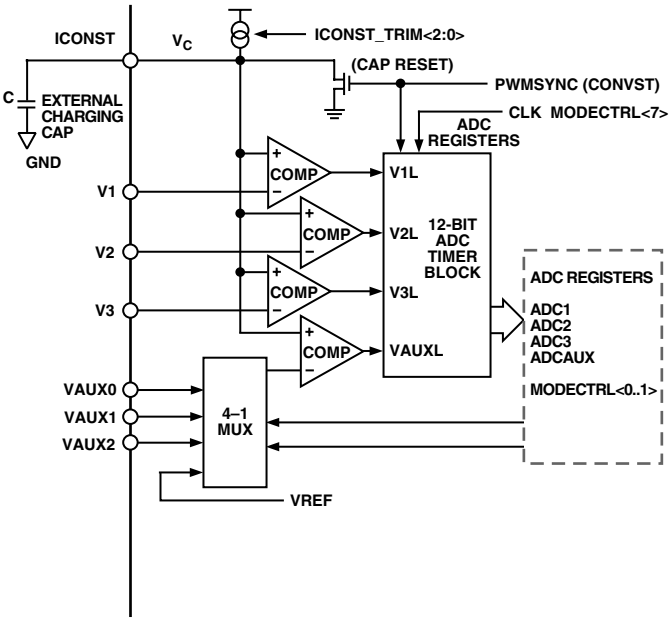


Figure 11. ADC Overview

Comparing each ADC input to a reference ramp voltage and timing the comparison of the two signals performs the conversion process. The actual conversion point is the time point intersection of the input voltage and the ramp voltage (V_C) as shown in Figure 12. This time is converted to counts by the 12-bit ADC Timer Block and is stored in the ADC registers. The ramp voltage used to perform the conversion is generated by driving a fixed current into an off-chip capacitor, where the capacitor voltage is

$$V_C = (I/C) \times t$$

Following reset, $V_C = 0$ at $t = 0$. This reset and the start of the conversion process are initiated by the PWMSYNC pulse, as shown in Figure 12. The width of the PWMSYNC pulse is controlled by the PWMSYNCWT Register and should be programmed according to Figure 13 to ensure complete resetting. In order to compensate for IC process manufacturing tolerances (and to adjust for capacitor tolerances), the current source of the ADMCF326 is software programmable. The software setting of the magnitude of the ICONST current generator is accomplished by selecting one of eight steps over approximately 20% current range.

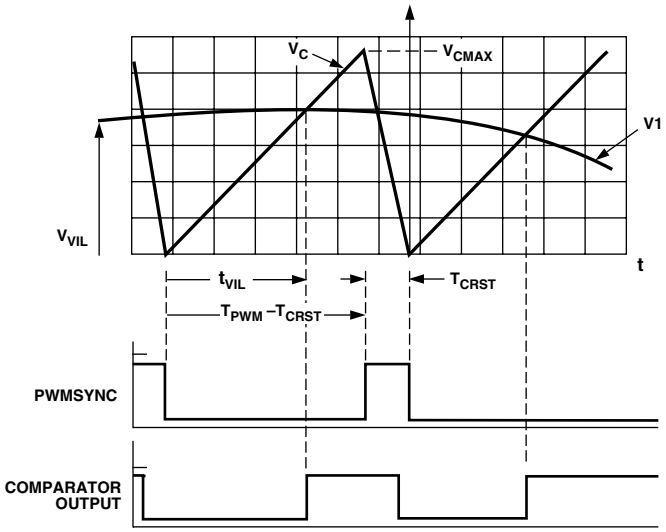


Figure 12. Analog Input Block Operation

The ADC system consists of four comparators and a single timer, which may be clocked at either the DSP rate or half the DSP rate, depending on the setting of the ADCCNT bit (Bit 7) of the MODECTRL Register. When this bit is cleared, the timers count at a slower rate of CLKIN. When this bit is set, they count at CLKOUT or twice the rate of CLKIN. ADC1, ADC2, ADC3, and ADCAUX are the registers that capture the conversion times, which are effectively the timer values, when the associated comparator trips.

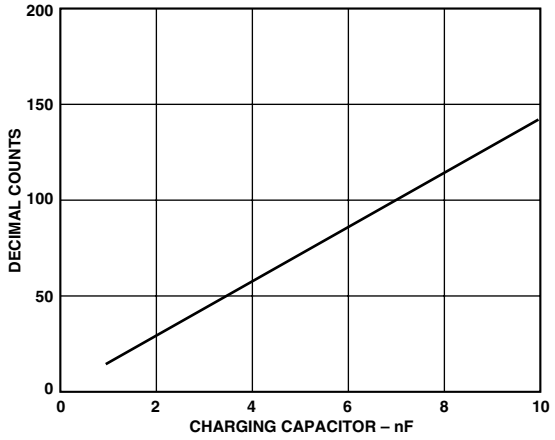


Figure 13. PWMSYNCWT Program Value

ADC Resolution

The ADC is intrinsically linked to the PWM block through the PWMSYNC pulse controlling the ADC conversion process. Because of this link, the effective resolution of the ADC is a function of both the PWM switching frequency and the rate at which the ADC counter timer is clocked. For a CLKOUT period of t_{CK} and a PWM period of T_{PWM}, the maximum count of the ADC is given by:

$$Max\ Count = \min\left(4095, \left(T_{PWM} - T_{CRST}\right)/2\,t_{CK}\right)$$

for MODECTRL Bit $7 = 1$

$$Max\ Count = \min\left(4095, \left(T_{PWM} - T_{CRST}\right)/t_{CK}\right)$$

for MODECTRL Bit $7 = 1$

Where T_{PWM} is equal to the PWM period if operating in Single Update Mode, or it is equal to half that period if operating in Double Update Mode. For an assumed CLKOUT frequency of 20 MHz and PWMSYNC pulsewidth of 2.0 µs, the effective resolution of the ADC block is tabulated for various PWM switching frequencies in Table VII.

Table VII. ADC Resolution Examples

PWM Frequency (kHz)	MODECTRL[7] = 0 Max Count	MODECTRL[7] = 0 Effective Resolution	MODECTRL[7] = 1 Max Count	MODECTRL[7] = 1 Effective Resolution
2.4	4095	12	4095	12
4	2480	>11	4095	12
8	1230	>10	2460	>11
18	535	>9	1070	>10
25	380	>8	760	>9

Charging Capacitor Selection

The charging capacitor value is selected based on the sample (PWM) frequency desired. A too-small capacitor value will reduce the available resolution of the ADC by having the ramp voltage rise rapidly and convert too quickly, not utilizing all possible counts available in the PWM cycle. Too large a capacitor may not convert in the available PWM cycle returning 0x000. To select a charging capacitor, use Figure 14, select the sampling frequency desired, determine if the current source is to be tuned to a nominal 100 µA or left in the default (0x0 code) trim state, then determine the proper charge capacitor off the appropriate curve.

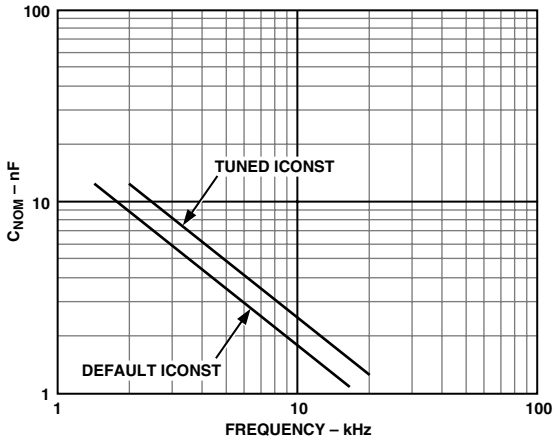


Figure 14. Timing Capacitor Selection

Programmable Current Source

The ADMCF326 has an internal current source that is used to charge an external capacitor, generating the voltage ramp used for conversion. The magnitude of the output of the current source circuit is subject to manufacturing variations and can vary from one device to the next. Therefore, the ADMCF326 incudes a programmable current source whose output can always be tuned to within 5% of the target 100 µA. A 3-bit register, ICONST_TRIM, allows the user to make this adjustment. The output current is proportional to the value written to the register: 0x0 produces the minimum output, and 0x7 produces the maximum output. The default value of ICONST_TRIM after reset is 0x0.

ADC Reference Ramp Calibration

The peak of the ADC ramp voltage should be as close as possible to 3.5 V to achieve the optimum ADC resolution and signal range. When the current source is in the default state, the peak of the ADC ramp slope will be lower than this "3.5 V" target ramp. When the current source value is increased, the ADC ramp slope will become closer to the target value. The "tuned" ramp slope is the one closest to the target ramp.

A simple calibration procedure using the internal 2.5 V reference voltage allows the selection of the ICONST_TRIM Register value to reach this:

1. A high quality linear ADC capacitor is selected using Figure 14 for a tuned ICONST.
2. Program PWMSYNCWT to proper count as in Figure 13.
3. The ADC Max Count is calculated, as described in a previous section.
4. The target reference conversion is calculated as TARGET = (Max Count) × (2.5 V/3.5 V).
5. Reset or software sets the ICONST_TRIM Register to zero.
6. Select calibration channel in software on ADC multiplexer.
7. The calibration channel value is compared with the target reference conversion.
8. If this value is greater than the TARGET, the ICONST_TRIM value is incremented by one, and Step 7 is repeated.
9. If the calibration channel value is less than the TARGET, the calibration is completed.

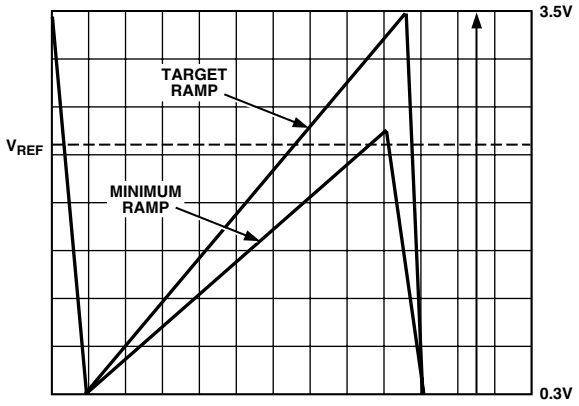


Figure 15. Current Ramp

ADC Registers

The configuration of all registers of the ADC System is shown at the end of the data sheet.

AUXILIARY PWM TIMERS

Overview

The ADMCF326 provides two variable frequency, variable duty cycle, 8-bit, auxiliary PWM outputs that are available at the AUX1 and AUX0 pins when enabled. These auxiliary PWM outputs can be used to provide switching signals to other circuits in a typical motor control system such as power factor corrected front end converters or other switching power converters. Alternatively, by addition of a suitable filter network, the auxiliary PWM output signals can be used as simple single-bit digital-to-analog converters.

The auxiliary PWM system of the ADMCF326 can operate in two different modes: Independent mode or Offset mode. The operating mode of the auxiliary PWM system is controlled by Bit 8 of the MODECTRL Register. Setting Bit 8 of the MODECTRL Register places the auxiliary PWM system in the Independent Mode. In this mode, the two auxiliary PWM generators are completely independent, and separate switching frequencies and duty cycles may be programmed for each auxiliary PWM output. In this mode, the 8-bit AUXTM0 Register sets the switching frequency of the signal at the AUX0 output pin. Similarly, the 8-bit AUXTM1 Register sets the switching frequency of the signal at the AUX1 pin. The fundamental time increment for the auxiliary PWM outputs is twice the DSP instruction rate (or 2 t_{CK}) and the corresponding switching periods are given by:

$$T_{AUX\ 0} = 2 \times (AUXTM0 + 1) \times t_{CK}$$

$$T_{AUX\ 1} = 2 \times (AUXTM1 + 1) \times t_{CK}$$

Since the values in both *AUXTM*0 and *AUXTM*1 can range from 0 to 0xFF, the achievable switching frequency of the auxiliary PWM signals may range from 39.1 kHz to 10 MHz for a CLKOUT frequency of 20 MHz.

The on-time of the two auxiliary PWM signals is programmed by the two 8-bit AUXCH0 and AUXCH1 Registers, according to:

$$T_{ON\ ,AUX\ 0} = 2 \times (AUXTM0) \times t_{CK}$$

$$T_{ON\ ,AUX\ 1} = 2 \times (AUXTM1) \times t_{CK}$$

so that output duty cycles from 0% to 100% are possible. Duty cycles of 100% are produced if the on-time value exceeds the period value. Typical auxiliary PWM waveforms in Independent Mode are shown in Figure 16(a).

When Bit 8 of the MODECTRL Register is cleared, the auxiliary PWM channels are placed in Offset Mode. In Offset Mode, the switching frequencies of the two signals on the AUX0 and AUX1 pins are identical and controlled by AUXTM0 in a manner similar to that previously described for Independent Mode. In addition, the on times of both the AUX0 and AUX1 signals are controlled by the AUXCH0 and AUXCH1 Registers as before. However, in this mode the AUXTM1 Register defines the offset time from the rising edge of the signal on the AUX0 pin to that on the AUX1 pin according to:

$$T_{OFFSET} = 2 \times (AUXTM1 + 1) \times t_{CK}$$

For correct operation in this mode, the value written to the AUXTM1 Register must be less than the value written to the AUXTM0 Register. Typical auxiliary PWM waveforms in Offset Mode are shown in Figure 16(b). Again, duty cycles from 0% to 100% are possible in this mode.

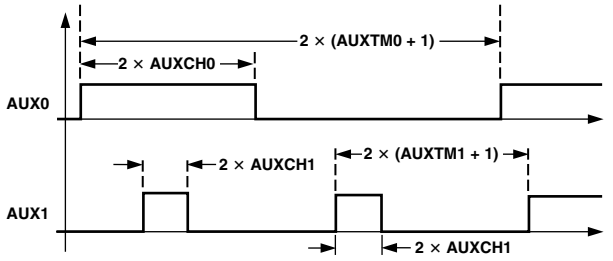
In both operating modes, the resolution of the auxiliary PWM system is eight bits only at the minimum switching frequency (AUXTM0 = AUXTM1 = 255 in Independent Mode, AUXTM0 = 255 in offset mode). Obviously, as the switching frequency is increased, the resolution is reduced.

Values can be written to the auxiliary PWM registers at any time. However, new duty cycle values written to the AUXCH0 and AUXCH1 Registers only become effective at the start of the next cycle. Writing to the AUXTM0 or AUXTM1 Registers causes the internal timers to be reset to 0 and new PWM cycles to begin.

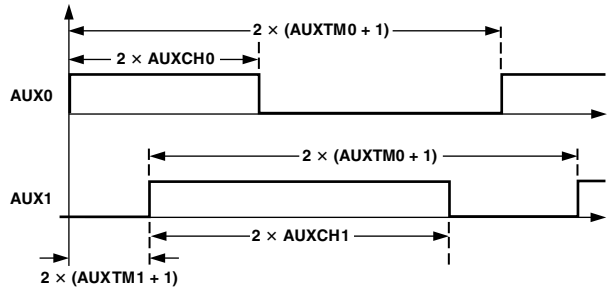
By default following a reset, Bit 8 of the MODECTRL Register is cleared, thus enabling Offset Mode. In addition, the registers AUXTM0 and AUXTM1 default to 0xFF, corresponding to the minimum switching frequency and zero offset. The on-time registers AUXCH0 and AUXCH1 default to 0x00.

Auxiliary PWM Interface, Registers and Pins

The registers of the auxiliary PWM system are summarized at the end of the data sheet.



(a) Independent Mode



(b) Offset Mode

Figure 16. Typical Auxiliary PWM Signals. (All Times in Increments of t_{CK})

PWM DAC Equation

The auxiliary PWM output can be filtered in order to produce a low frequency analog signal between 0 V to V_{DD}. For example, a 2-pole filter with a 1.2 kHz cutoff frequency will sufficiently attenuate the PWM carrier. Figure 17 shows how the filter would be applied.

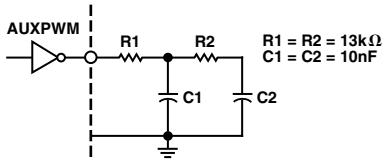


Figure 17. Auxiliary PWM Output Filter

WATCHDOG TIMER

The ADMCF326 incorporates a watchdog timer that can perform a full reset of the DSP and motor control peripherals in the event of software error. The watchdog timer is enabled by writing a timeout value to the 16-bit WDTIMER Register. The timeout value represents the number of CLKIN cycles required for the watchdog timer to count down to zero. When the watchdog timer reaches zero, a full DSP core and motor control peripheral reset is performed. In addition, Bit 1 of the SYSSTAT Register is set so that after a watchdog reset, the ADMCF326 can determine that the reset was due to the timeout of the watchdog timer and not an external reset. Following a watchdog reset, Bit 1 of the SYSSTAT Register may be cleared by writing zero to the WDTIMER Register. This clears the status bit but does not enable the watchdog timer.

On reset, the watchdog timer is disabled and is only enabled when the first timeout value is written to the WDTIMER Register. To prevent the watchdog timer from timing out, the user must write to the WDTIMER Register at regular intervals (shorter than the programmed WDTIMER period value). On all but the first write to WDTIMER, the particular value written to the register is unimportant since writing to WDTIMER simply reloads the first value written to this register.

PROGRAMMABLE DIGITAL INPUT/OUTPUT

The ADMCF326 has nine programmable digital input/output (PIO) pins that are all multiplexed with other functions. The nine PIO lines PIO0–PIO8 are multiplexed with the serial port (Pins PIO0/TFS1 to PIO5/RFS1), the CLKOUT (Pin PIO6/CLKOUT), and the auxiliary PWM outputs (Pins PIO7/AUX1 and PIO8/AUX0). When configured as a PIO, each of these nine pins can act as an input, output, or an interrupt source.

The operating mode of pins PIO0/TFS1 to PIO7/AUX1 is controlled by the PIOSELECT Register. This 8-bit register has a bit for each input so that the mode of each pin may be selected individually. Bit 0 of PIOSELECT controls the operation of the PIO0/TFS1 pin. Bit 1 controls the PIO1/DT1 pin, etc. Setting the appropriate bit in the PIOSELECT Register causes the corresponding pin to be configured for PIO functionality. Clearing the bit selects the alternate (SPORT, CLKOUT, or AUXPWM) mode of the corresponding pin. Following power-on reset, all bits of PIOSELECT are set such that PIO functionality is selected. The operating mode of the PIO8/AUX0 pin is selected by Bit 1 of the PIODATA1 Register. In a manner identical to the PIOSELECT Register, setting this bit enables PIO functionality (PIO8) while clearing the bit enables auxiliary PWM functionality (AUX0).

Once PIO functionality has been selected for any or all of these nine pins, the direction may be set by the 8-bit PIODIR0 Register (for PIO0 to PIO7) and the 1-bit PIODIR1 Register (for PIO8). Clearing any bit configures the corresponding PIO line as an input while setting the bit configures it as an output. By default, following a reset, all bits of PIODIR0 and PIODIR1 are cleared configuring the PIO lines as inputs.

The data of the PIO0 to PIO8 lines is controlled by the PIODATA0 Register (for PIO0 to PIO7) and Bit 0 of the PIODATA1 Register (for PIO8). These registers can be used to read data from those PIO lines configured as inputs and write data to those configured as outputs. Any of the nine pins that have been configured for PIO functionality can be made to act as an interrupt source by setting the appropriate bit of the PIOINTEN0 Register (for PIO0 to PIO7) or the PIOINTEN1 Register (for PIO8). In order to act as an interrupt source, the pin must also be configured as an input. An interrupt is generated upon a change of state (low-to-high transition or high-to-low transition) on any input that has been configured as an interrupt source. Following a change of state event on any such input, the corresponding bit is set in the PIOFLAG0 Register (for PIO0 to PIO7), and PIOFLAG1 (for PIO8) and a common PIO interrupt is generated. Reading the PIOFLAG0 and PIOFLAG1 Registers permits determining the interrupt source. Reading the PIOFLAG0 and PIOFLAG1 Registers automatically clears all bits of the registers.

Table VIII. Auxiliary PWM Timer

AUXILIARY PWM TIMERS

Parameter	Test Conditions	Min	Typ	Max	Unit
Resolution			8		Bits
PWM Frequency	10 MHz CLKIN	0.039			MHz

Following power-on or reset, all bits of PIOINTEN0 and PIOINTEN1 are cleared so that no interrupts are enabled.

Each PIO line has an internal pull-down resistor so that following power-on or reset, all nine lines are configured as input PIOs and will be read as logic lows if left unconnected.

Multiplexing of PIO Lines

The PIO0–PIO5 lines are multiplexed on the ADMCF326 with the functional lines of the serial port, SPORT1. Although the PIOSELECT Register permits individual selection of the functionality of each pin, certain restrictions apply when using SPORT1 for serial communications.

In general, when transmitting and receiving data on the DTI and DRIB pins, respectively, the PIO0/TFS1 and PIO5/RFS1 pins must also be selected for SPORT (TFS1 and RFS1) functionality even if unframed communication is implemented. Therefore, when using SPORT1 for any type of serial communication, the minimal setting for PIOSELECT is 0xD8 (i.e., select DTI, DRIB, RFS1 and TFS1, select PIO7, PIO6, PIO4, PIO3 as digital I/O).

If the serial port communications use an internally generated SCLK1, the PIO3/SCLK1 pin may be used as a general-purpose PIO line. When External SCLK Mode is selected, the PIO/SCLK1 pin must be enabled as SCLK1 (PIOSELECT [3] = 0).

When the DRIB data receive line of SPORT1 is selected as the data receive line (MODECTRL [4] = 1), the PIO4/DRIA line may be used as a general-purpose PIO pin. When the DRIA data receive line of SPORT1 is selected as the data receive line (MODECTRL [4] = 0), the PIO2/DRIB line may be used as a general-purpose PIO pin.

The functionality of the PIO6/CLKOUT, PIO7/AUX1, and PIO8/AUX0 pins may be selected on a pin-by-pin basis as desired.

PIO Registers

The configuration of all registers of the PIO system is shown at the end of the data sheet.

INTERRUPT CONTROL

The ADMCF326 can respond to 16 different interrupt sources, some of which are generated by internal DSP core interrupts and others from the motor control peripherals. The DSP core interrupts include the following:

- A Peripheral (or IRQ2) Interrupt
- A SPORT1 Receive (or $\overline{\text{IRQ0}}$) and a SPORT1 Transmit (or $\overline{\text{IRQ1}}$) Interrupt
- Two Software Interrupts
- An Interval Timer Time-Out Interrupt

The interrupts generated by the motor control peripherals include:

- A PWMSYNC Interrupt
- Nine Programmable Input/Output (PIO) Interrupts
- A PWM Trip Interrupt

The core interrupts are internally prioritized and individually maskable. All peripheral interrupts are multiplexed into the DSP core through the peripheral ($\overline{\text{IRQ2}}$) interrupt**.**

The PWMSYNC interrupt is triggered by a low-to-high transition on the PWMSYNC pulse. The $\overline{\text{PWMTRIP}}$ interrupt is triggered on a high-to-low transition on the $\overline{\text{PWMTRIP}}$ pin, or by writing to the PWMSWT Register. A PIO interrupt is detected on any change of state (high-to-low or low-to-high) on the PIO lines.

The ADMCF326 interrupt control system is configured and controlled by the IFC, IMASK, and ICNTL Registers of the DSP core and by the IRQFLAG register for the PWMSYNC and $\overline{\text{PWMTRIP}}$ interrupts. PIO interrupts are enabled and disabled by the PIOINTEN0 and PIOINTEN1 Registers.

Table IX. Interrupt Vector Addresses

Interrupt Source	Interrupt Vector Address
$\overline{\text{PWMTRIP}}$	0x002C (Highest Priority)
Peripheral Interrupt ($\overline{\text{IRQ2}}$)	0x0004
PWMSYNC	0x000C
PIO	0x0008
Software Interrupt 1	0x0018
Software Interrupt 0	0x001C
SPORT1 Transmit Interrupt (or $\overline{\text{IRQ1}}$)	0x0020
SPORT1 Receive Interrupt (or $\overline{\text{IRQ0}}$)	0x0024
Timer	0x0028 (Lowest Priority)

Interrupt Masking

Interrupt masking (or disabling) is controlled by the IMASK register of the DSP core. This register contains individual bits that must be set to enable the various interrupt sources. If any peripheral interrupt (PWMSYNC, $\overline{\text{PWMTRIP}}$, or PIO) is to be enabled, the $\overline{\text{IRQ2}}$ interrupt enable bit (Bit 9) of the IMASK Register must be set. The configuration of the IMASK Register of the ADMCF326 is shown at the end of the data sheet.

Interrupt Configuration

The IFC and ICNTL Registers of the DSP core control and configure the interrupt controller of the DSP core. The IFC register is a 16-bit register that may be used to force and/or clear any of the eight DSP interrupts. Bits 0 to 7 of the IFC register may be used to clear the DSP interrupts while Bits 8 to 15 can be used to force a corresponding interrupt. Writing to Bits 11 and 12 in IFC is the only way to create the two software interrupts.

The ICNTL register is used to configure the sensitivity (edge or level) of the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts and to enable/disable interrupt nesting. Setting Bit 0 of ICNTL configures the $\overline{\text{IRQ0}}$ as edge-sensitive, while clearing the bit configures it for level-sensitive. Bit 1 is used to configure the $\overline{\text{IRQ1}}$ interrupt.

Bit 2 is used to configure the $\overline{\text{IRQ2}}$ interrupt. It is recommended that the $\overline{\text{IRQ2}}$ interrupt always be configured as level-sensitive to ensure that no peripheral interrupts are lost. Setting Bit 4 of the ICNTL Register enables interrupt nesting. The configuration of both the IFC and ICNTL Registers is shown at the end of the data sheet.

Interrupt Operation

Following a reset, the ROM code on the ADMCF326 must copy a default interrupt vector table into program memory RAM from Address 0x0000 to 0x002F. Since each interrupt source has a dedicated four-word space in this vector table, it is possible to code short interrupt service routines (ISR) in place. Alternatively, it may be necessary to insert a JUMP instruction to the appropriate start address of the interrupt service routine if more memory is required for the ISR.

When an interrupt occurs, the program sequencer ensures that there is no latency (beyond synchronization delay) when processing unmasked interrupts. In the case of the timer, SPORT1, and software interrupts, the interrupt controller automatically jumps to the appropriate location in the interrupt vector table. At this point, a JUMP instruction to the appropriate ISR is required.

Motor control peripheral interrupts are slightly different. When a peripheral interrupt is detected, a bit is set in the IRQFLAG Register for PWMSYNC and $\overline{\text{PWMTRIP}}$, or in the PIOFLAG0 or PIOFLAG1 Registers for a PIO interrupt, and the $\overline{\text{IRQ2}}$ line is pulled low until all pending interrupts are acknowledged.

The DSP software must determine the source of the interrupts by reading IRQFLAG Register. If more than one interrupt occurs simultaneously, the higher priority interrupt service routine is executed. Reading the IRQFLAG Register clears the $\overline{\text{PWMTRIP}}$ and PWMSYNC bits and acknowledges the interrupt, thus allowing further interrupts when the ISR exits.

A user's PIO interrupt service routine must read the PIOFLAG0 and PIOFLAG1 Registers to determine which PIO port is the source of the interrupt. Reading registers PIOFLAG0 and PIOFLAG1 clears all bits in the registers and acknowledges the interrupt, thus allowing further interrupts after the ISR exits.

The configuration of all these registers is shown at the end of the data sheet.

SYSTEM CONTROLLER

The system controller block of the ADMCF326 performs the following functions:

1. Manages the interface and data transfer between the DSP core and the motor control peripherals
2. Handles interrupts generated by the motor control peripherals and generates a DSP core interrupt signal $\overline{\text{IRQ2}}$
3. Controls the ADC multiplexer select lines
4. Enables $\overline{\text{PWMTRIP}}$ and PWMSYNC interrupts
5. Controls the multiplexing of the SPORT1 pins to select either DR1A or DR1B data receive pins. It also allows configuration of SPORT1 as a UART interface.
6. Controls the PWM Single/Double Update Mode
7. Controls the ADC conversion time modes
8. Controls the auxiliary PWM Operation Mode
9. Contains a status register (SYSSTAT) that indicates the state of the $\overline{\text{PWMTRIP}}$ pin, the watchdog timer, and the PWM timer
10. Performs a reset of the motor control peripherals and control registers following a hardware, software, or watchdog initiated reset

SPORT1 Control

Both data receive pins are multiplexed internally into the single data receive input of SPORT1 as shown in Figure 18. Two control bits in the MODECTRL Register control the state of the SPORT1 pins by manipulating internal multiplexers in the ADMCF326.

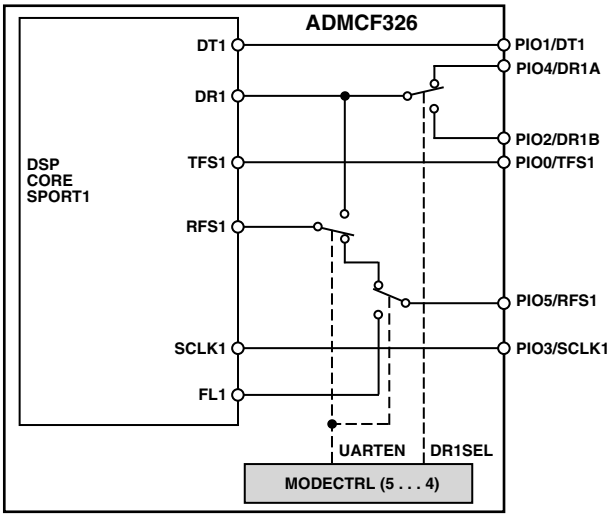


Figure 18. Internal Multiplexing of SPORT1 Pins

Bit 4 of the MODECTRL Register (DR1SEL) selects between the two data receive pins. Setting Bit 4 of MODECTRL connects pin DR1B to the internal data receive port DR1 of SPORT1. Clearing Bit 4 connects DR1A to DR1.

Setting Bit 5 of the MODECTRL Register (SPORT1 Mode) configures the serial port for UART Mode. In this mode, the DR1 and RFS1 pins of the internal serial port are connected together. Additionally, setting the SPORT1 Mode bit connects the FL1 flag of the DSP to the external PIO5/RFS1 pin.

Flag Pins

The ADMCF326 provides flag pins. The alternate configuration of SPORT1 includes a Flag In (FI) and Flag Out (FO) pin. This alternate configuration of SPORT1 is selected by Bit 10 of the DSP system control register, SYSCNTL at data memory address 0x3FFF. In the alternate configuration, the DR1 pin (either DR1A or DR1B depending upon the state of the DR1SEL bit) becomes the FI pin and the DT1 pin becomes the FO pin. Additionally, RFS1 is configured as the $\overline{\text{IRQ0}}$ interrupt input and TFS1 is configured as the $\overline{\text{IRQ1}}$ interrupt. The serial port clock, SCLK1, is still available in the alternate configuration.

Development Tools

Users are recommended to obtain the ADMCF326-EVALKIT from Analog Devices. The tool kit contains everything required to quickly and easily evaluate and develop applications using the ADMCF326 and ADMC326 DSP Motor Controllers. Please contact your ADI sales representative for ordering information.

Table X. Peripheral Register Map

Address (HEX)	Name	Bits Used	Function
0x2000	ADC1	[15 . . . 4]	ADC Results for V1
0x2001	ADC2	[15 . . . 4]	ADC Results for V2
0x2002	ADC3	[15 . . . 4]	ADC Results for V3
0x2003	ADCAUX	[15 . . . 4]	ADC Results for VAUX
0x2004	PIODIR0	[7 . . . 0]	PIO0 . . . 7 Pins Direction Setting
0x2005	PIODATA0	[7 . . . 0]	PIO0 . . . 7 Pins Input/Output Data
0x2006	PIOINTEN0	[7 . . . 0]	PIO0 . . . 7 Pins Interrupt Enable
0x2007	PIOFLAG0	[7 . . . 0]	PIO0 . . . 7 Pins Interrupt Status
0x2008	PWMTM	[15 . . . 0]	PWM Period
0x2009	PWMDT	[9 . . . 0]	PWM Dead Time
0x200A	PWMPD	[9 . . . 0]	PWM Pulse Deletion Time
0x200B	PWMGATE	[9 . . . 0]	PWM Gate Drive Configuration
0x200C	PWMCHA	[15 . . . 0]	PWM Channel A Pulsewidth
0x200D	PWMCHB	[15 . . . 0]	PWM Channel B Pulsewidth
0x200E	PWMCHC	[15 . . . 0]	PWM Channel C Pulsewidth
0x200F	PWMSEG	[8 . . . 0]	PWM Segment Select
0x2010	AUXCH0	[7 . . . 0]	AUX PWM Output 0
0x2011	AUXCH1	[7 . . . 0]	AUX PWM Output 1
0x2012	AUXTM0	[7 . . . 0]	Auxiliary PWM Frequency Value
0x2013	AUXTM1	[7 . . . 0]	Auxiliary PWM Frequency Value/Offset
0x2014			Reserved
0x2015	MODECTRL	[8 . . . 0]	Mode Control Register
0x2016	SYSSTAT	[3 . . . 0]	System Status
0x2017	IRQFLAG	[1 . . . 0]	Interrupt Status
0x2018	WDTIMER	[15 . . . 0]	Watchdog Timer
0x2019 . . . 43			Reserved
0x2044	PIODIR1	[0]	PIO8 Pin Direction Setting
0x2045	PIODATA1	[1 . . . 0]	PIO8 Data and Mode Control
0x2046	PIOINTEN1	[0]	PIO8 Pin Interrupt Enable
0x2047	PIOFLAG1	[0]	PIO8 Pin Interrupt Status
0x2048			Reserved
0x2049	PIOSELECT	[7 . . . 0]	PIO0 to PIO7 Mode Select
0x204A . . . 5F			Reserved
0x2060	PWMSYNCWT	[7 . . . 0]	PWMSYNC Pulsewidth
0x2061	PWMSWT	[0]	PWM S/W Trip Bit
0x2062 . . . 67			Reserved
0x2068	ICONST_TRIM	[2. . .0]	ICONST_TRIM
0x2069 . . . 70			Reserved
0x2080	FMCR	[15. . .0]	Flash Memory Control Register
0x2081	FMAR	[11. . .0]	Flash Memory Address Register
0x2082	FMDRH	[13. . .0]	Flash Memory Data Register High
0x2083	FMDRL	[15. . .0]	Flash Memory Data Register Low
0x2084 . . . FF			Reserved

Table XI. DSP Core Registers

Address	Name	Bits	Function
0x3FFF	SYSCNTL	[15 . . . 0]	System Control Register
0x3FFE	MEMWAIT	[15 . . . 0]	Memory Wait State Control Register
0x3FFD	TPERIOD	[15 . . . 0]	Interval Timer Period Register
0x3FFC	TCOUNT	[15 . . . 0]	Interval Timer Count Register
0x3FFB	TSCALE	[7 . . . 0]	Interval Timer Scale Register
0x3FFA . . . F3			Reserved
0x3FF2	SPORT1_CTRL_REG	[15 . . . 0]	SPORT1 Control Register
0x3FF1	SPORT1_SCLKDIV	[15 . . . 0]	SPORT1 Clock Divide Register
0x3FF0	SPORT1_RFSDIV	[15 . . . 0]	SPORT1 Receive Frame Sync Divide
0x3FEF	SPORT1_AUTOBUF_CTRL	[15 . . . 0]	SPORT1 Autobuffer Control Register

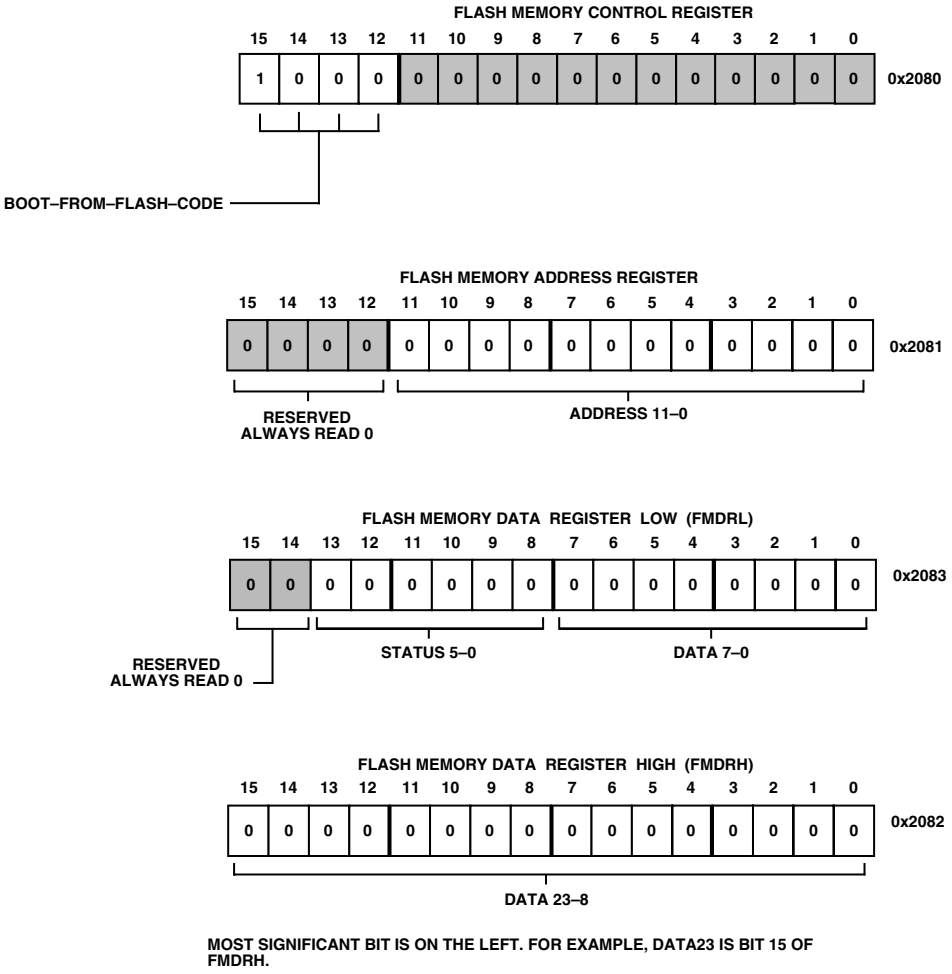


Figure 19. Configuration of Flash Memory Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

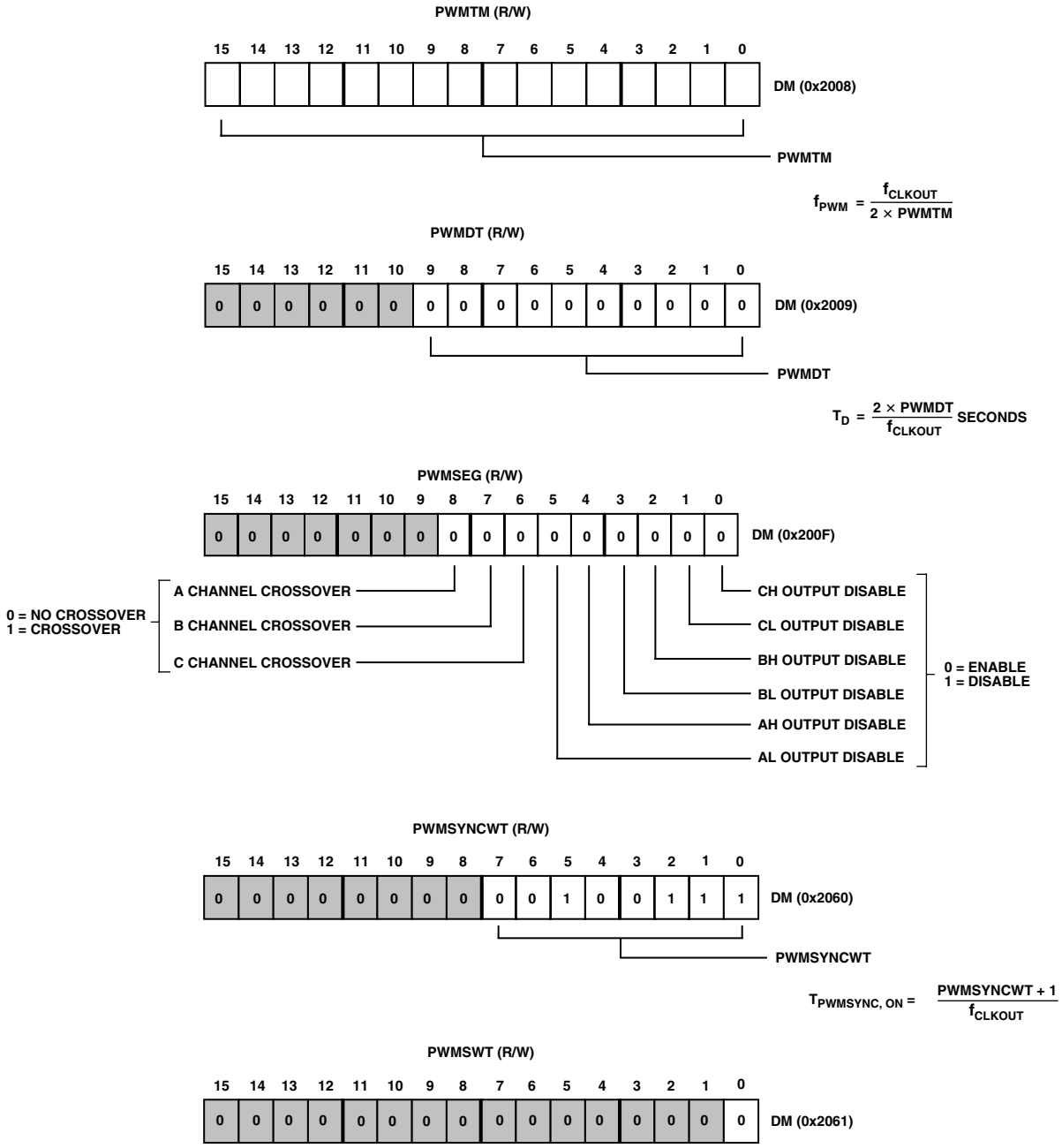


Figure 20. Configuration of PWM Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

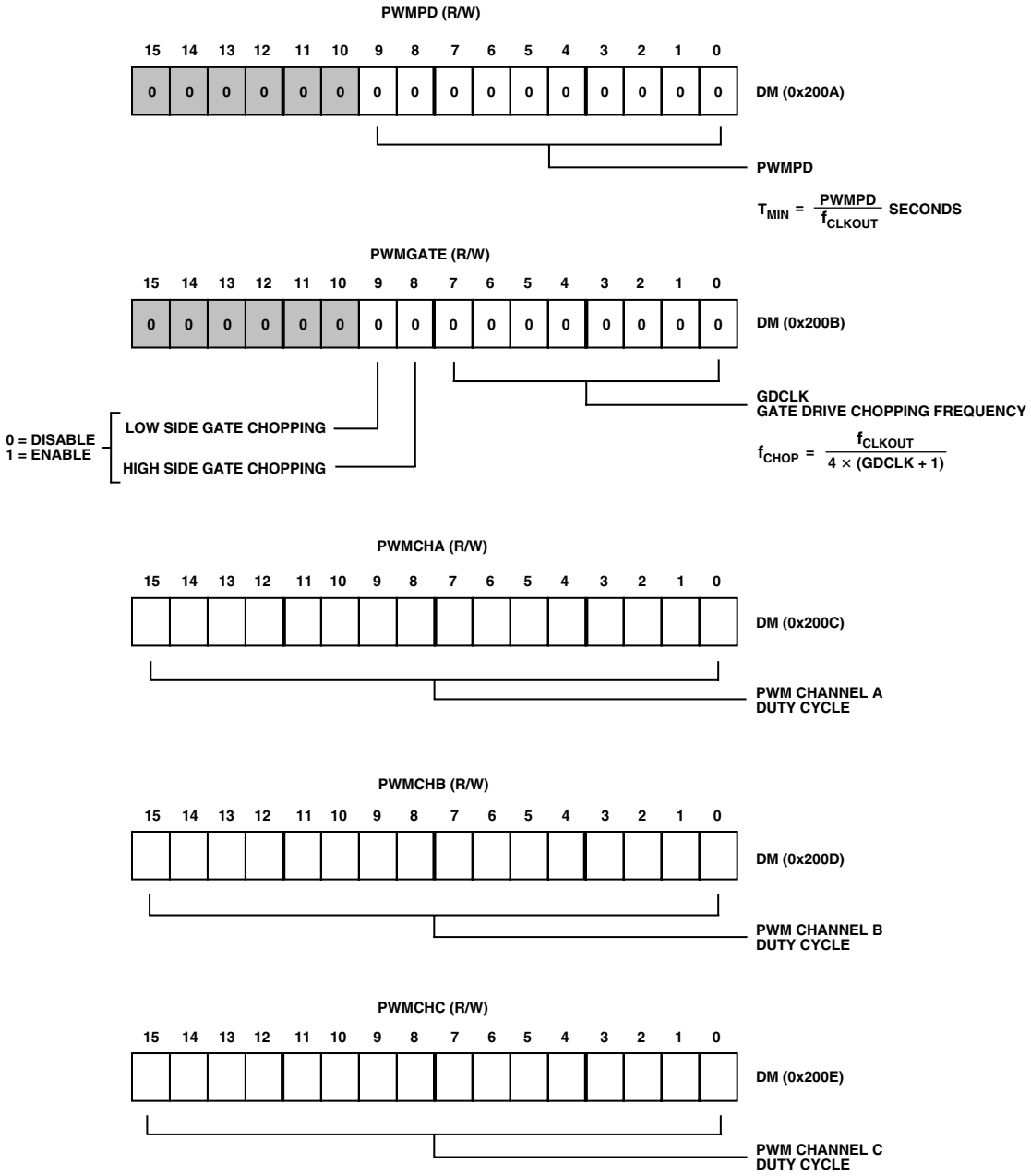


Figure 21. Configuration of Additional PWM Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

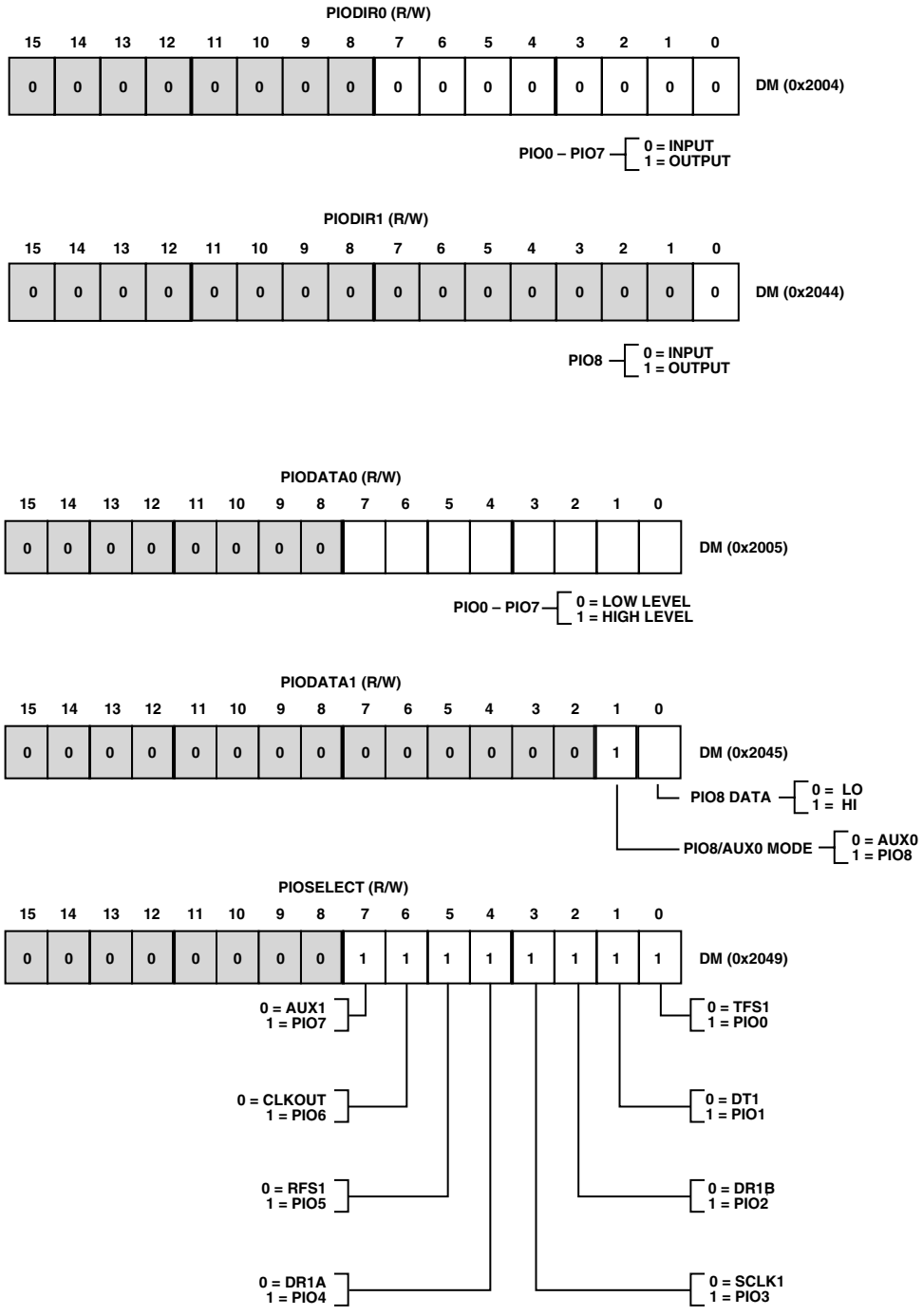


Figure 22. Configuration of PIO Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

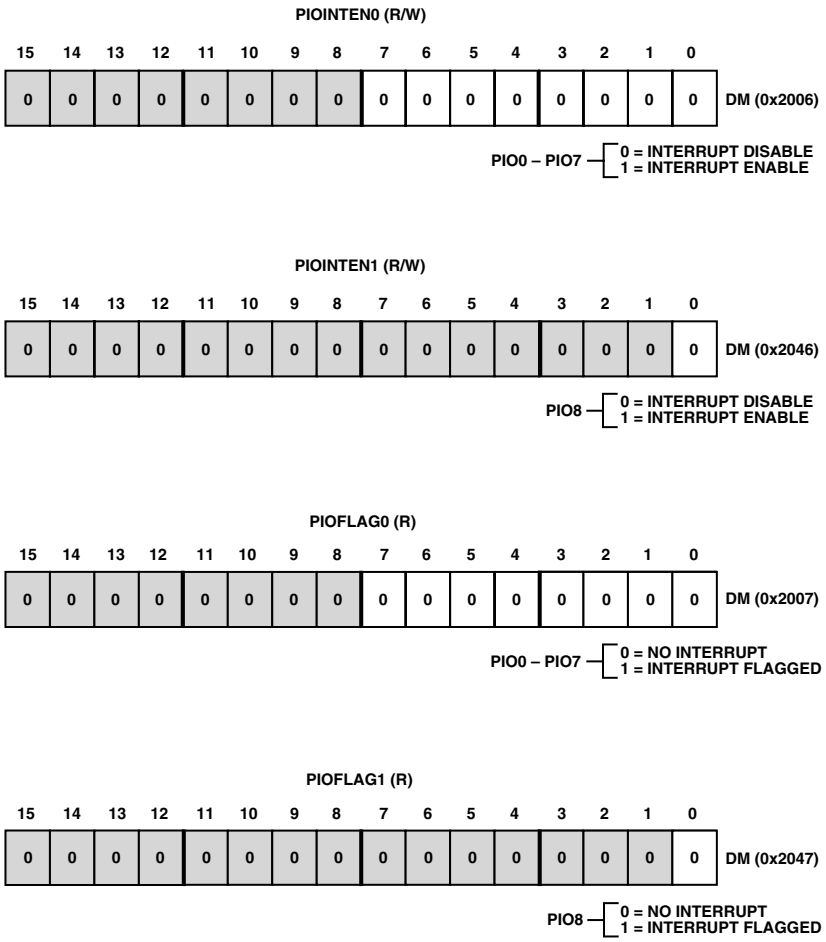


Figure 23. Configuration of Additional PIO Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

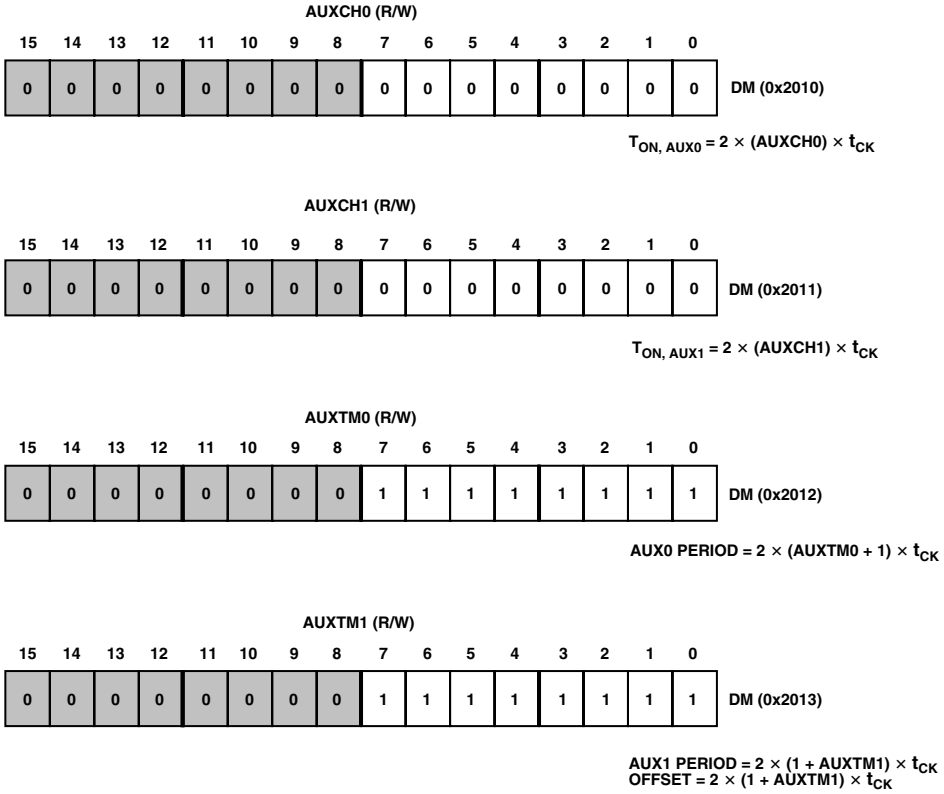


Figure 24. Configuration of AUX Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

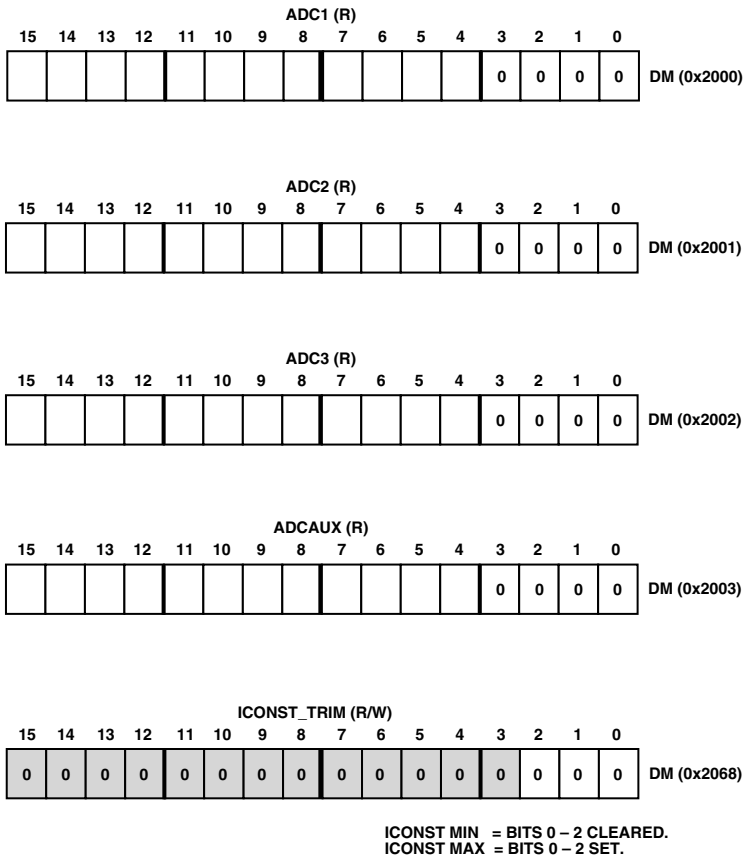


Figure 25. Configuration of Additional AUX Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

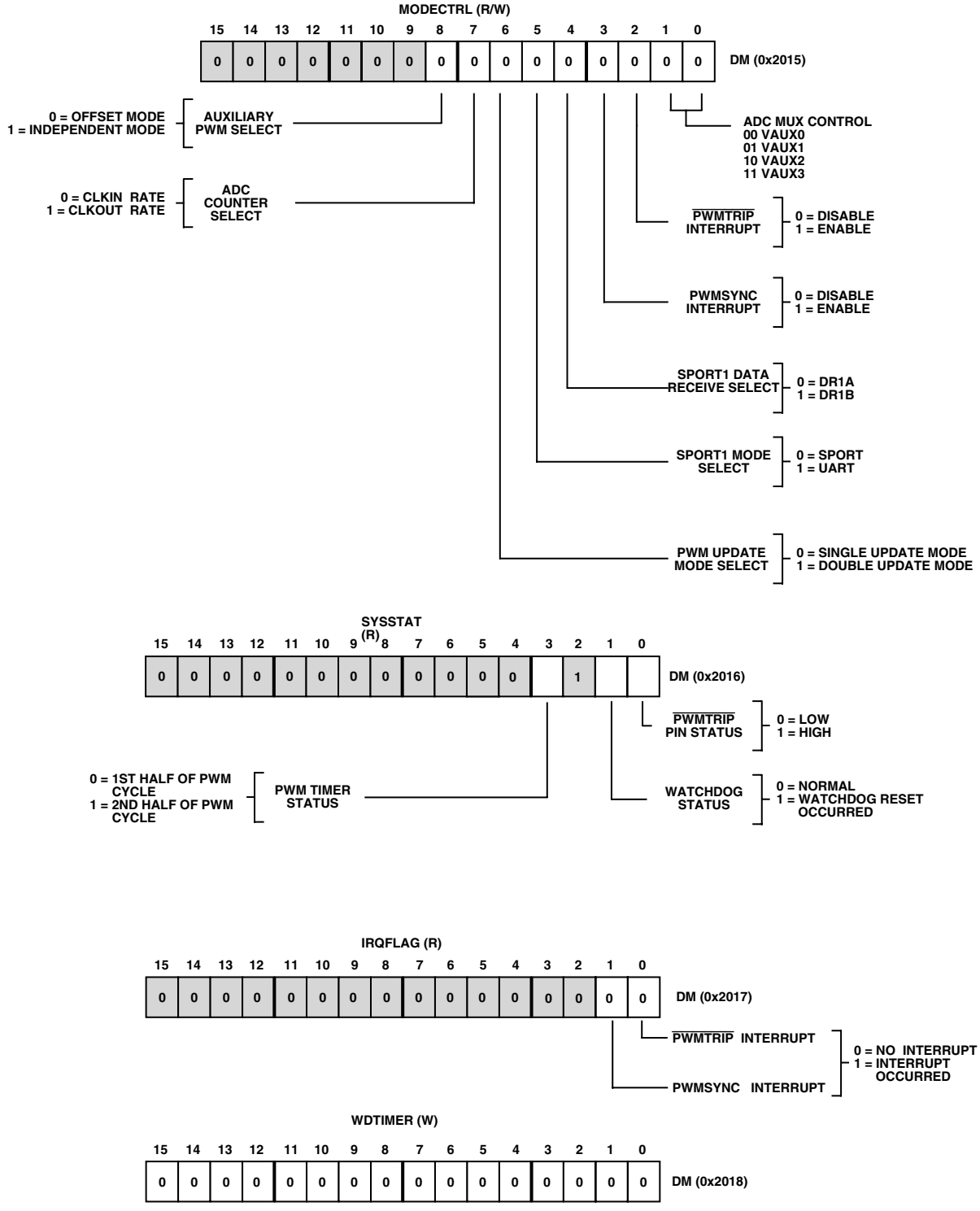


Figure 26. Configuration of Status Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

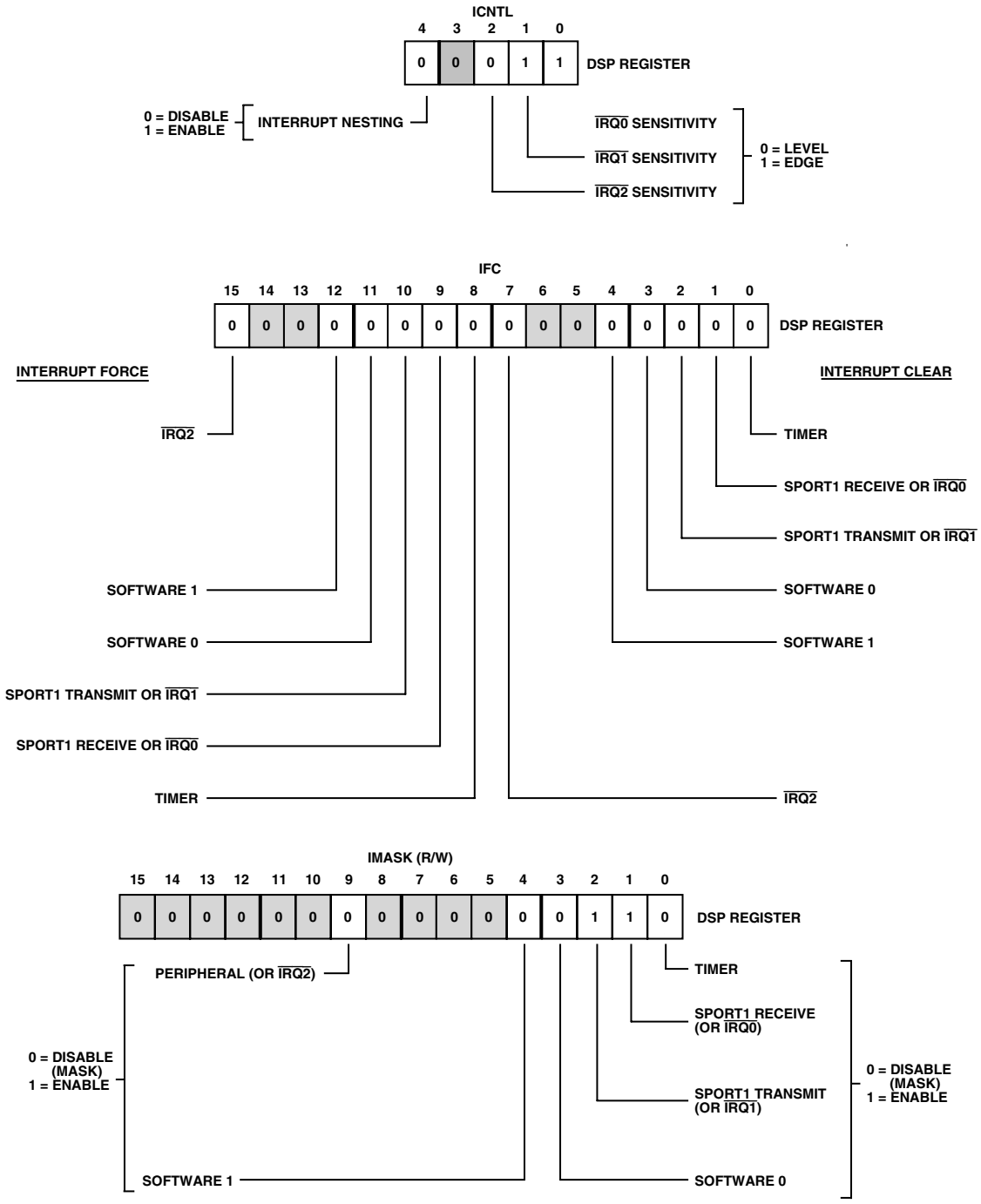


Figure 27. Configuration of Interrupt Control Registers

Default bit values are shown; if no value is shown, the bit field is undefined at reset. Reserved bits are shown on a gray field—these bits should always be written as shown.

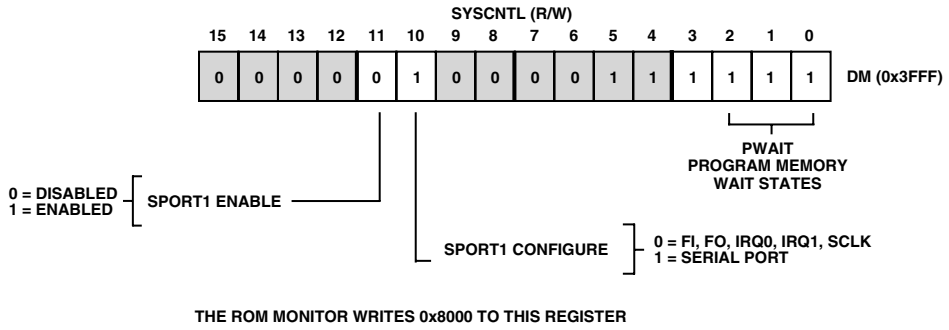
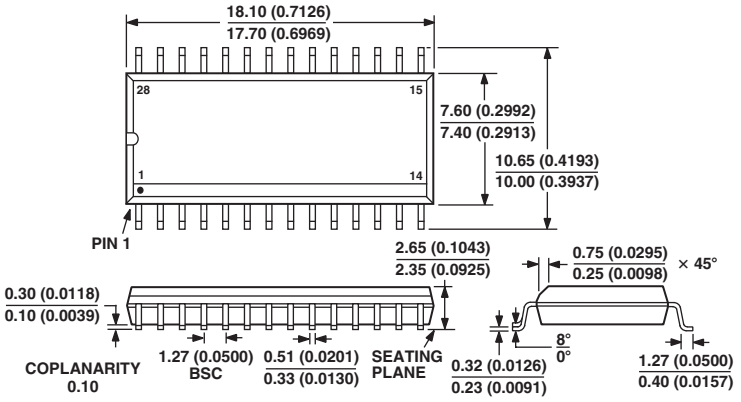


Figure 28. Configuration of Registers

OUTLINE DIMENSIONS

28-Lead Standard Small Outline Package [SOIC]
Wide-Body
(R-28)

Dimensions shown in millimeters and (inches)

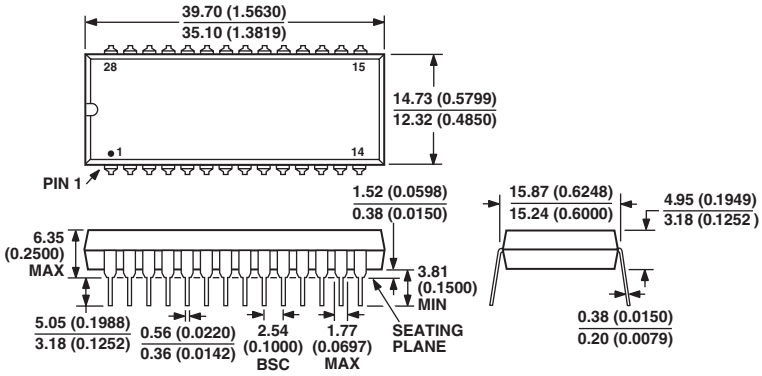


CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

COMPLIANT TO JEDEC STANDARDS MS-013AE

28-Lead Plastic Dual-In-Line Package [PDIP]
(N-28)

Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

ADMC326–Revision History

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8/02—Data Sheet changed from REV. 0 to REV. A.

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