Contents

Selection Guide

Description		-10	-12	-20	Unit
Maximum Access Time		10	12	20	ns
Maximum Operating Current	Automotive-A	100	–	85	mA
	Automotive-E	130	120	90	mA
Maximum CMOS Standby Current	Automotive-A	10	–	10	mA
	Automotive-E	15	15	15	mA

Pin Configuration

Figure 1. 44-pin SOJ/TSOP II pinout (Top View) [1]

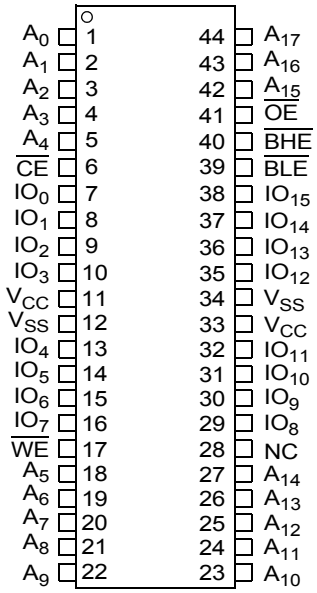
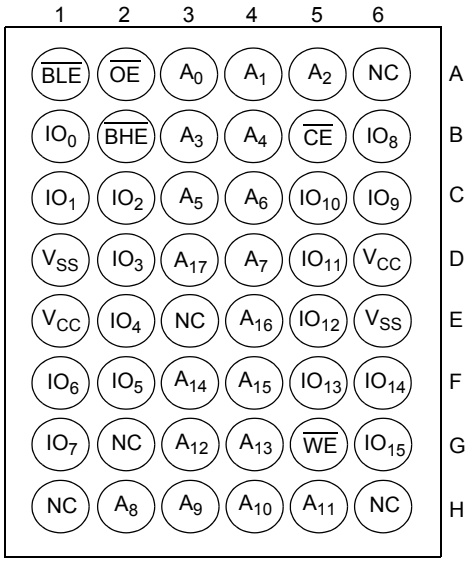


Figure 2. 48-ball FBGA pinout (Top View) [1]



Note
1. NC pins are not connected on the die.

Pin Definitions

Pin Name	SOJ, TSOP Pin Number	BGA Pin Number	I/O Type	Description
A_0–A_{17}	1–5, 18–27, 42–44	A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3	Input	**Address Inputs**. Used to select one of the address locations.
I/O_0–I/O_{15}	7–10,13–16, 29–32, 35–38	B1, C1, C2, D2, E2, F2, F1, G1, B6, C6, C5, D5, E5, F5, F6, G6	Input or Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	28	A6, E3, G2, H1, H6	No Connect	**No Connects**. Not connected to the die.
$\overline{WE}$	17	G5	Input or Control	**Write Enable Input, Active LOW**. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.
$\overline{CE}$	6	B5	Input or Control	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	B2, A1	Input or Control	**Byte Write Select Inputs, Active LOW**. $\overline{BHE}$ controls I/O_{15}–I/O_8, $\overline{BLE}$ controls I/O_7–I/O_0.
$\overline{OE}$	41	A2	Input or Control	**Output Enable, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, the I/O pins are tri-stated and act as input data pins.
V_{SS}	12, 34	D1, E6	Ground	**Ground for the Device**. Connected to ground of the system.
V_{CC}	11, 33	D6, E1	Power Supply	**Power Supply Inputs to the Device**.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND [2] .....–0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State [2] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [2] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Automotive-A	–40 °C to +85 °C	3.3 V ± 10%
Automotive-E	–40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		-20		Unit
				Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	–	0.4	–	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL} [2]	Input LOW Voltage			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Auto-A	–1	+1	–	–	–1	+1	µA
			Auto-E	–20	+20	–20	+20	–20	+20	
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	Auto-A	–1	+1	–	–	–1	+1	µA
			Auto-E	–20	+20	–20	+20	–20	+20	
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$	Auto-A	–	100	–	–	–	85	mA
			Auto-E	–	130	–	120	–	90	
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH}, or V_{IN} ≤ V_{IL}, f = f_{MAX}	Auto-A	–	40	–	–	–	40	mA
			Auto-E	–	45	–	45	–	45	
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	Auto-A	–	10	–	–	–	10	mA
			Auto-E	–	15	–	15	–	15	

Note

2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 0.5 V for pulse durations of less than 20 ns.

Capacitance

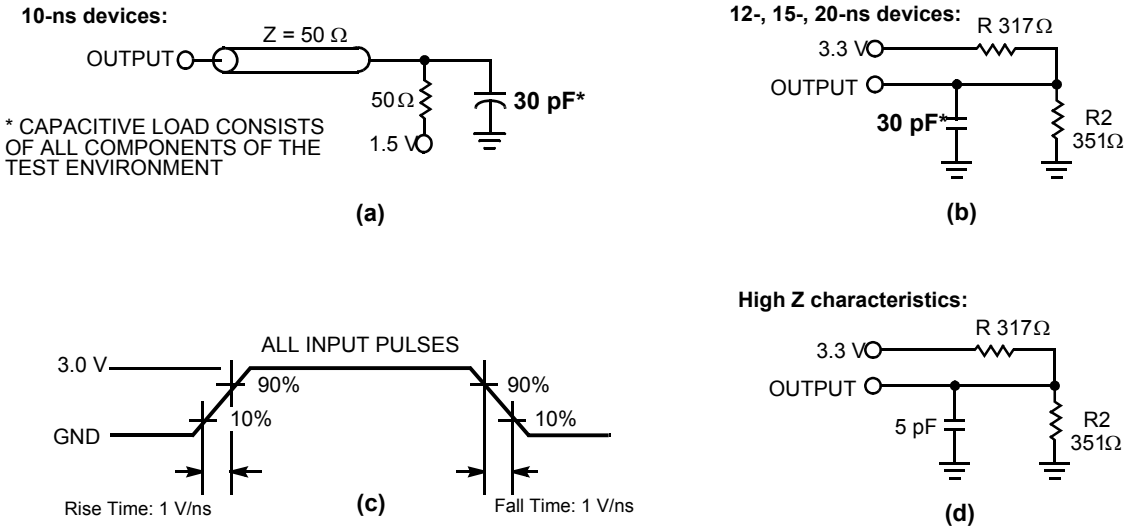
Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	44-pin SOJ	44-pin TSOP II	48-ball FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	25.99	42.96	38.15	°C/W
Θ_{JC}	Thermal resistance (junction to case)		18.8	10.75	9.15	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [4]



Notes

3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High Z) for 10 ns parts are tested using the load conditions shown in Figure 3 (a). All other speeds are tested using the Thevenin load shown in Figure 3 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (d).

Switching Characteristics

Over the Operating Range

Parameter [5]	Description		-10		-12		-20		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle									
t_{power}[6]	V_{CC}(Typical) to the First Access		100	–	100	–	100	–	µs
t_{RC}	Read Cycle Time		10	–	12	–	20	–	ns
t_{AA}	Address to Data Valid		–	10	–	12	–	20	ns
t_{OHA}	Data Hold from Address Change		3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		–	10	–	12	–	20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	Auto-A	–	5	–	6	–	8	ns
		Auto-E	–	6	–	7	–	8	
t_{LZOE}	$\overline{OE}$ LOW to Low Z [7]		0	–	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [7, 8]		–	5	–	6	–	8	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [7]		3	–	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [7, 8]		–	5	–	6	–	8	ns
t_{PU}	$\overline{CE}$ LOW to Power Up		0	–	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		–	10	–	12	–	20	ns
t_{DBE}	Byte Enable to Data Valid	Auto-A	–	5	–	6	–	8	ns
		Auto-E	–	6	–	7	–	8	
t_{LZBE}	Byte Enable to Low Z		0	–	0	–	0	–	ns
t_{HZBE}	Byte Disable to High Z		–	6	–	6	–	8	ns
Write Cycle [9, 10]									
t_{WC}	Write Cycle Time		10	–	12	–	20	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End		7	–	8	–	10	–	ns
t_{AW}	Address Setup to Write End		7	–	8	–	10	–	ns
t_{HA}	Address Hold from Write End		0	–	0	–	0	–	ns
t_{SA}	Address Setup to Write Start		0	–	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width		7	–	8	–	10	–	ns
t_{SD}	Data Setup to Write End		5	–	6	–	8	–	ns
t_{HD}	Data Hold from Write End		0	–	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [7]		3	–	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [7, 8]		–	5	–	6	–	8	ns
t_{BW}	Byte Enable to End of Write		7	–	8	–	10	–	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
6. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
7. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
8. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 6. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
10. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

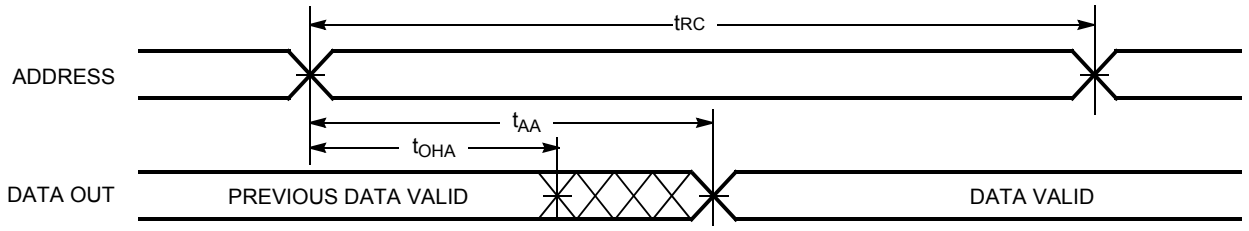
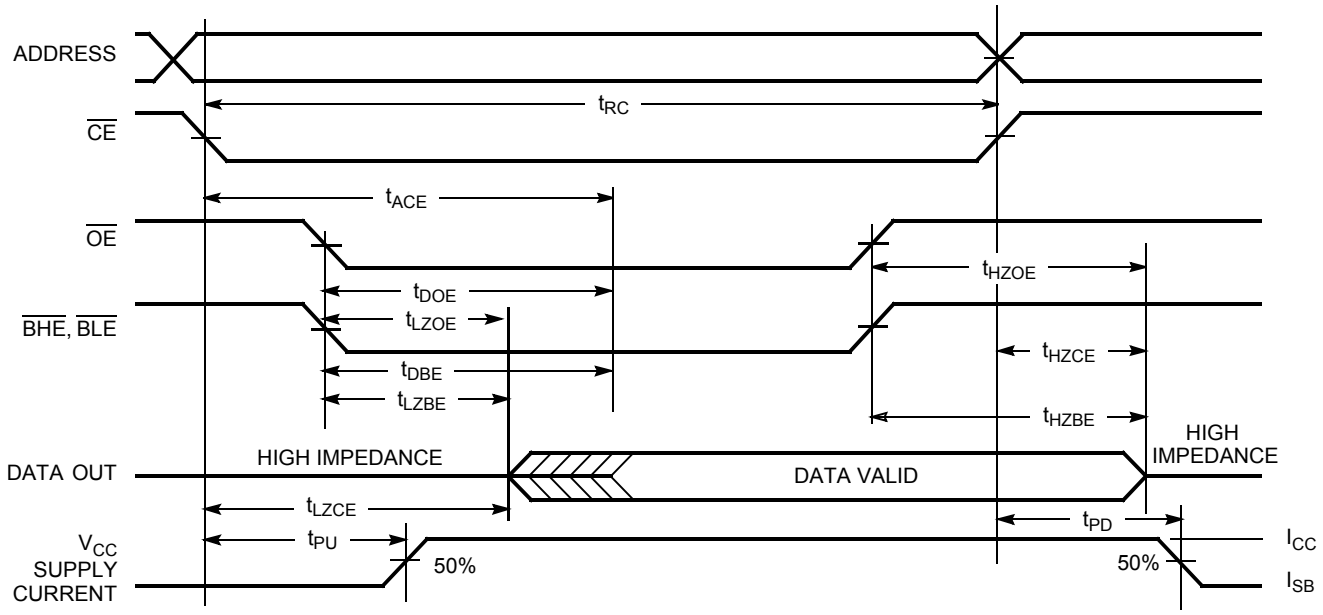


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]



Notes
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [14, 15]

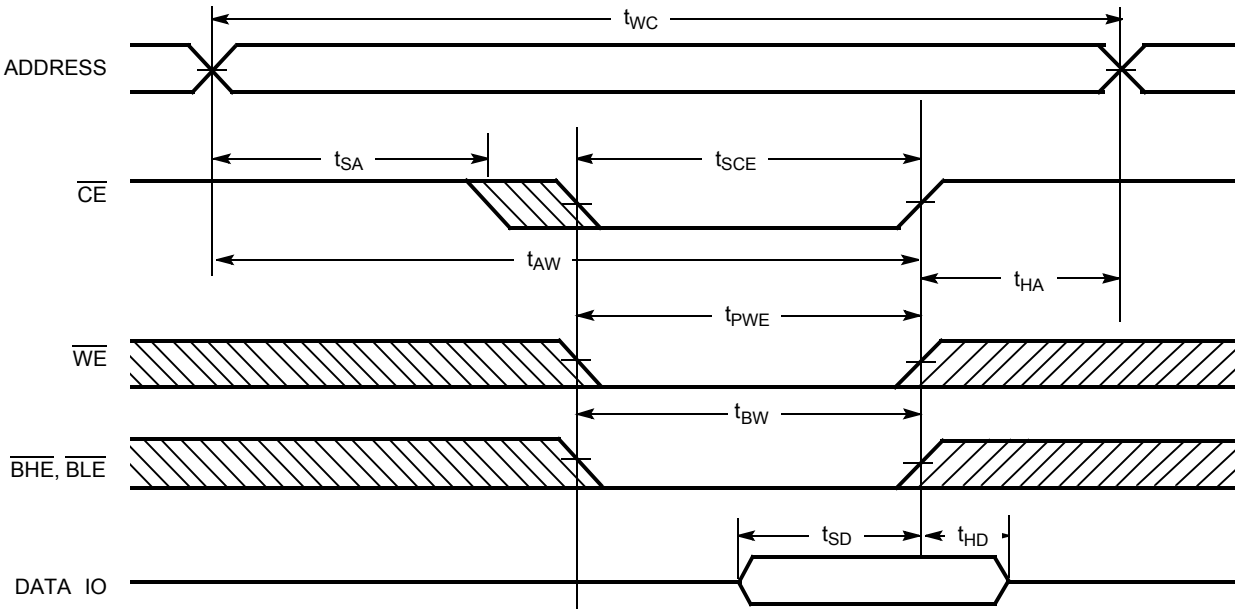
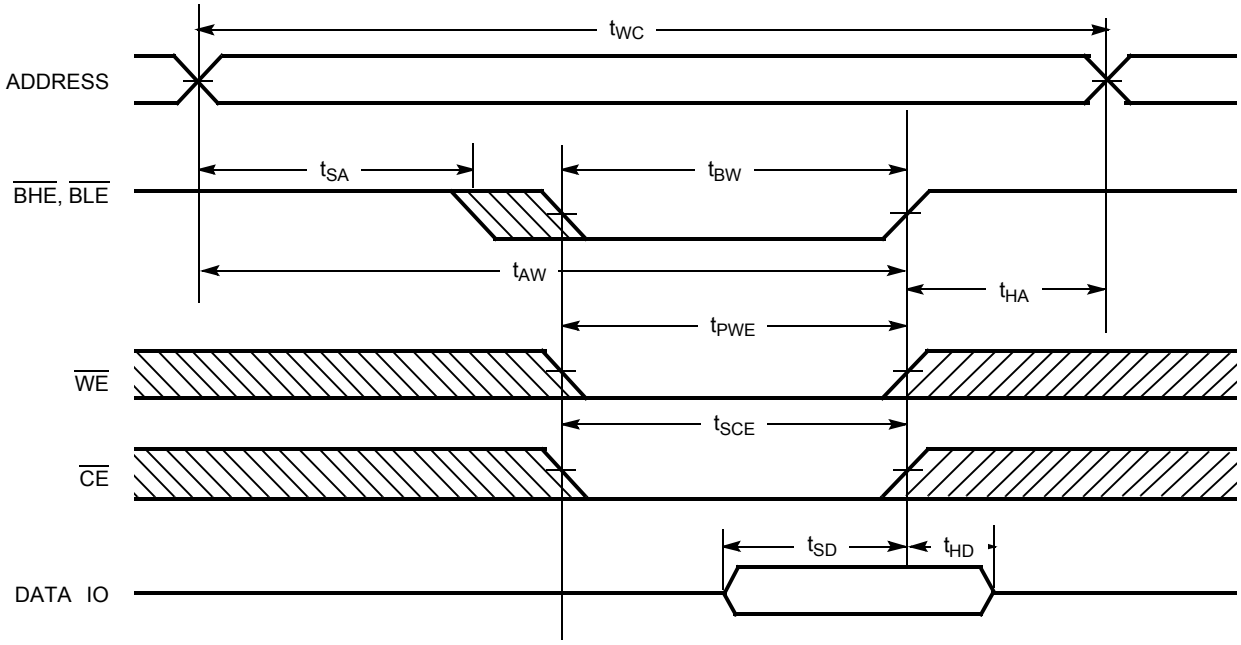


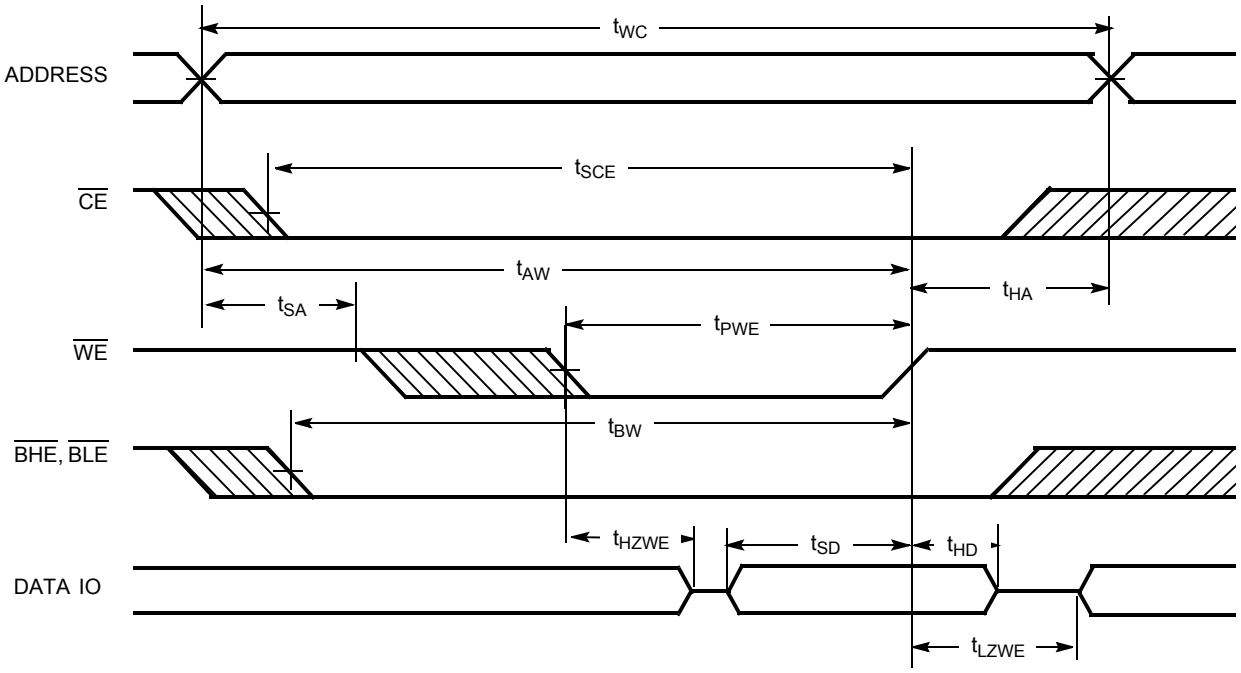
Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
14. Data IO is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All Bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All Bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

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Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available.For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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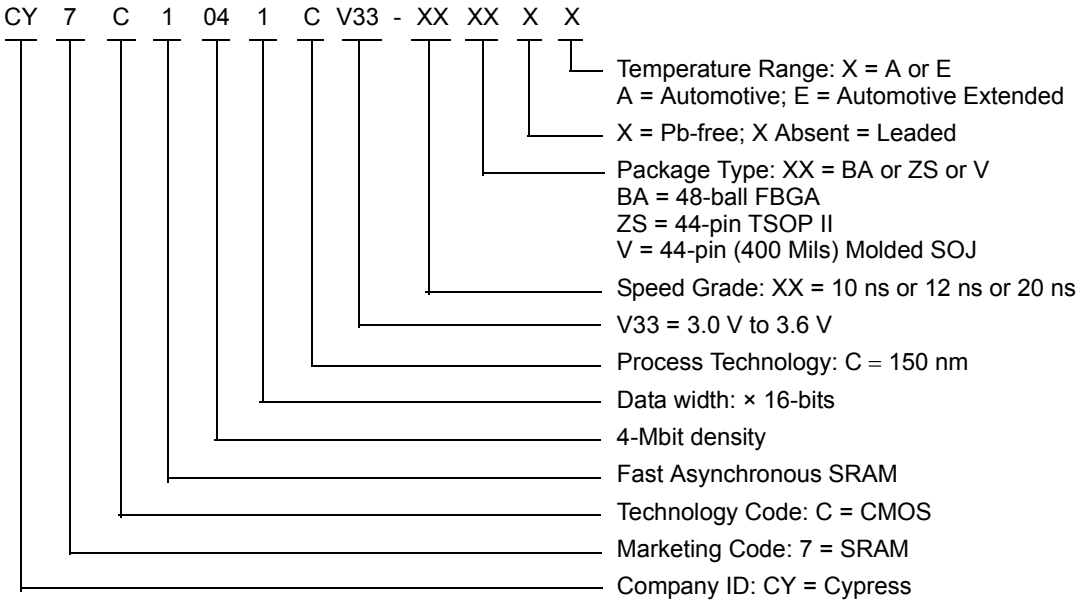
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1041CV33-10BAXA	51-85106	48-ball FBGA (Pb-free)	Automotive-A
	CY7C1041CV33-10ZSXA	51-85087	44-pin TSOP II (Pb-free)	
	CY7C1041CV33-10BAXE	51-85106	48-ball FBGA (Pb-free)	Automotive-E
12	CY7C1041CV33-12BAXE	51-85106	48-ball FBGA (Pb-free)	Automotive-E
	CY7C1041CV33-12ZSXE	51-85087	44-pin TSOP II (Pb-free)	
20	CY7C1041CV33-20ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
	CY7C1041CV33-20VXE		44-pin (400-mil) Molded SOJ (Pb-free)	Automotive-E
	CY7C1041CV33-20ZSXE		44-pin TSOP II (Pb-free)	

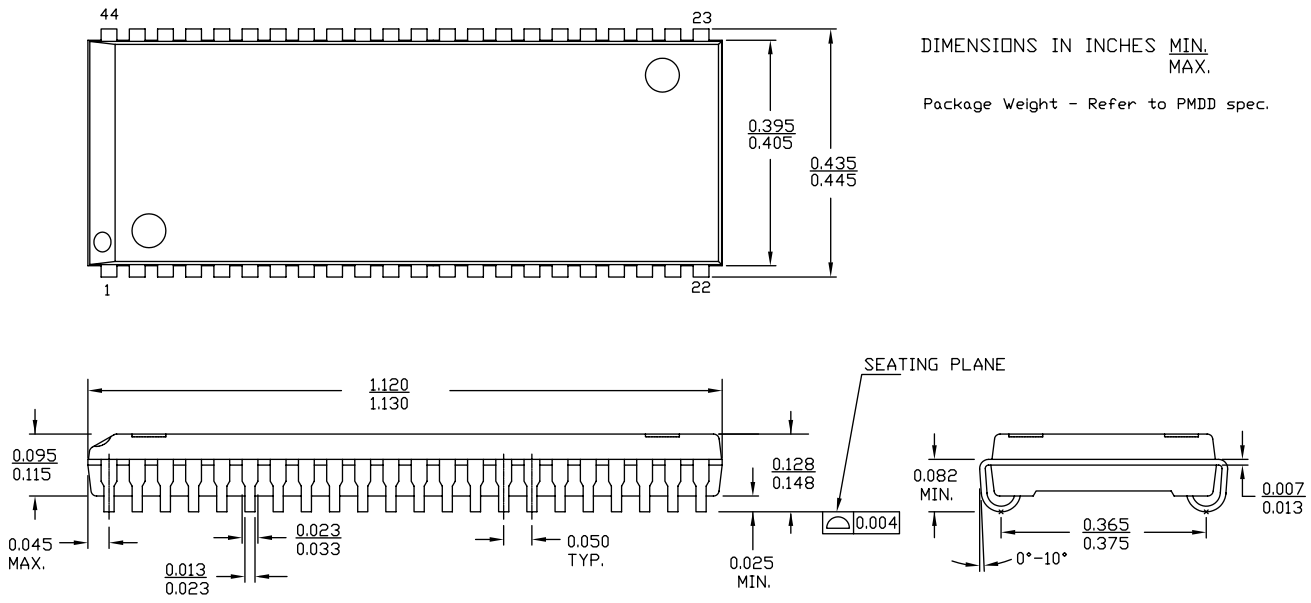
Please contact your local Cypress sales representative for availability of these parts

Ordering Code Definitions



Package Diagrams

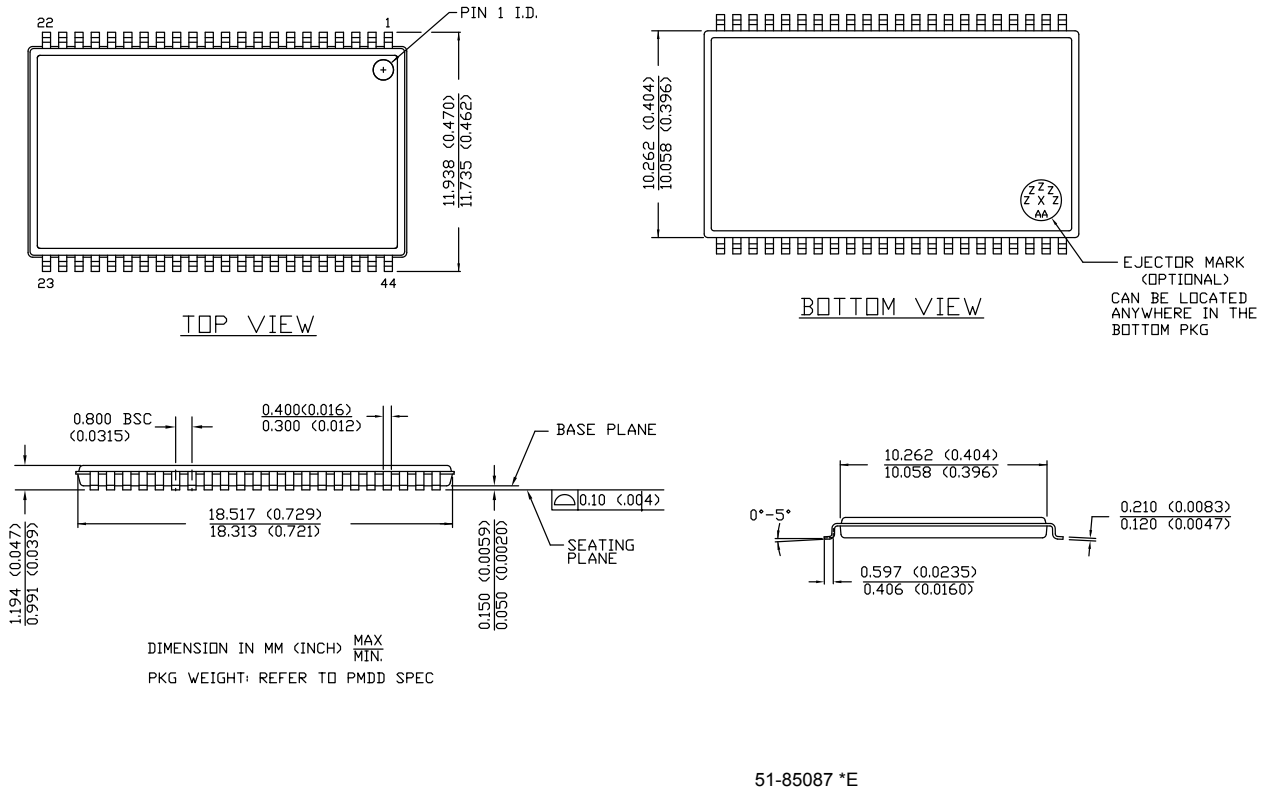
Figure 9. 44-pin SOJ 400 Mils V44.4 Package Outline, 51-85082



51-85082 *E

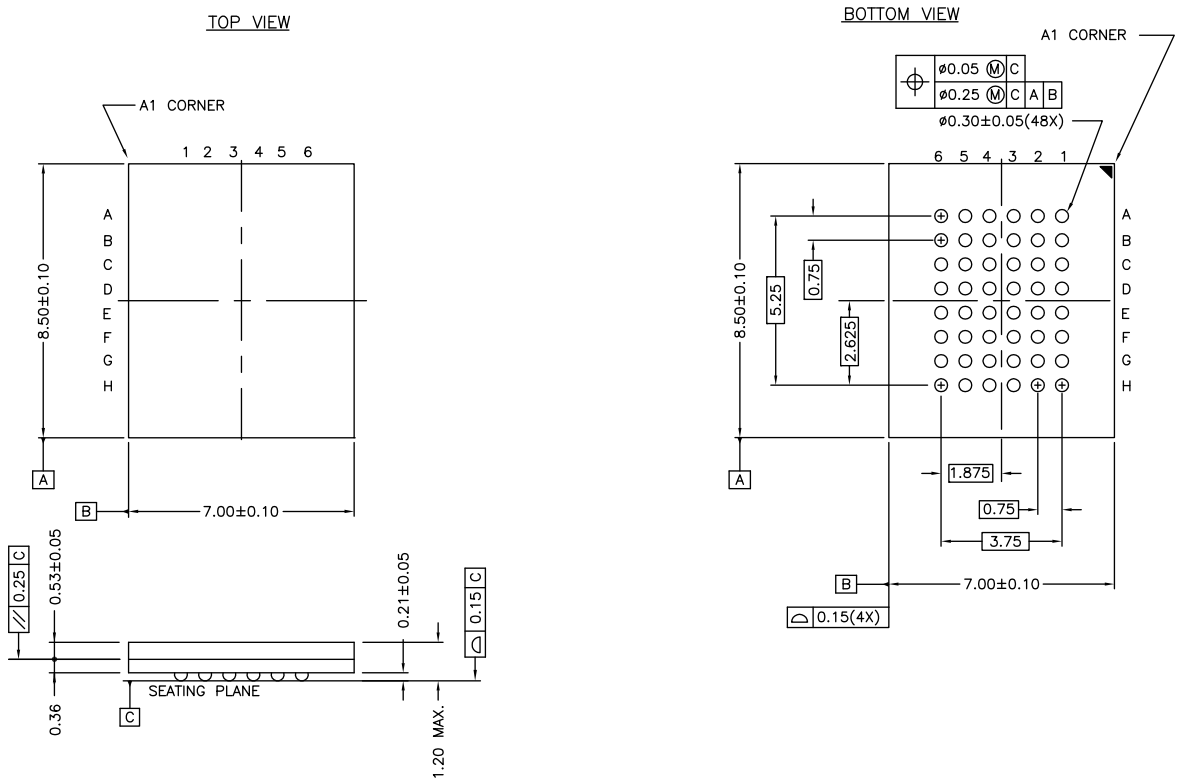
Package Diagrams *(continued)*

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



Package Diagrams *(continued)*

Figure 11. 48-ball FBGA (7.0 × 8.5 × 1.2 mm) BA48A Package Outline, 51-85106



51-85106 *G

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1041CV33 Automotive, 4-Mbit (256 K × 16) Static RAM Document Number: 001-67307				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	3187164	03/03/2011	PRAS	Separation of the automotive datasheet from CY7C1041CV33 spec no. 38-05134 Rev. *K. Further rev of 38-05134 would include only industrial / commercial parts.
*A	3265070	05/24/2011	PRAS	Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.").
*B	3507652	01/24/2012	TAVA	Updated Features. Updated Selection Guide. Updated Electrical Characteristics. Updated Switching Characteristics. Updated Ordering Information. Updated Package Diagrams.
*C	4318563	03/24/2014	VINI	Updated Package Diagrams: spec 51-85082 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.

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