

# NCP2821

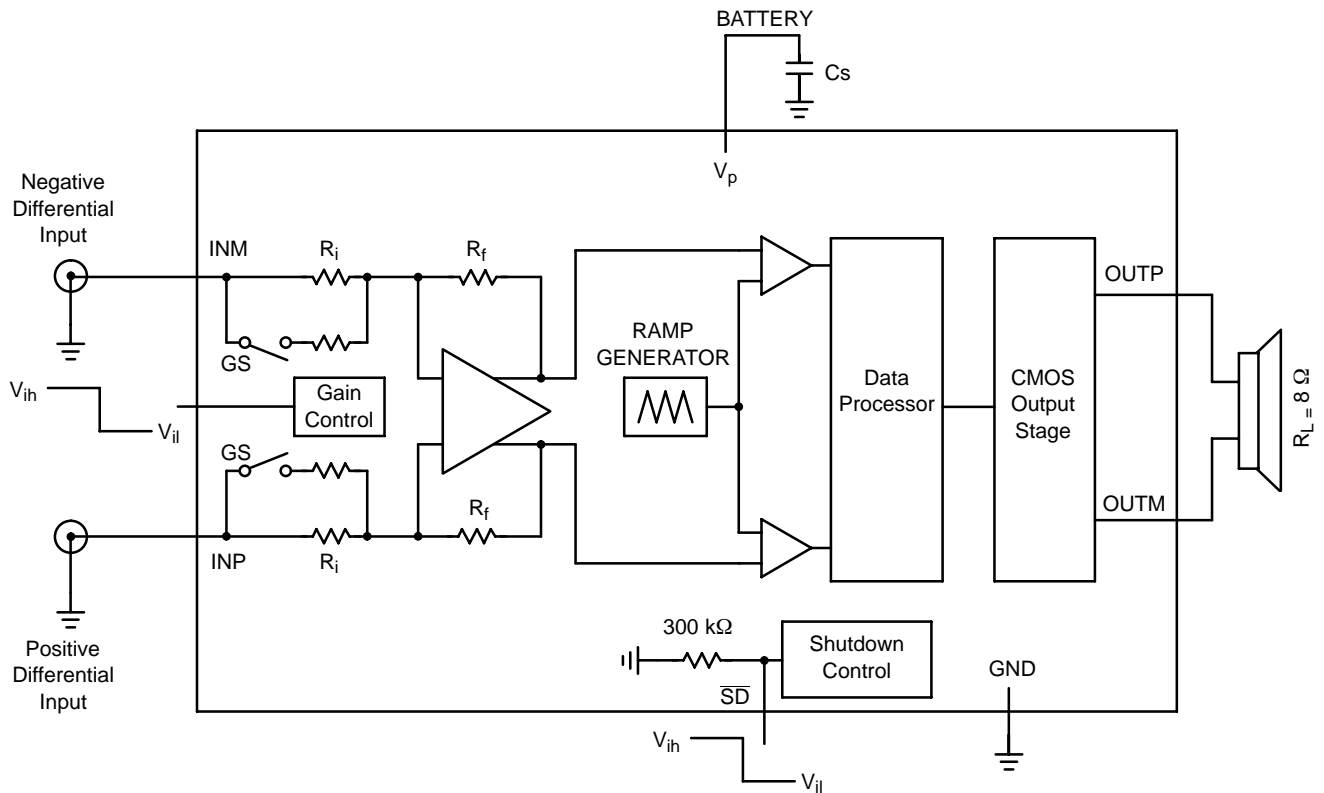


Figure 1. Typical Application

## PIN DESCRIPTION

Pin No.	Symbol	Type	Description
A1	INP	I	Positive Differential Input.
A2	GS	I	Gain Select Input.
A3	OUTM	O	Negative BTL Output.
B1	V <sub>p</sub>	I	Power Analog Positive Supply. Range: 2.5 V – 5.5 V.
B2	V <sub>p</sub>	I	Power Analog Positive Supply. Range: 2.5 V – 5.5 V.
B3	GND	I	Analog Ground.
C1	INM	I	Negative Differential Input.
C2	$\overline{SD}$	I	Shutdown Input.
C3	OUTP	O	Positive BTL Output.

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## MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Supply Voltage	$V_p$	6.0	V
Operating Supply Voltage	$O_p V_p$	2.5 to 5.5	V
Input Voltage	$V_{in}$	-0.3 to $V_p + 0.3$	V
Power Dissipation (Note 1)	$P_d$	Internally Limited	–
Operating Ambient Temperature	$T_A$	-40 to +85	°C
Max Junction Temperature	$T_J$	150	°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Thermal Resistance Junction-to-Air	$R_{\theta JA}$	90 (Note 2)	°C/W
ESD Protection			
Human Body Model (HBM) (Note 3)	–	> 2000	V
Machine Model (MM) (Note 4)	–	> 200	
Latchup Current @ $T_A = 85^\circ\text{C}$ (Note 5)	–	$\pm 100$	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. The thermal shutdown is set to 160°C (typical) avoiding irreversible damage to the device due to power dissipation.
2. For the 9-Pin Flip-Chip CSP package, the  $R_{\theta JA}$  is highly dependent of the PCB Heatsink area. For example,  $R_{\theta JA}$  can equal 195°C/W with 50 mm<sup>2</sup> total area and also 135°C/W with 500 mm<sup>2</sup>. When using ground and power planes, the value is around 90°C/W, as specified in table.
3. Human Body Model: 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
4. Machine Model: 200 pF discharged through all pins following specification JESD22/A115.
5. Latchup Testing per JEDEC Standard JESD78. SD and GS are qualified at 70 mA versus 100 mA for the other pins.

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## ELECTRICAL CHARACTERISTICS (Limits apply for $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit	
Operating Supply Voltage	$V_P$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	2.5	–	5.5	V	
Supply Quiescent Current	$I_{dd}$	$V_P = 3.6\text{ V}$ , $R_L = 8.0\ \Omega$	–	2.5	–	mA	
		$V_P = 5.5\text{ V}$ , No Load	–	3.1	–		
		$V_P$ from 2.5 V to 5.5 V, No Load	–	–	–		
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	–	–	4.5		
Shutdown Current	$I_{sd}$	$V_P = 4.2\text{ V}$ , $T_A = +25^\circ\text{C}$	–	0.5	–	$\mu\text{A}$	
		$V_P = 5.5\text{ V}$ , $T_A = +25^\circ\text{C}$	–	0.8	–	$\mu\text{A}$	
		$V_P = 2.5\text{ V}$ to $5.5\text{ V}$	–	–	–		
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	–	–	1.4		
SD Voltage High	$V_{sdih}$		1.2	–	–	V	
SD Voltage Low	$V_{sdil}$		–	–	0.4	V	
GS Voltage High	$V_{gsih}$		1.2	–	–	V	
GS Voltage Low	$V_{gsil}$		–	–	0.4	V	
Differential Input Resistance	$R_{in}$	G = 6 dB	–	150	–	k $\Omega$	
		G = 12 dB	–	75	–	k $\Omega$	
Switching Frequency	$F_{SW}$	$V_P = 2.5\text{ V}$ to $5.5\text{ V}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	200	250	300	kHz	
Gain	G	$R_L = 8.0\ \Omega$ , $V_{GS} = \text{High}$	5.5	6	6.5	dB	
		$R_L = 8.0\ \Omega$ , $V_{GS} = \text{Low}$	11.5	12	12.5	dB	
Resistance from SD to Gnd	$R_{SD}$		200	300	–	k $\Omega$	
Output Offset Voltage	$V_{os}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	–25	2.5	+25	mV	
Turn On Time	$T_{ON}$	$V_P = 2.5\text{ V}$ to $5.5\text{ V}$	–	9	–	ms	
Turn Off Time	$T_{OFF}$	$V_P = 2.5\text{ V}$ to $5.5\text{ V}$	–	5	–	ms	
Thermal Shutdown Temperature	$T_{sd}$		–	160	–	$^\circ\text{C}$	
Output Noise Voltage	$V_n$	$V_P = 3.6\text{ V}$	–	–	–	$\mu\text{Vrms}$	
		F = 20kHz to 20kHz	–	63	–		
		No weighting filter	–	–	–		
		A weighting filter	–	40	–		
RMS Output Power	$P_o$	$R_L = 8\ \Omega$ , f = 1 kHz, THD+N < 1%	$V_P = 2.5\text{ V}$	–	0.32	–	W
			$V_P = 3.0\text{ V}$	–	0.48	–	
			$V_P = 3.6\text{ V}$	–	0.7	–	
			$V_P = 4.2\text{ V}$	–	0.97	–	
			$V_P = 5.0\text{ V}$	–	1.38	–	
			$R_L = 8\ \Omega$ , f = 1 kHz, THD+N < 10%	–	0.4	–	W
		$V_P = 2.5\text{ V}$	–	0.59	–		
		$V_P = 3.0\text{ V}$	–	0.87	–		
		$V_P = 4.2\text{ V}$	–	1.19	–		
		$V_P = 5.0\text{ V}$	–	1.7	–		
RMS Output Power	$P_o$	$R_L = 4\ \Omega$ , f = 1 kHz, THD+N < 1%	$V_P = 2.5\text{ V}$	–	0.49	–	W
			$V_P = 3.0\text{ V}$	–	0.72	–	
			$V_P = 3.6\text{ V}$	–	1.06	–	
			$V_P = 4.2\text{ V}$	–	1.62	–	
			$V_P = 5.0\text{ V}$	–	2.12	–	
			$R_L = 4\ \Omega$ , f = 1 kHz, THD+N < 10%	–	0.6	–	W
		$V_P = 2.5\text{ V}$	–	0.9	–		
		$V_P = 3.0\text{ V}$	–	1.33	–		
		$V_P = 4.2\text{ V}$	–	2.0	–		
		$V_P = 5.0\text{ V}$	–	2.65	–		

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## ELECTRICAL CHARACTERISTICS (Limits apply for $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise	THD+N	$V_p = 5.0\text{ V}$ , $R_L = 8\ \Omega$ , $f = 1\text{ kHz}$ , $P_{out} = 0.25\text{ W}$	-	0.05	-	%
		$V_p = 3.6\text{ V}$ , $R_L = 8\ \Omega$ , $f = 1\text{ kHz}$ , $P_{out} = 0.25\text{ W}$	-	0.09	-	%
Efficiency	$\eta$	$R_L = 8\ \Omega$ , $f = 1\text{ kHz}$ $V_p = 5\text{ V}$ , $P_{out} = 1.2\text{ W}$ $V_p = 3.6\text{ V}$ , $P_{out} = 600\text{ mW}$	-	91	-	%
		$R_L = 4\ \Omega$ , $f = 1\text{ kHz}$ $V_p = 5\text{ V}$ , $P_{out} = 2\text{ W}$ $V_p = 3.6\text{ V}$ , $P_{out} = 600\text{ mW}$	-	82	-	%
Common Mode Rejection Ratio	CMRR	$V_p = 2.5\text{ V to } 5.5\text{ V}$ , $G = 6\text{ dB}$ $V_{ic} = 0.5\text{ V to } V_p - 0.8\text{ V}$ $V_p = 3.6\text{ V}$ , $V_{ic} = 1\text{ V}_{pp}$ $G = 6\text{ dB}$ , $f = 1\text{ kHz}$		-62		dB
		$G = 6\text{ dB}$ , $f = 1\text{ kHz}$		-59		dB
		$G = 12\text{ dB}$ , $f = 1\text{ kHz}$		-53		dB
Power Supply Rejection Ratio	PSRR	$V_{ripple\_pk-pk} = 200\text{ mV}$ , $R_L = 8\ \Omega$ , Inputs AC grounded, $V_p = 3.6\text{ V}$ $f = 217\text{ Hz}$ $f = 1\text{ kHz}$	-	-63	-	dB

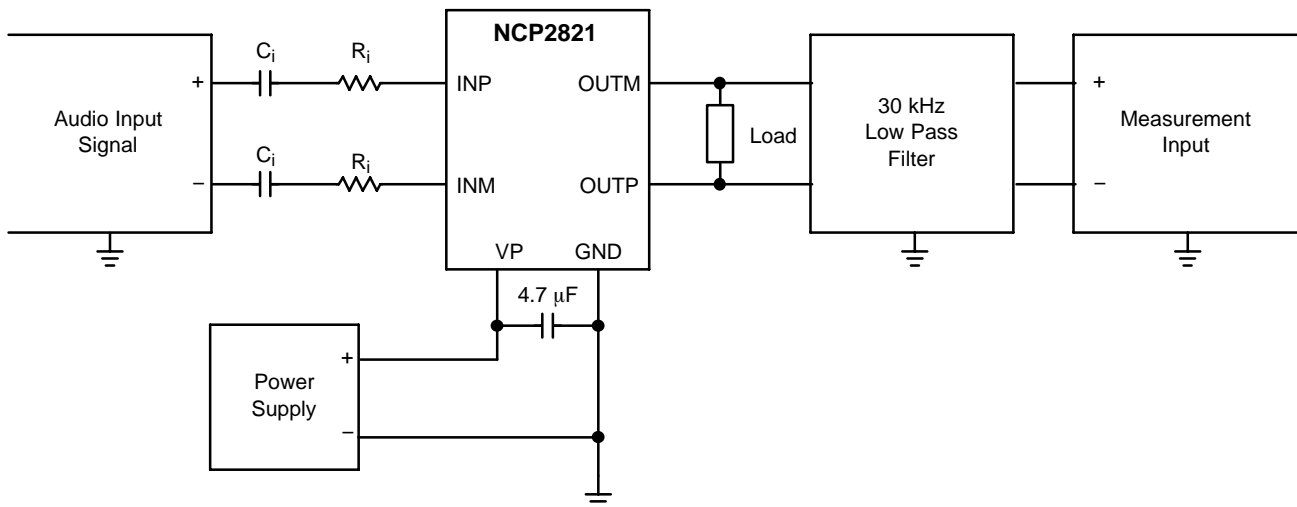


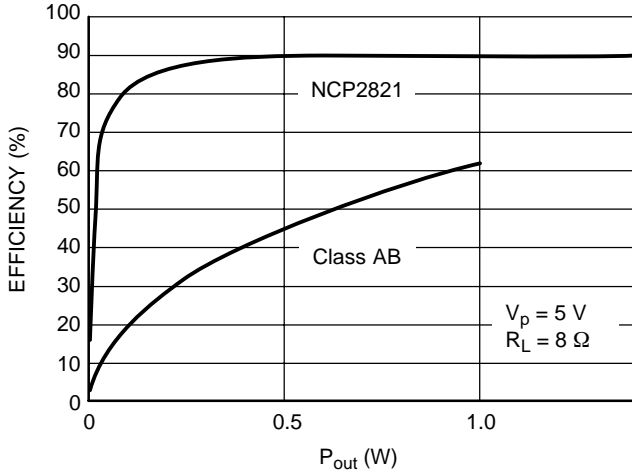
Figure 2. Test Setup for Graphs

### NOTES:

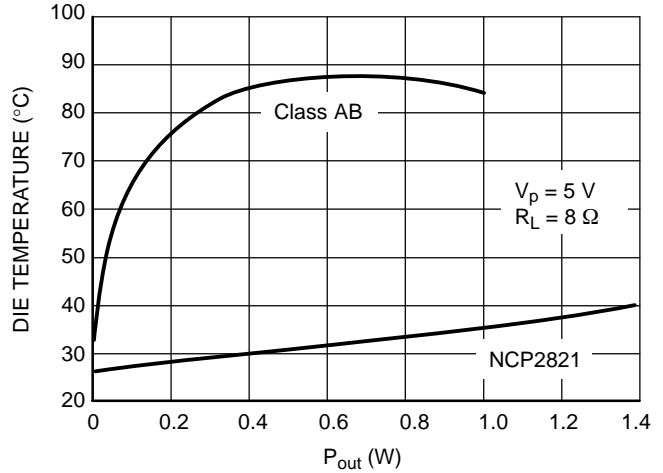
- Unless otherwise noted,  $C_i = 100\text{ nF}$  and  $R_i = 150\text{ k}\Omega$ . Thus, the gain setting is  $2\text{ V/V}$  and the cutoff frequency of the input high pass filter is set to  $10\text{ Hz}$ . Input capacitors are shorted for CMRR measurements.
- To closely reproduce a real application case, all measurements are performed using the following loads:  
 $R_L = 8\ \Omega$  means Load =  $15\ \mu\text{H} + 8\ \Omega + 15\ \mu\text{H}$   
 $R_L = 4\ \Omega$  means Load =  $15\ \mu\text{H} + 4\ \Omega + 15\ \mu\text{H}$   
 Very low DCR  $15\ \mu\text{H}$  inductors ( $50\text{ m}\Omega$ ) have been used for the following graphs. Thus, the electrical load measurements are performed on the resistor ( $8\ \Omega$  or  $4\ \Omega$ ) in differential mode.
- For Efficiency measurements, the optional  $30\text{ kHz}$  filter is used. An RC low-pass filter is selected with ( $100\ \Omega$ ,  $47\text{ nF}$ ) on each PWM output.

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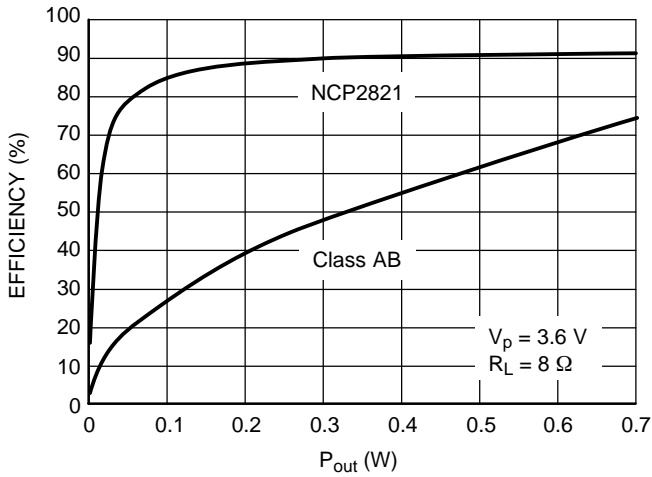
## TYPICAL CHARACTERISTICS



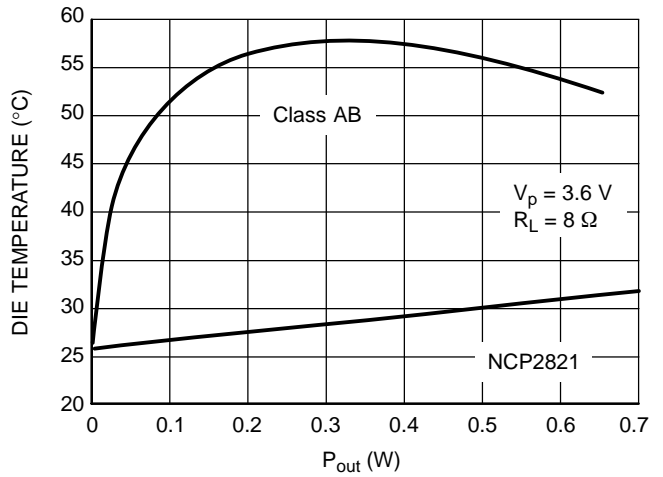
**Figure 3. Efficiency vs.  $P_{out}$**   
 $V_p = 5\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$



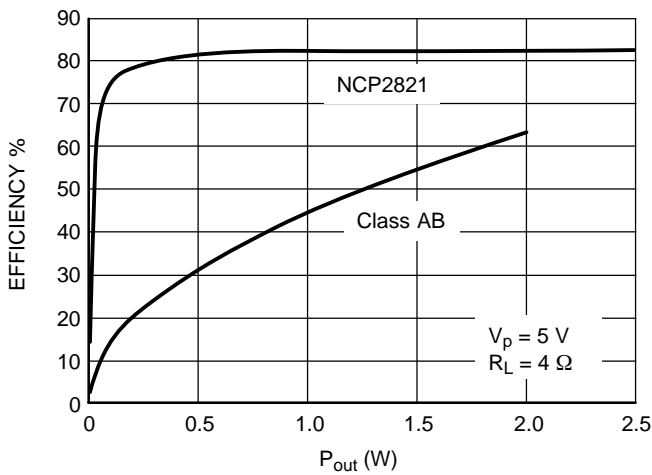
**Figure 4. Die Temperature vs.  $P_{out}$**   
 $V_p = 5\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$  @  $T_A = +25^\circ\text{C}$



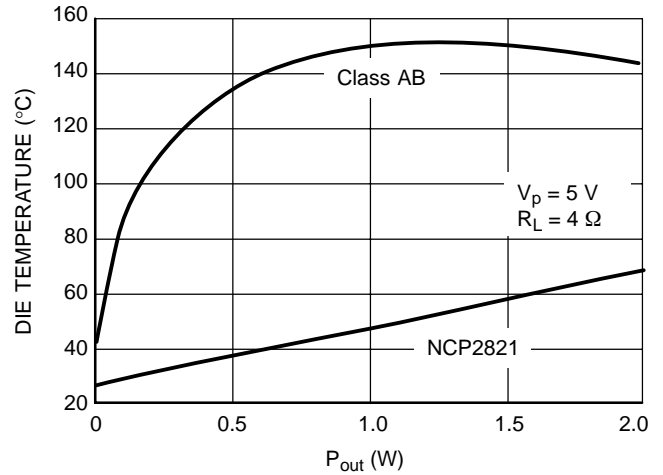
**Figure 5. Efficiency vs.  $P_{out}$**   
 $V_p = 3.6\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$



**Figure 6. Die Temperature vs.  $P_{out}$**   
 $V_p = 3.6\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$  @  $T_A = +25^\circ\text{C}$



**Figure 8. Efficiency vs.  $P_{out}$**   
 $V_p = 5\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$



**Figure 7. Die Temperature vs.  $P_{out}$**   
 $V_p = 5\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$  @  $T_A = +25^\circ\text{C}$

TYPICAL CHARACTERISTICS

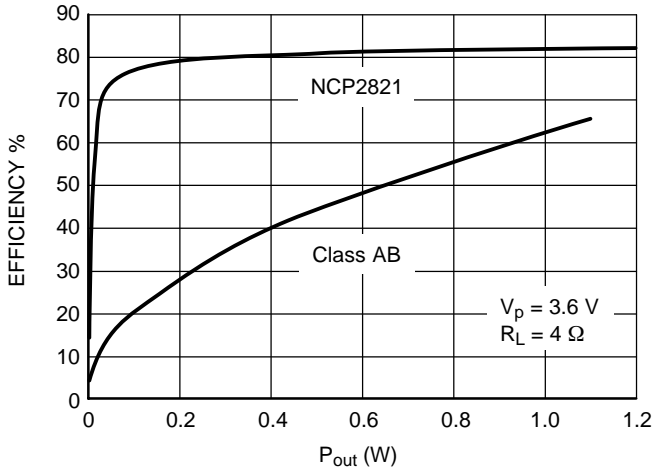


Figure 9. Efficiency vs.  $P_{out}$   
 $V_p = 3.6\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$

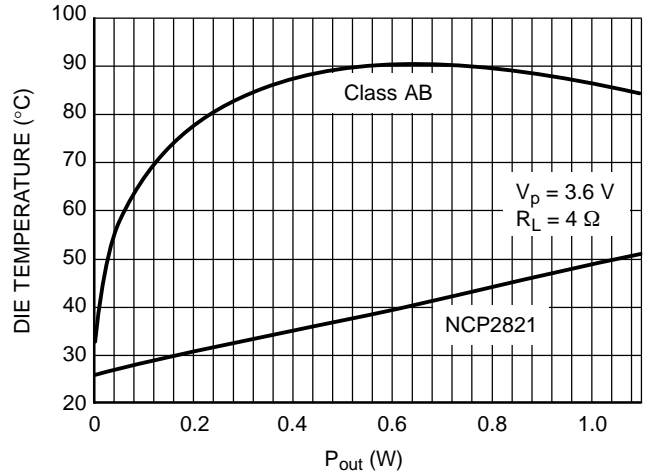


Figure 10. Die Temperature vs.  $P_{out}$   
 $V_p = 3.6\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$  @  $T_A = +25^\circ\text{C}$

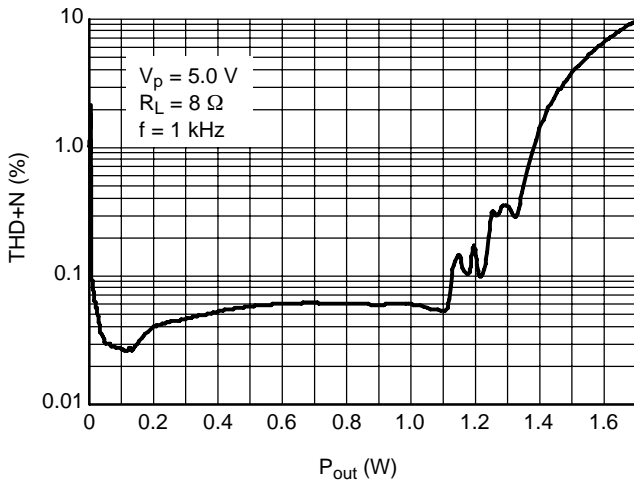


Figure 11. THD+N vs.  $P_{out}$   
 $V_p = 5\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$

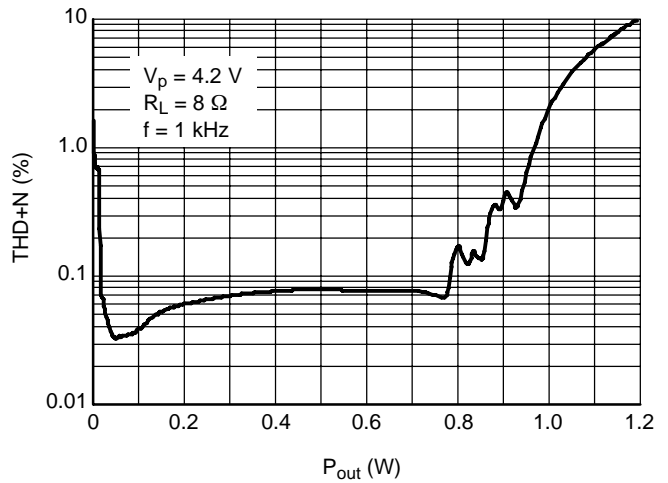


Figure 12. THD+N vs.  $P_{out}$   
 $V_p = 4.2\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$

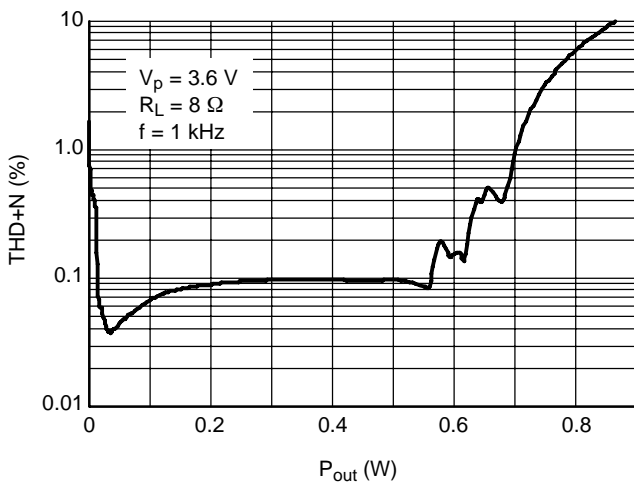


Figure 13. THD+N vs.  $P_{out}$   
 $V_p = 3.6\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$

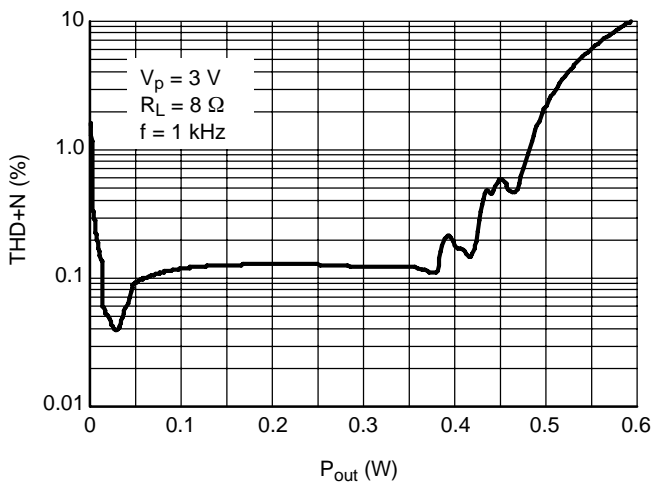


Figure 14. THD+N vs.  $P_{out}$   
 $V_p = 3\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$

TYPICAL CHARACTERISTICS

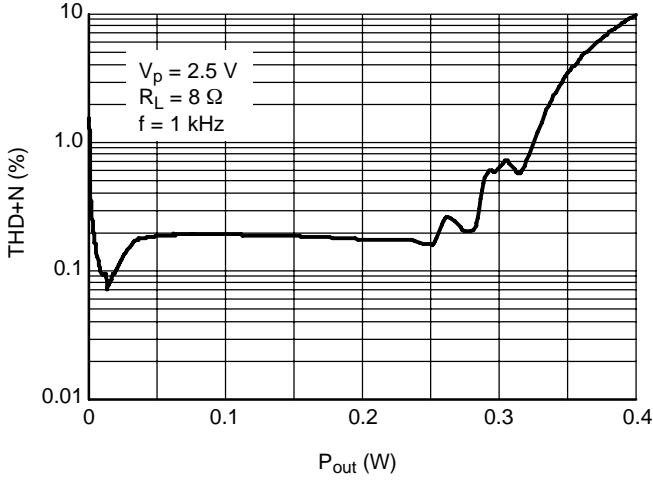


Figure 15. THD+N vs. Pout  
 $V_p = 2.5\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $f = 1\text{ kHz}$

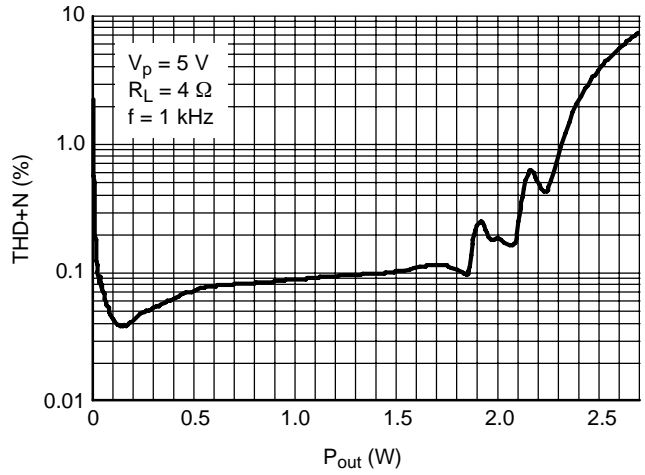


Figure 16. THD+N vs. Pout  
 $V_p = 5\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$

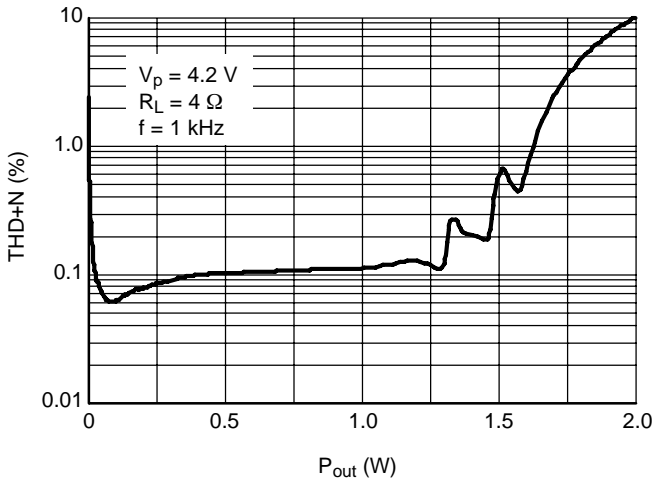


Figure 17. THD+N vs. Pout  
 $V_p = 4.2\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$

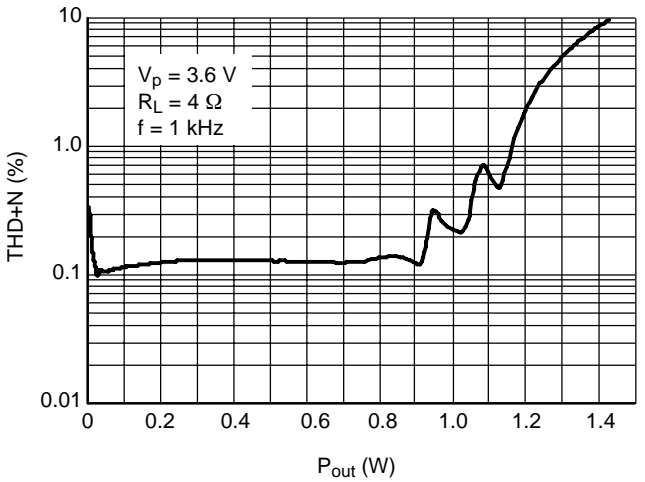


Figure 18. THD+N vs. Pout  
 $V_p = 3.6\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$

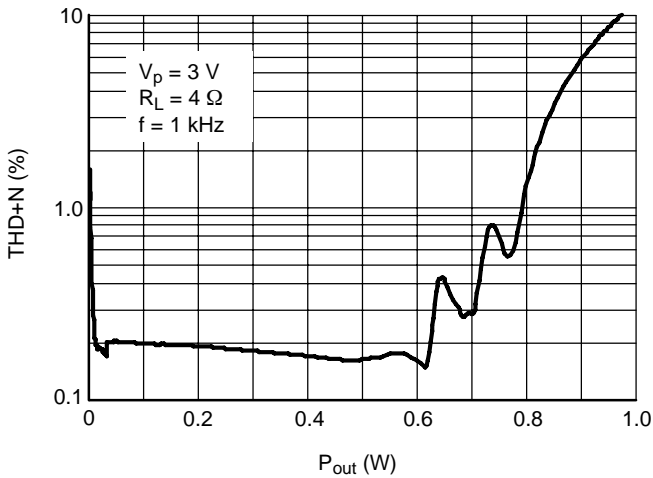


Figure 19. THD+N vs. Power Out  
 $V_p = 3\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$

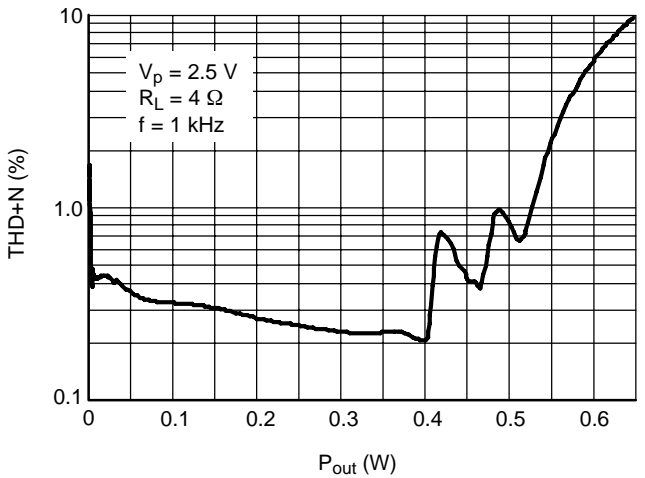


Figure 20. THD+N vs. Power Out  
 $V_p = 2.5\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$

TYPICAL CHARACTERISTICS

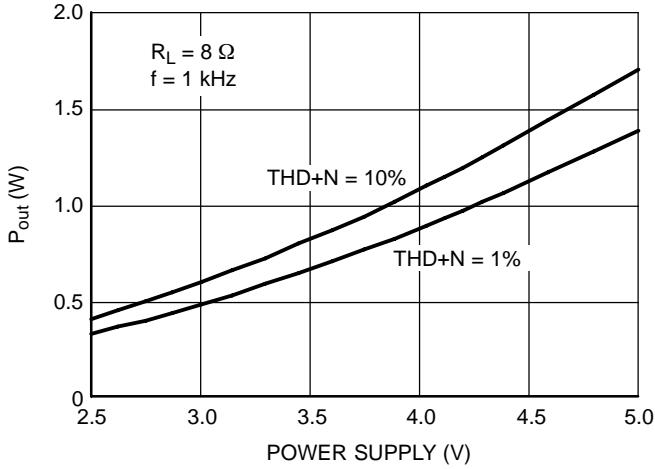


Figure 21. Output Power vs. Power Supply  
 $R_L = 8 \Omega$  @  $f = 1 \text{ kHz}$

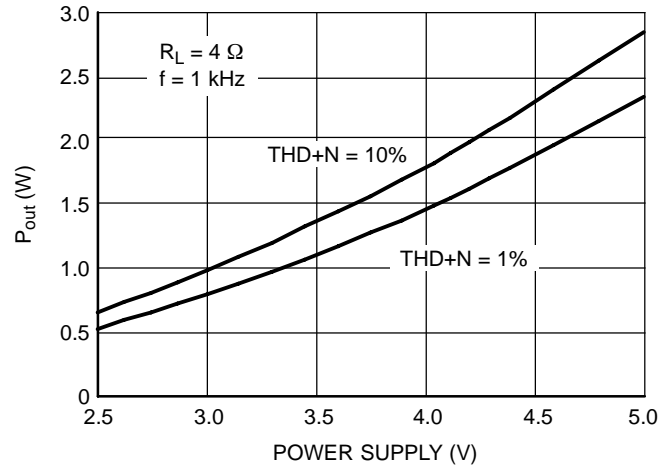


Figure 22. Output Power vs. Power Supply  
 $R_L = 4 \Omega$  @  $f = 1 \text{ kHz}$

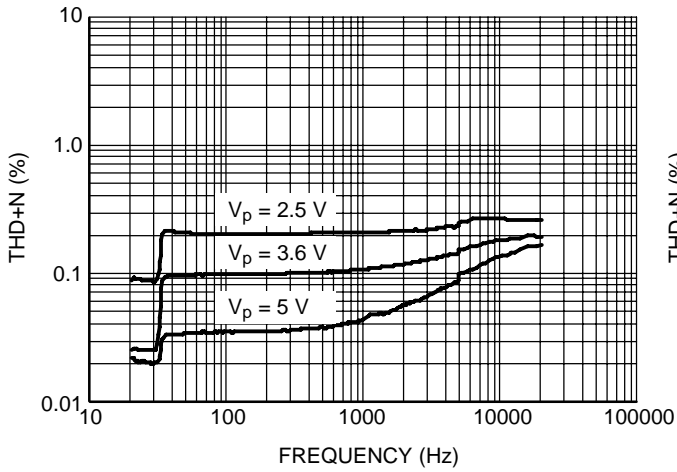


Figure 23. THD+N vs. Frequency  
 $R_L = 8 \Omega$ ,  $P_{out} = 250 \text{ mW}$  @  $f = 1 \text{ kHz}$

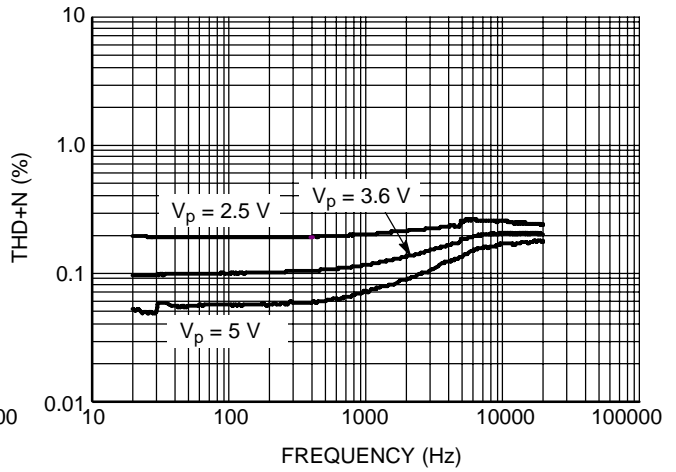


Figure 24. THD+N vs. Frequency  
 $R_L = 4 \Omega$ ,  $P_{out} = 250 \text{ mW}$  @  $f = 1 \text{ kHz}$

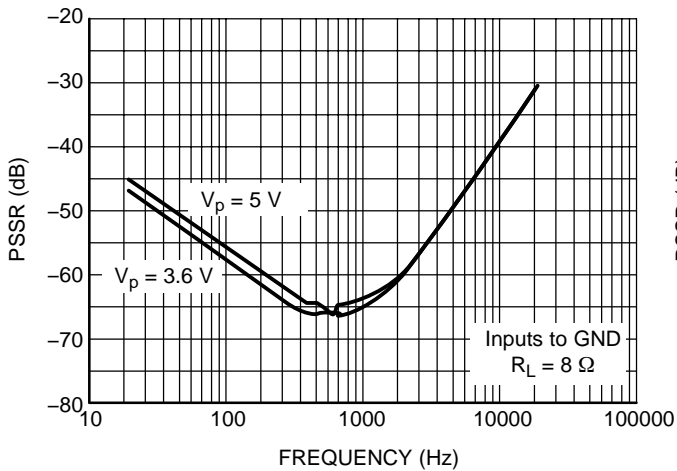


Figure 25. PSRR vs. Frequency  
 Inputs Grounded,  $R_L = 8 \Omega$ , Vripple = 200 mVpkpk

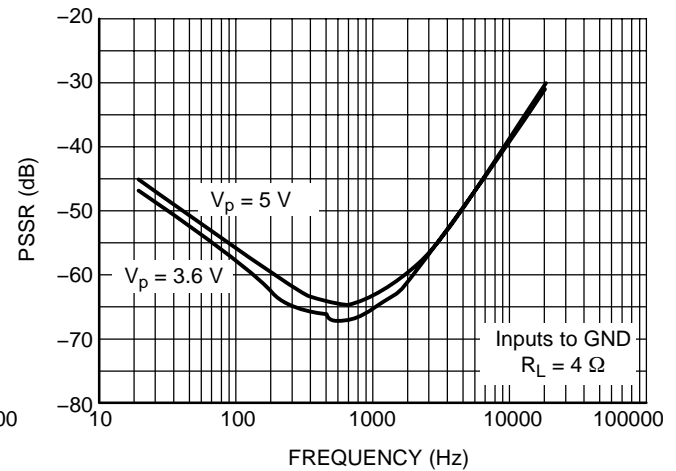


Figure 26. PSRR vs. Frequency  
 Inputs grounded,  $R_L = 4 \Omega$ , Vripple = 200 mVpkpk



TYPICAL CHARACTERISTICS

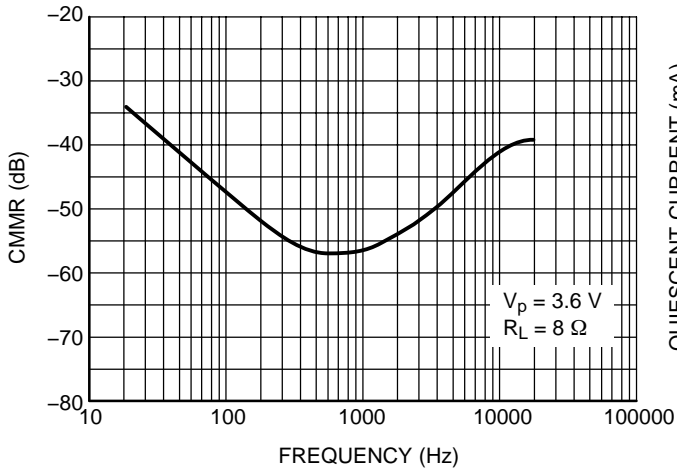


Figure 27. PSRR vs. Frequency  
 $V_p = 3.6\text{ V}$ ,  $R_L = 8\ \Omega$ ,  $V_{ic} = 200\text{ mvpkpk}$

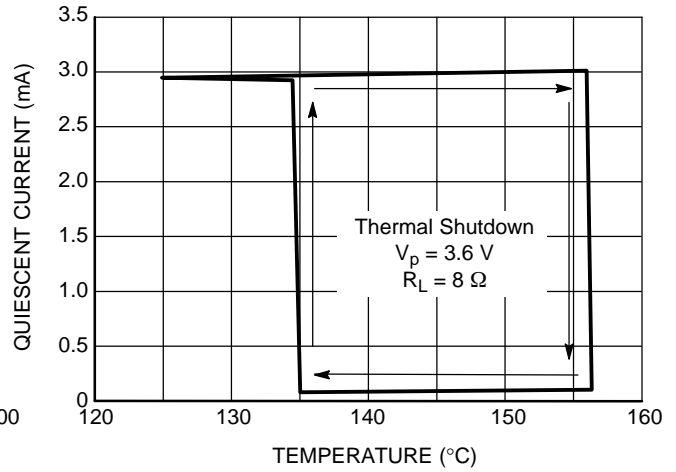


Figure 28. Thermal Shutdown vs. Temperature  
 $V_p = 5\text{ V}$ ,  $R_L = 8\ \Omega$ ,

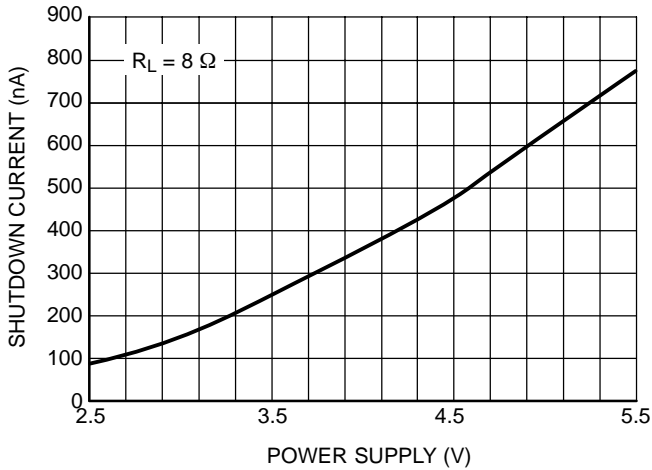


Figure 29. Shutdown Current vs. Power Supply  
 $R_L = 8\ \Omega$

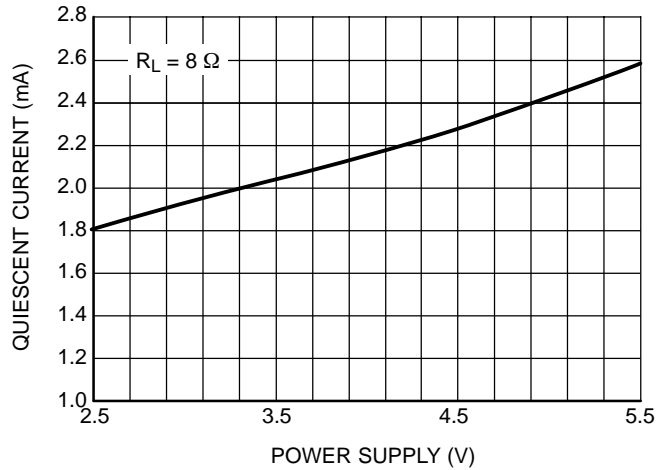


Figure 30. Quiescent Current vs. Power Supply  
 $R_L = 8\ \Omega$

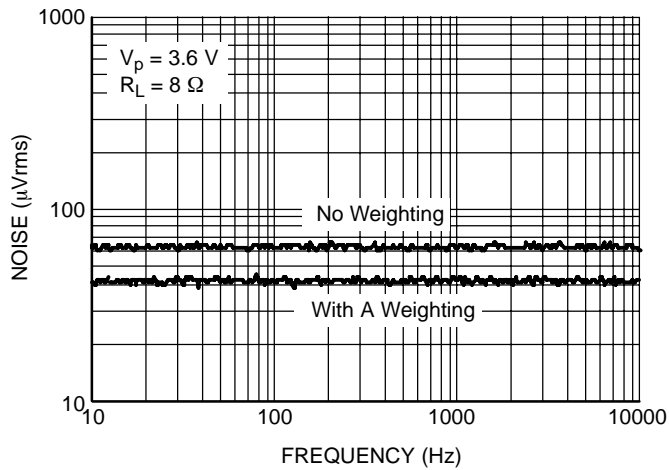


Figure 31. Noise Floor, Inputs AC Grounded  
 with  $1\ \mu\text{F}$   $V_p = 3.6\text{ V}$

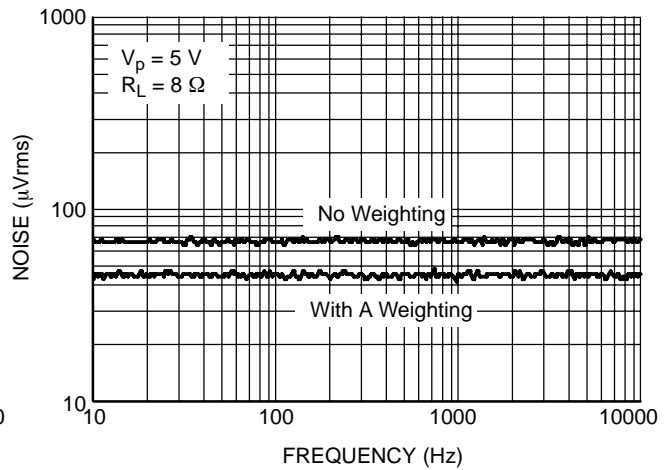


Figure 32. Noise Floor, Inputs AC Grounded  
 with  $1\ \mu\text{F}$   $V_p = 5\text{ V}$

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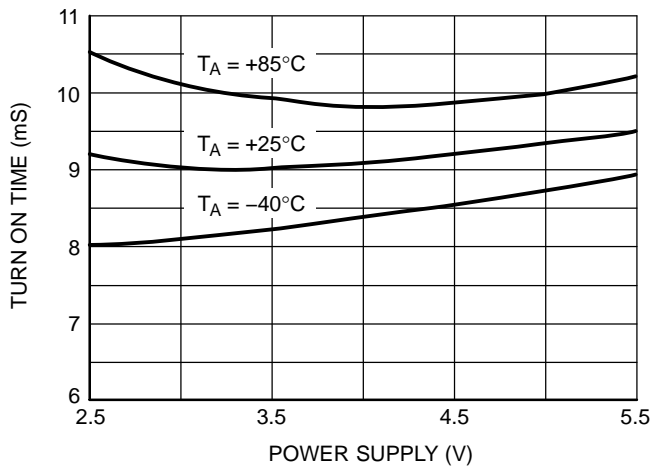


Figure 33. Turn on Time

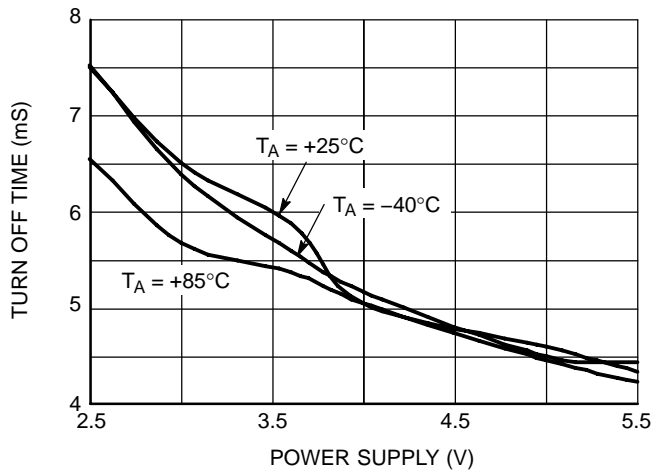


Figure 34. Turn off Time

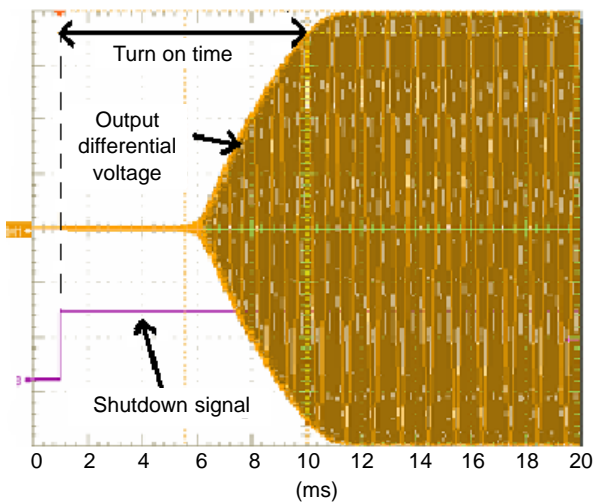


Figure 35. Turn on sequence  
 $V_p = 3.6\text{ V}$ ,  $R_L = 8\ \Omega$

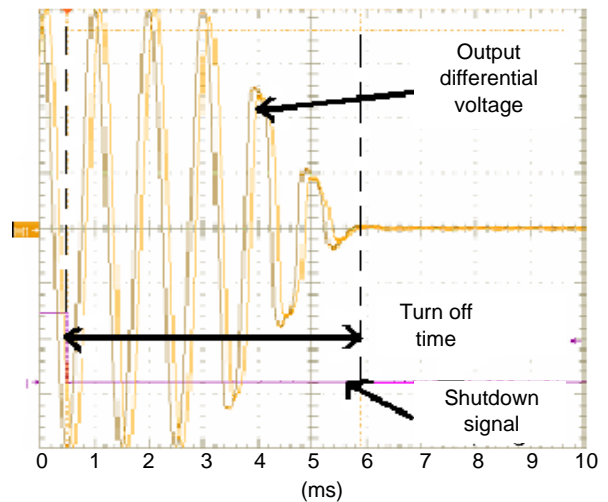


Figure 36. Turn off sequence  
 $V_p = 3.6\text{ V}$ ,  $R_L = 8\ \Omega$

## DESCRIPTION INFORMATION

### Detailed Description

The basic structure of the NCP2821 is composed of one analog pre-amplifier, a pulse width modulator and an H-bridge CMOS power stage. The first stage is externally configurable with gain-setting resistor  $R_i$  and the internal fixed feedback resistor  $R_f$  (the closed-loop gain is fixed by the ratios of these resistors) and the other stage is fixed. The load is driven differentially through two output stages.

The differential PWM output signal is a digital image of the analog audio input signal. The human ear is a band pass filter regarding acoustic waveforms, the typical values of which are 20 Hz and 20 kHz. Thus, the user will hear only the amplified audio input signal within the frequency range. The switching frequency and its harmonics are fully filtered. The inductive parasitic element of the loudspeaker helps to guarantee a superior distortion value.

### Power Amplifier

The output PMOS and NMOS transistors of the amplifier have been designed to deliver the output power of the specifications without clipping. The channel resistance ( $R_{on}$ ) of the NMOS and PMOS transistors is typically 0.3  $\Omega$ .

### Turn On and Turn Off Transitions

In order to eliminate “pop and click” noises during transition, the output power in the load must not be established or cutoff suddenly. When a logic high is applied to the shutdown pin, the internal biasing voltage rises quickly and, 4 ms later, once the output DC level is around the common mode voltage, the gain is established slowly

(5.0 ms). This method to turn on the device is optimized in terms of rejection of “pop and click” noises. Thus, the total turn on time to get full power to the load is 9 ms (typical) (see Figure 35).

The device has the same behavior when it is turned-off by a logic low on the shutdown pin. No power is delivered to the load 5 ms after a falling edge on the shutdown pin (see Figure 36). Due to the fast turn on and off times, the shutdown signal can be used as a mute signal as well.

### Shutdown Function

The device enters shutdown mode when the shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 1.5  $\mu$ A.

### Current Breaker Circuit

The maximum output power of the circuit corresponds to an average current in the load of 820 mA.

In order to limit the excessive power dissipation in the load if a short-circuit occurs, a current breaker cell shuts down the output stage. The current in the four output MOS transistors are real-time controlled, and if one current exceeds the threshold set to 1.5 A, the MOS transistor is opened and the current is reduced to zero. As soon as the short-circuit is removed, the circuit is able to deliver the expected output power.

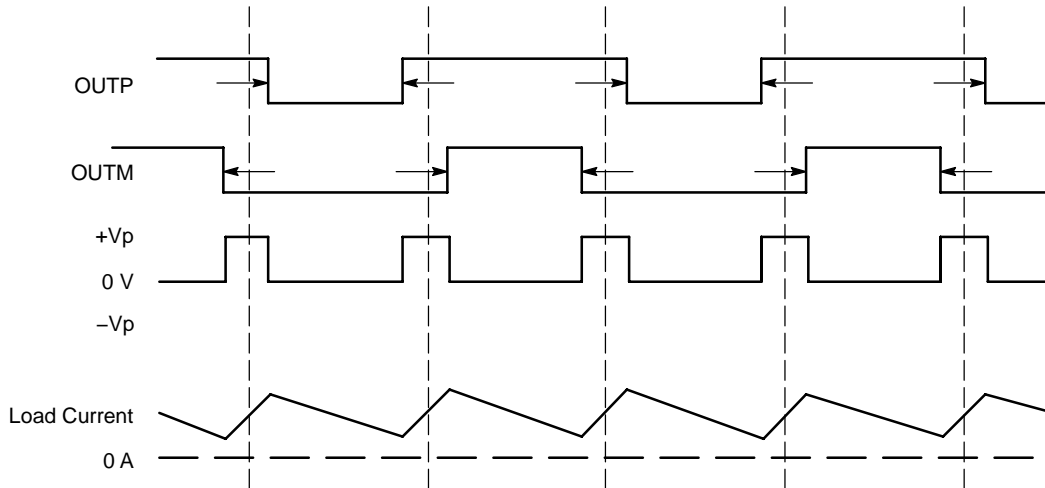
This patented structure protects the NCP2821. Since it completely turns off the load, it minimizes the risk of the chip overheating which could occur if a soft current limiting circuit was used.

## APPLICATION INFORMATION

**NCP2821 PWM Modulation Scheme**

The NCP2821 uses a PWM modulation scheme with each output switching from 0 to the supply voltage. If  $V_{in} = 0$  V outputs OUTM and OUTP are in phase and no current is flowing through the differential load. When a positive signal

is applied, OUTP duty cycle is greater than 50% and OUTM is less than 50%. With this configuration, the current through the load is 0 A most of the switching period and thus power losses in the load are lowered.



**Figure 37. Output Voltage and Current Waveforms into an Inductive Loudspeaker DC Output Positive Voltage Configuration**

**Voltage Gain**

The first stage is an analog amplifier. The second stage is a comparator: the output of the first stage is compared with a periodic ramp signal. The output comparator gives a pulse width modulation signal (PWM). The third and last stage is the direct conversion of the PWM signal with MOS transistors H-bridge into a powerful output signal with low impedance capability.

With an  $8 \Omega$  load, the total gain of the device is typically set to:

- 12 dB if a low level is applied to the GS pin
- 6 dB if a high level is applied to the GS pin

**Input Capacitor Selection ( $C_{in}$ )**

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high-pass filter with  $R_{in}$ , the cut-off frequency is given by

$$F_c = \frac{1}{2 \times \pi \times R_i \times C_i}$$

When a 6 dB gain is chosen the internal impedance is set to  $150 \text{ k}\Omega$ . With a 12 dB gain, the internal resistance is  $75 \text{ k}\Omega$  and thus an input capacitor value between  $10 \text{ nF}$  and  $1 \mu\text{F}$  will give a cutoff frequency between  $1 \text{ Hz}$  and  $212 \text{ Hz}$ . The NCP2821 also includes a built in low pass filtering function. Its cutoff frequency is set to  $20 \text{ kHz}$ .

**Optional Output Filter**

This filter is optional due to the capability of the speaker to filter by itself the high frequency signal. Nevertheless, the high frequency is not audible and filtered by the human ear.

An optional filter can be used for filtering high frequency signal before the speaker. In this case, the circuit consists of two inductors ( $15 \mu\text{H}$ ) and two capacitors ( $2.2 \mu\text{F}$ ) (Figure 38). The size of the inductors is linked to the output power requested by the application. A simplified version of this filter requires a  $1 \mu\text{F}$  capacitor in parallel with the load, instead of two  $2.2 \mu\text{F}$  connected to ground (Figure 39).

Cellular phones and portable electronic devices are great applications for Filterless Class-D as the track length between the amplifier and the speaker is short, thus, there is usually no need for an EMI filter. However, to lower radiated emissions as much as possible when used in filterless mode, a ferrite filter can often be used. Select a ferrite bead with the high impedance around  $100 \text{ MHz}$  and a very low DCR value in the audio frequency range is the best choice. The MPZ1608S221A1 from TDK is a good choice. The package size is 0603.

# NCP2821

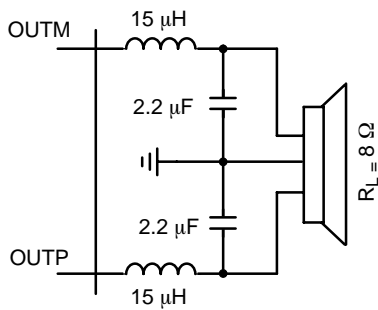


Figure 38. Advanced Optional Audio Output Filter

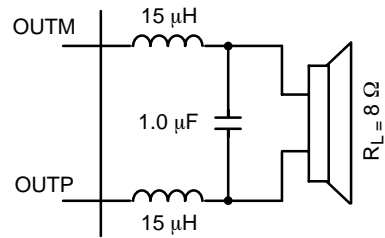


Figure 39. Optional Audio Output Filter

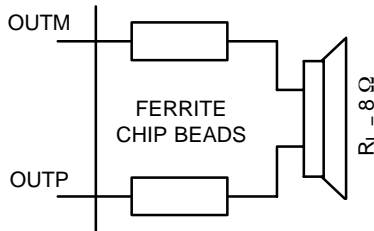


Figure 40. Optional EMI Ferrite Bead Filter

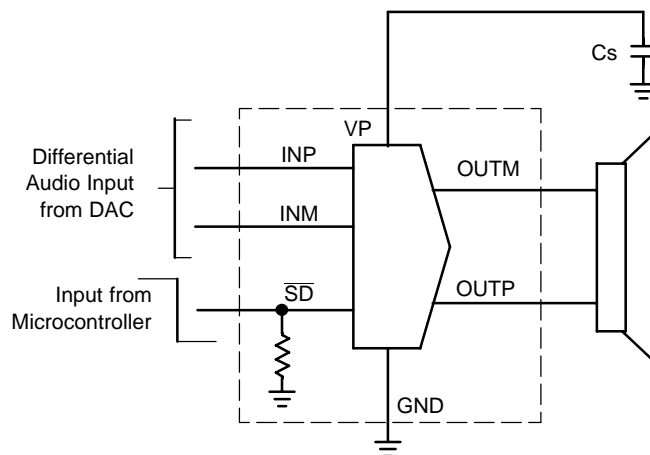


Figure 41. NCP2821 Application Schematic with Fully Differential Input Configuration

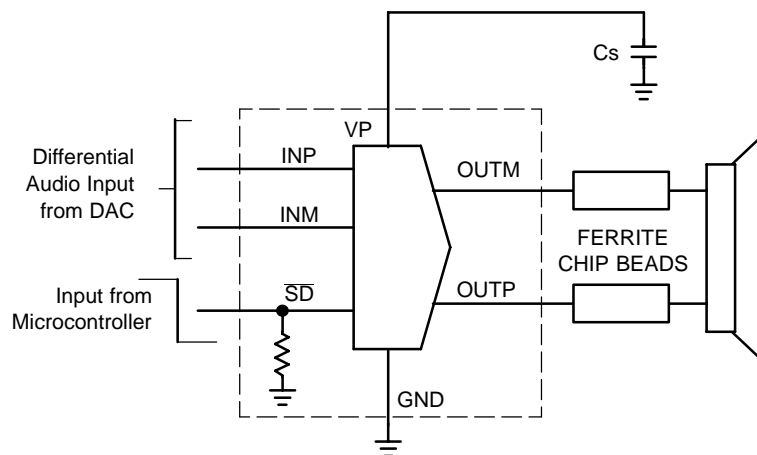


Figure 42. NCP2821 Application Schematic with Fully Differential Input Configuration and Ferrite Chip Beads as an Output EMI Filter

# NCP2821

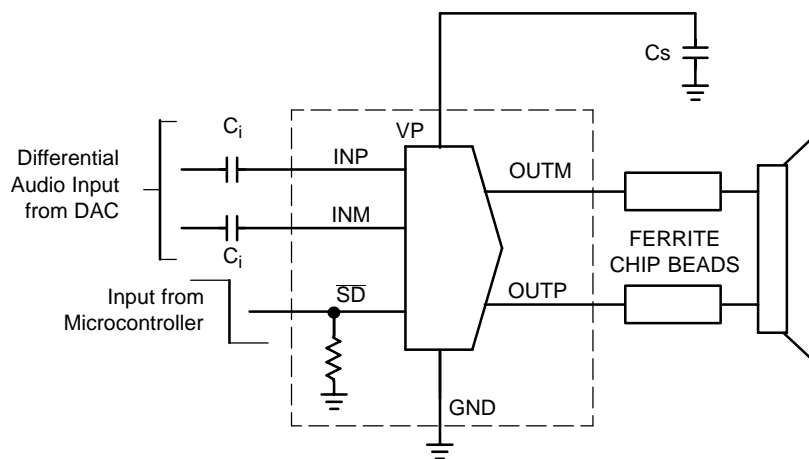


Figure 43. NCP2821 Application Schematic with Differential Input Configuration and High Pass Filtering Function

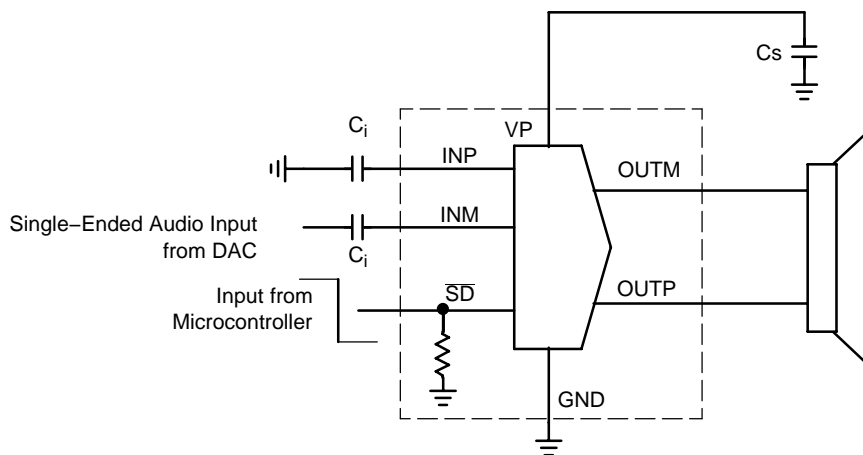


Figure 44. NCP2821 Application Schematic with Single Ended Input Configuration

# NCP2821

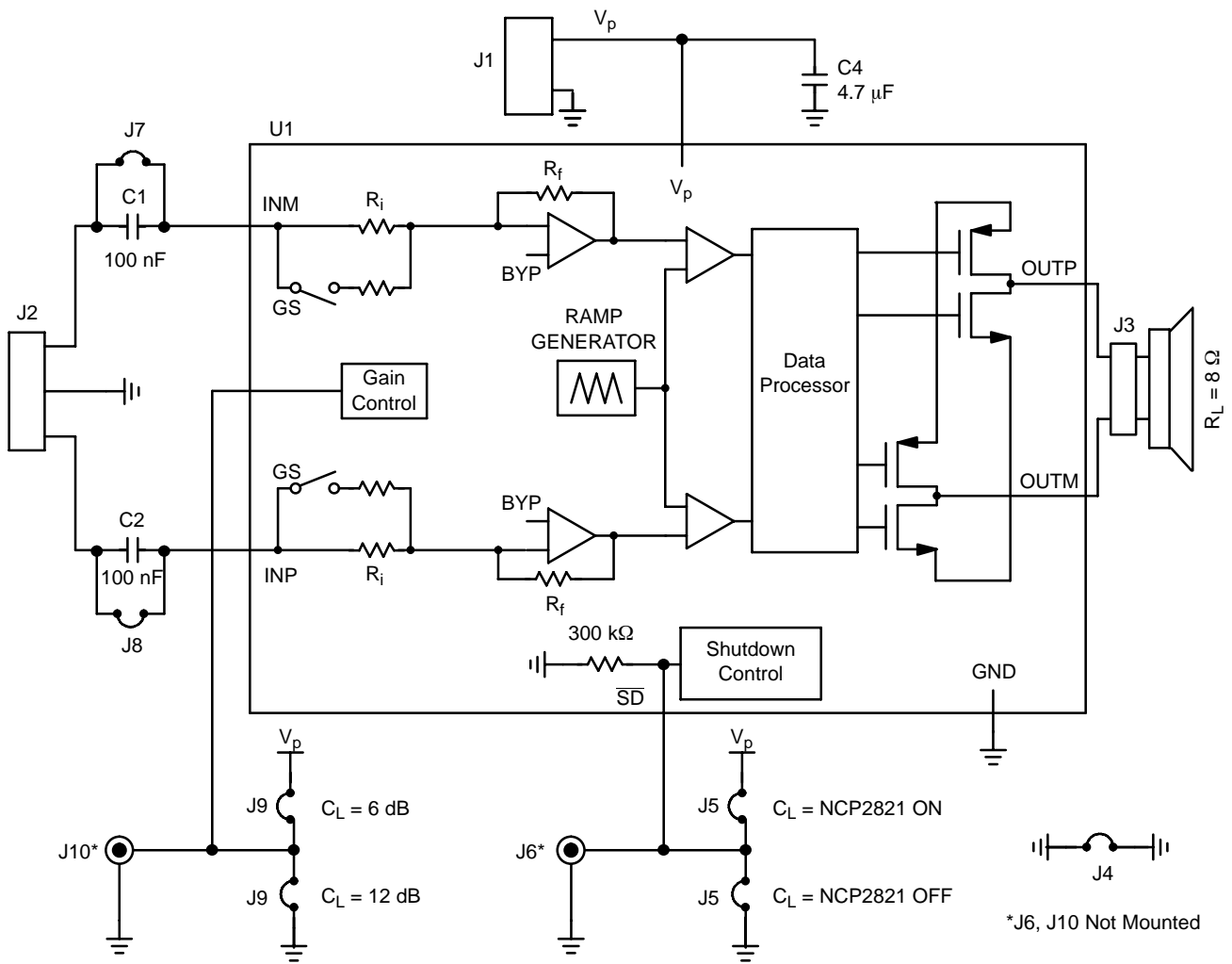


Figure 45. Schematic of the Demonstration Board of the 9-pin Flip-Chip CSP Device

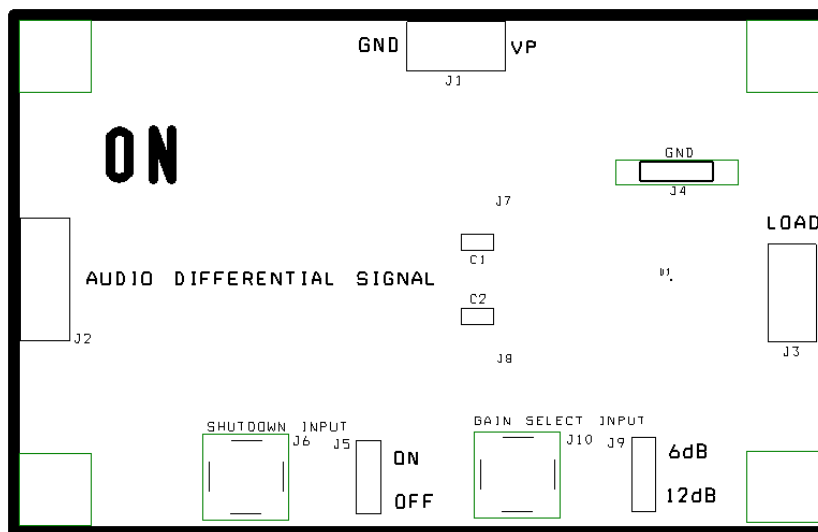


Figure 46. Silkscreen Layer

## NCP2821

### PCB Layout Information

NCP2821 is suitable for low cost solution. In a very small package it gives all the advantages of a Class-D audio amplifier. The required application board is focused on low cost solution too. Due to its fully differential capability, the audio signal can only be provided by an input resistor. If a low pass filtering function is required, then an input coupling capacitor is needed. The values of these components determine the voltage gain and the bandwidth frequency. The battery positive supply voltage requires a good decoupling capacitor versus the expected distortion.

When the board is using Ground and Power planes with at least 4 layers, a single 4.7  $\mu\text{F}$  filtering ceramic capacitor on the bottom face will give optimized performance.

A 1.0  $\mu\text{F}$  low ESR ceramic capacitor can also be used with slightly degraded performances on the THD+N from 0.06% up to 0.2%.

In a two layers application, if both  $V_p$  pins are connected on the top layer, a single 4.7  $\mu\text{F}$  decoupling capacitor will optimize the THD+N level.

The NCP2821 power audio amplifier can operate from 2.5 V until 5.5 V power supply. With less than 2% THD+N, it delivers 500 mW rms output power to a 8.0  $\Omega$  load at  $V_p = 3.0$  V and 1.0 W rms output power at  $V_p = 4.0$  V.

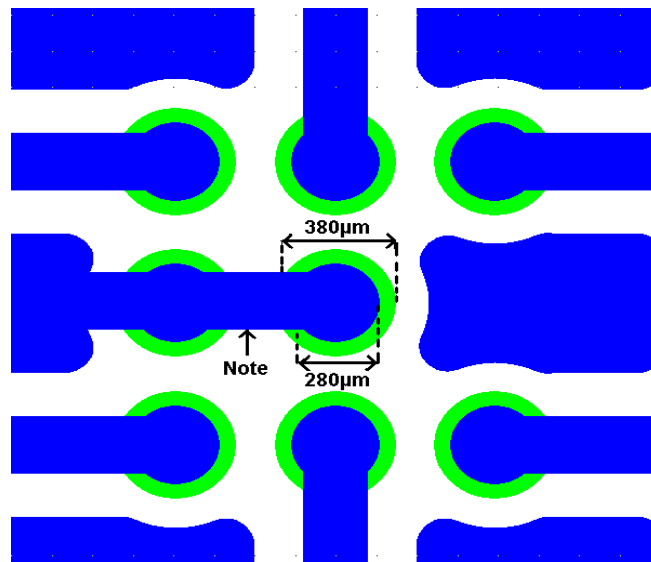


Figure 47. Top Layer

Note: This track between  $V_p$  pins is only needed when a 2 layers board is used. In case of a typical 4 or more layers, the use of laser vias in pad will optimize the THD+N floor. The demonstration board delivered by ON Semiconductor is a 4 Layers with Top, Ground, Power Supply and Bottom.



# NCP2821

## Bill of Materials

Item	Part Description	Ref	PCB Footprint	Manufacturer	Part Number
1	NCP2821 Audio Amplifier	U1			NCP2821
2	Ceramic Capacitor 100 nF, 50 V, X7R	C1, C2	0603	TDK	C1608X7R1H104KT
3	Ceramic Capacitor 4.7 $\mu$ F, 6.3 V, X5R	C4	0603	TDK	C1608X5R0J475MT
4	PCB Footprint	J7, J8			
5	I/O connector. It can be plugged by MC-1,5/3-ST-3,81	J2		Phoenix Contact	MC-1,5/3-G
6	I/O connector. It can be plugged by BLZ5.08/2 (Weidmuller Reference)	J1, J3		Weidmuller	SL5.08/2/90B
7	Jumper Connector, 400 mils	J4		Harwin	D3082-B01
8	Jumper Header Vertical Mount 3*1, 2.54 mm.	J5, J9		Tyco Electronics / AMP	5-826629-0

## ORDERING INFORMATION

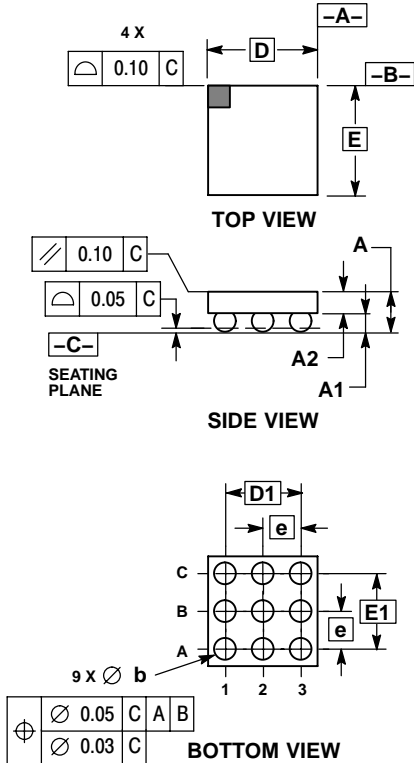
Device	Marking	Package	Shipping†
NCP2821FCT1G	MAU	9-Pin Flip-Chip CSP (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP2821

## PACKAGE DIMENSIONS

### 9-PIN FLIP-CHIP CSP FC SUFFIX CASE 499AL-01 ISSUE O



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

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