Si50x-32x4-EVB

1. Functional Description

The Si50x-32x4-EVB provides access to all I/O signals for configuring, operating, and testing the device. Jumpers and test points are provided as described below.

1.1. Power Supply

The Si50x supports operation from nominal voltages of 1.8, 2.5, and 3.3 V. Supply VDD and GND are wired in at the J1 ± terminals. Review the device data sheet and part number for allowed configurations of output buffer type and device power supply.

1.2. Jumpers

The jumpers at JP1 and JP2 allow one to pull up or pull down OE or MODE to VDD or GND. (The MODE signal is reserved for future use. It is not used by either the Si500S or the Si500D.) The current silkscreen for these jumpers is reproduced in Figure 1.
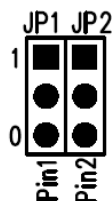

Figure 1. Jumpers Silkscreen

Pins 1 and 2 in Figure 1 refer respectively to the Si50x's OE and MODE pins. The jumper positions are illustrated in Figure 2.

The Si50x can be ordered with the OE pin pulled to the desired state, so the JP1 jumper would typically be needed only to access the opposing state.
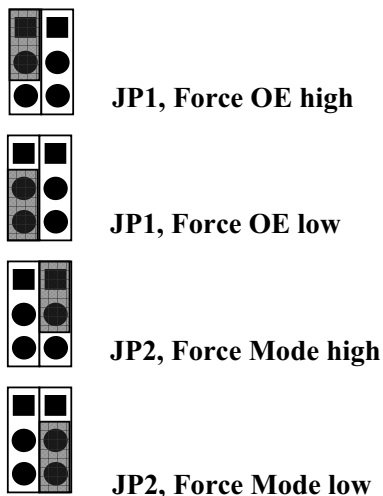

JP1, Force OE high

JP1, Force OE low

JP2, Force Mode high

JP2, Force Mode low

Figure 2. JP1–JP2 Jumper Positions

1.3. Preparing the EVB

By default, the evaluation board is set up to support ac-coupling of differential mode configured devices (i.e., Low Power LVPECL, LVDS, and SSTL). The stuffing variations for the supported output modes are tabulated in Table 1.

Table 1. Stuffing Variations

Driver	R1, R4	C2, C3	J2, J4	Instrument Termination
CMOS	empty	empty	empty	Active scope probes[*]
HCSL	empty	0.1 µF	filled	HI-Z
Low Power LVPECL	empty	0.1 µF	filled	50 Ω
LVDS	empty	0.1 µF	filled	50 Ω
LVPECL 2.5 V	100 Ω	0.1 µF	filled	50 Ω
LVPECL 3.3 V	200 Ω	0.1 µF	filled	50 Ω
SSTL	empty	0.1 µF	filled	50 Ω

*Note: Use of Coax and 50 Ω termination produces good signal integrity but incorrect signal levels and power; use of Coax and Hi-Z produces extremely bad signal integrity.

1.3.1. LVPECL Biasing

Because the Si50x can support an LVPECL buffer type (in addition to CMOS, HCSL, LVDS, or SSTL), pulldown resistor locations (R1 and R4) are available for proper output biasing. For LVPECL buffers, correct biasing can be achieved through a variety of equivalent circuits; the Si50x-32x4-EVB allows for a commonly used approximation using pulldown resistors. After the output biasing, the high-speed outputs are dc-blocked for connection to differently biased inputs such as standard test equipment.

1.4. Test Points

There are 4 through-hole test points as follows:

TP1—VDD

TP2—Output CLK_N

TP3—GND

TP4—Output CLK

Test point TP1 is located near terminal J1. Test points TP2–TP4 are located in between the output connectors.
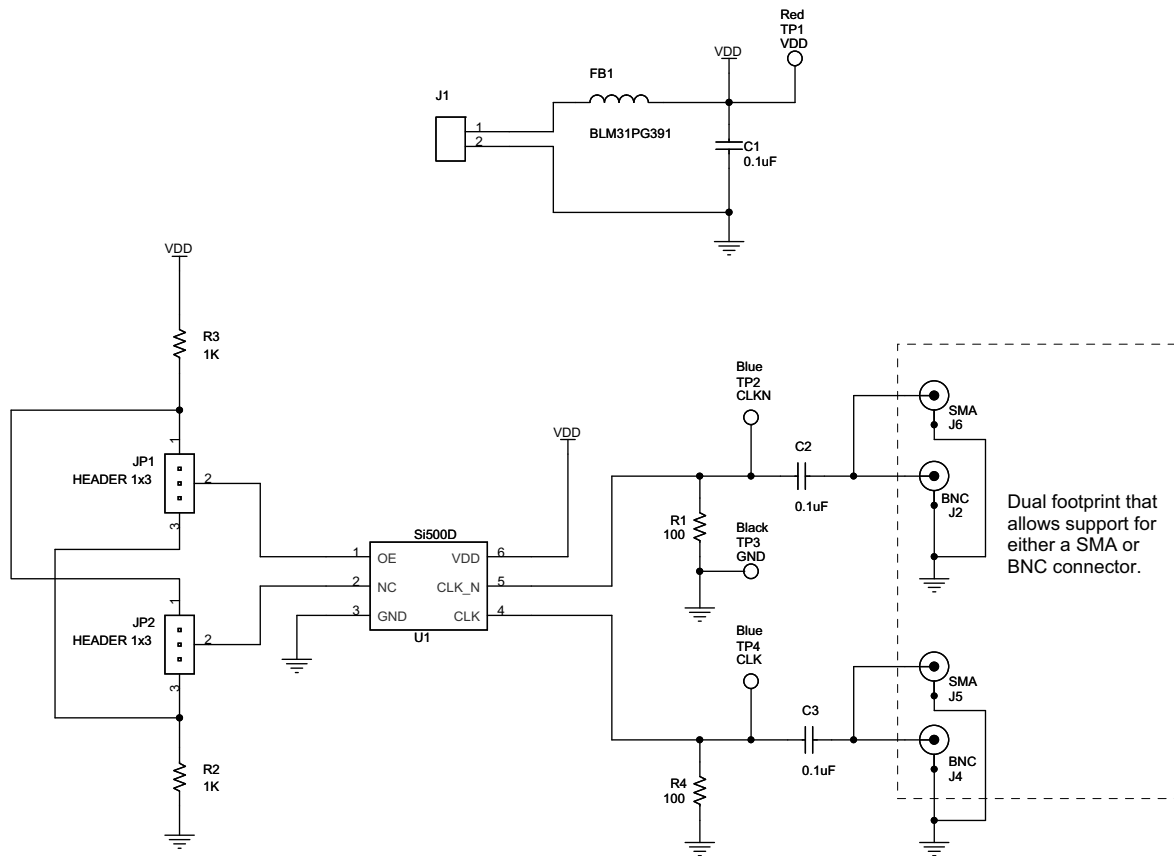
2. Schematics

Figure 3. Si50x-32x4-EVB Schematic

3. Bill of Materials

| Item	Qty	Reference	Description	Manufacturer's #	Manufacturer
1	3	C1,C2,C3	0.1 µF, 10V, ±20%, X7R, C0603	C0603X7R100-104M	Venkel
2	1	FB1	BLM31PG391, 3000mA, SMT, L1206	BLM31PG391SN1	MuRata
3	2	JP1,JP2	HEADER 1x3, Header, CONN-1X3	TSW-103-07-T-S	Samtec
4	1	J1	CONN TRBLK 2,CONN-1X2-TB	1729018	Phoenix Contact
5	2	R2,R3	1 kΩ, 1/10 W, ±1%, ThickFilm, R0603	CR0603-10W-1001F	Venkel
6	1	TP1	Test Point, Red, TESTPOINT	151-207	Kobiconn
7	2	TP2,TP4	Test Point, Blue, TESTPOINT	151-205	Kobiconn
8	1	TP3	Test Point, Black, TESTPOINT	151-230	Kobiconn
9	2	J5,J6	SMA, RF, CONN-SMA-RT	142-0701-301	Johnson Components
No Load					
10	2	J2,J4	BNC, CONN-BNC_RT	5413631-1	Tyco
11	2	R1,R4	100 Ω, 1/16 W, ±1%, ThickFilm, R0603	CR0603-16W-1000F	Venkel
12	1	U1	Si500	Si500	Skyworks Solutions

4. Layout
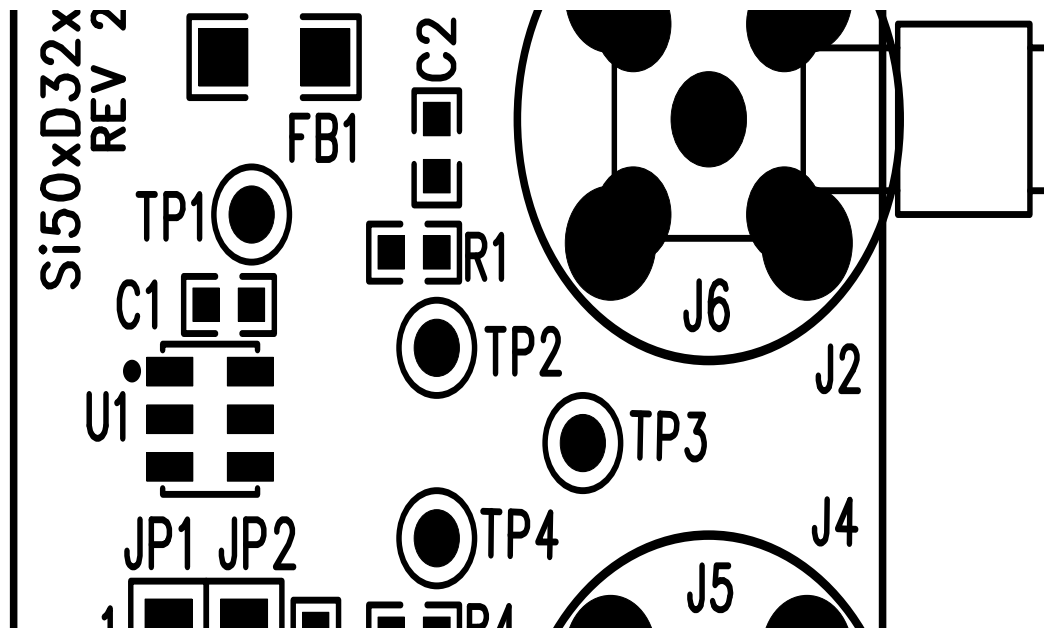
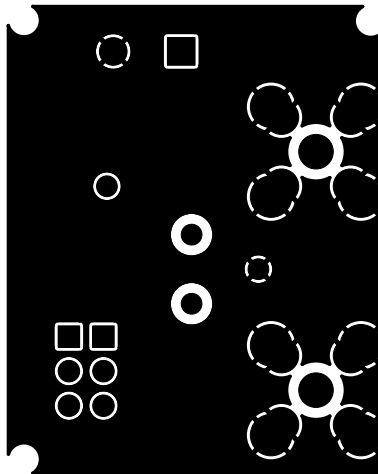**Figure 4. Assembly Drawing**
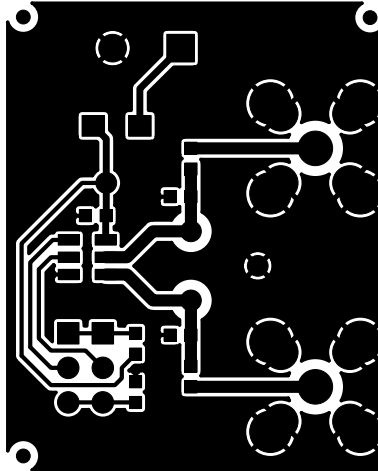
Figure 5. Layer 1 Primary

Figure 6. Layer 2 Secondary

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Revised text, schematic, layout, and BOM to reflect Si50x-32x4-EVB Rev. 2.0 instead of Rev. 1.0.

NOTES:

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