

# Improved Low-Power, CMOS Analog Switches with Latches

## ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-	Continuous Power Dissipation (T <sub>A</sub> = +70°C)
V+ ..... 44V	16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
GND ..... 25V	20-Pin PLCC (derate 10.00mW/°C above +70°C) ..... 800mW
V <sub>L</sub> ..... (GND - 0.3V) to (V+ + 0.3V)	16-Pin CERDIP (derate 10.00mW/°C above +70°C) ... 800mW
Digital Inputs, V <sub>S</sub> , V <sub>D</sub> (Note 1) ..... (V- - 2V) to (V+ + 2V)	Operating Temperature Ranges
Current (any terminal, except S or D) ..... 30mA	DG42_C_ ..... 0°C to +70°C
Continuous Current, S or D ..... 20mA	DG42_D_ ..... -40°C to +85°C
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) ... 100mA	DG42_A_ ..... -55°C to +125°C
	Storage Temperature Ranges
	DG42_C_/DG42_D_ ..... -65°C to +125°C
	DG42_A_ ..... -65°C to +150°C
	Lead Temperature (soldering, 10sec) ..... +300°C

**Note 1:** Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V<sub>L</sub> = +5V, GND = 0V, V<sub>INH</sub> = +2.4V, V<sub>INL</sub> = +0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	DG42_C, DG42_D			DG42_A			UNITS			
			MIN	TYP	MAX	MIN	TYP	MAX				
<b>SWITCH</b>												
Analog Signal Range	V <sub>ANALOG</sub>	(Note 3)	-15		15	-15		15	V			
Drain-Source On-Resistance	r <sub>DS(ON)</sub>	V+ = 13.5V, V- = -13.5V, I <sub>S</sub> = -10mA, V <sub>D</sub> = ±10V	T <sub>A</sub> = +25°C			20			45	Ω		
		T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			45			45				
On-Resistance Match Between Channels (Note 4)	Δr <sub>DS(ON)</sub>	V+ = 16.5V, V- = -16.5V, I <sub>S</sub> = -10mA, V <sub>D</sub> = ±10V	T <sub>A</sub> = +25°C			3			3	Ω		
		T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			4			4				
On-Resistance Flatness (Note 4)	r <sub>FLAT(ON)</sub>	V+ = 15V, V- = -15V, I <sub>S</sub> = -10mA, V <sub>D</sub> = ±5V	T <sub>A</sub> = +25°C			4			4	Ω		
		T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			5			5				
Source-Off Leakage Current (Note 5)	I <sub>S(OFF)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ∓15.5V	T <sub>A</sub> = +25°C			-0.50	-0.01	0.50	-0.25	-0.01	0.25	nA
		T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			-5		5	-10		10		
Drain-Off Leakage Current (Note 5)	I <sub>D(OFF)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ∓15.5V	T <sub>A</sub> = +25°C			-0.50	-0.01	0.50	-0.25	-0.01	0.25	nA
		T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			-5		5	-10		10		
Drain-On Leakage Current (Note 5)	I <sub>D(ON)</sub>	V+ = 16.5V, V- = -16.5V, V <sub>D</sub> = ±15.5V, V <sub>S</sub> = ±15.5V	T <sub>A</sub> = +25°C			-1.0	-0.04	1.0	-0.40	-0.04	0.40	nA
		T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			-10		10	-20		20		

# Improved Low-Power, CMOS Analog Switches with Latches

DG421/DG423/DG425

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, VL = +5V, GND = 0V, VINH = +2.4V, VINL = +0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS	
<b>INPUT</b>							
Input Current with Input Voltage High	IINH	IN = 2.4V, all others = 0.8V	-0.50	0.005	0.50	μA	
Input Current with Input Voltage Low	IINL	IN = 0.8V, all others = 2.4V	-0.50	0.005	0.50	μA	
<b>SUPPLY</b>							
Power Supply Range	V+, V-	(Note 3)	±4.5		±20	V	
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1.0	0.01	1.0	μA
			TA = TMIN to TMAX	-5.0		5.0	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1.0	-0.01	1.0	μA
			TA = TMIN to TMAX	-5.0		5.0	
Logic Supply Current	IL	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1.0	-0.01	1.0	μA
			TA = TMIN to TMAX	-5.0		5.0	
Ground Current	IGND	All channels on or off, V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V	TA = +25°C	-1.0	-0.01	1.0	μA
			TA = TMIN to TMAX	-5.0		5.0	
<b>DYNAMIC</b>							
Turn-On Time	tON	Figure 2	TA = +25°C	150	250	ns	
			TA = TMIN to TMAX		300		
Turn-Off Time	toFF	Figure 2			200	ns	
Latch Timing	tww	VS = ±10V, RL = 300Ω, CL = 35pF, Figure 3	TA = +25°C	200		ns	
			TA = -55°C to +125°C	200			
	TA = +25°C		100				
	TA = -55°C to +125°C		100				
	TA = +25°C		60				
	tDW		TA = +25°C	60			
	tWD		TA = -55°C to +125°C	100			
Break-Before-Make Interval (Note 3)	tD	DG423, Figure 4	TA = +25°C	5	25	ns	
Charge Injection (Note 3)	Q	CL = 10nF, VG = 0V, RG = 0Ω, Figure 5	TA = +25°C	10	15	pC	
Off-Isolation Rejection Ratio (Note 6)	OIRR	RL = 100Ω, CL = 5pF, f = 1MHz, Figure 6	TA = +25°C	72		dB	
Crosstalk (Note 7)		RL = 50Ω, CL = 5pF, f = 1MHz, Figure 7	TA = +25°C	90		dB	
Drain-Off Capacitance	CD(OFF)	f = 1MHz, Figure 8	TA = +25°C	12		pF	
Source-Off Capacitance	CS(OFF)	f = 1MHz, Figure 8	TA = +25°C	12		pF	
Drain-On Capacitance	CD(ON)	f = 1MHz, Figure 9	TA = +25°C	39		pF	
Source-On Capacitance	CS(ON)	f = 1MHz, Figure 9	TA = +25°C	39		pF	

**Note 2:** Typical values are for design aid only, are not guaranteed, and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

**Note 3:** Guaranteed by design.

**Note 4:** On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

**Note 5:** Leakage parameters IS(OFF), ID(OFF), and ID(ON) are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

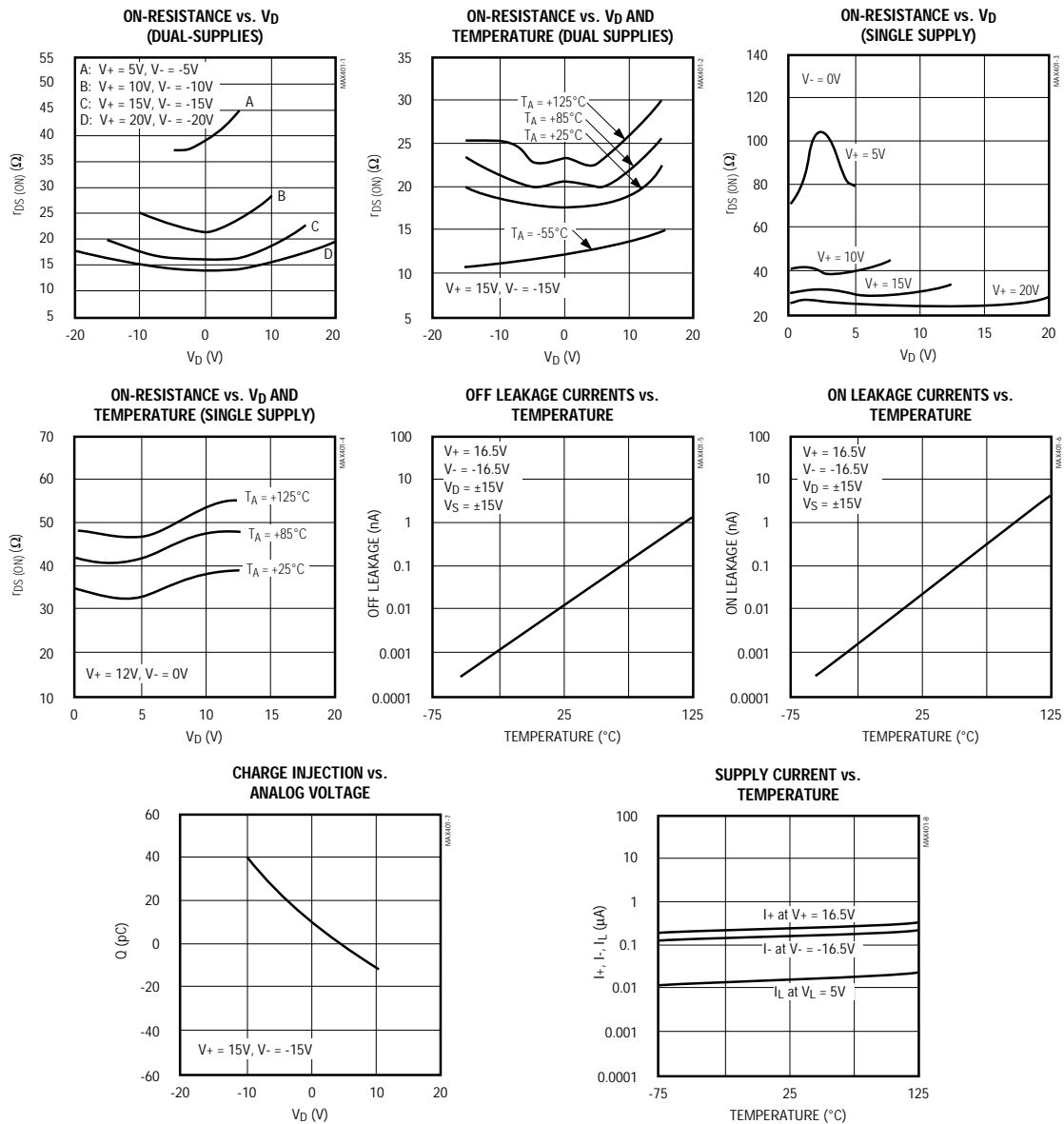
**Note 6:** Off-Isolation Rejection Ratio = 20log (VD/VS), VD = output, VS = input to off switch.

**Note 7:** Between any two switches.

# Improved Low-Power, CMOS Analog Switches with Latches

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# Improved Low-Power, CMOS Analog Switches with Latches

DG421/DG423/DG425

## Pin Descriptions

DG421			
PIN	NAME	FUNCTION	
1, 8	D1, D2	Drain Terminals	
2	$\overline{WR}$	Write Select	
3, 4, 5, 6	N.C.	No Internal Connection	
7	$\overline{RS}$	Reset Select	
9, 16	S1, S2	Source Terminals	
10, 15	IN1, IN2	Input Control	
11	V+	Positive Supply	
12	V <sub>L</sub>	Logic Supply	
13	GND	Ground	
14	V-	Negative Supply	
DG423/DG425			
DIP	PLCC	NAME	FUNCTION
1, 8, 3, 6	2, 10, 4, 8	D1-D4	Drain Terminals
2	3	$\overline{WR}$	Write Select
16, 9, 4, 5	20, 12, 5, 7	S1-S4	Source Terminals
7	9	$\overline{RS}$	Resets Select
15, 10	19, 13	IN1, IN2	Input Control
11	14	V+	Positive Supply
12	15	V <sub>L</sub>	Logic Supply
—	1, 6, 11, 16	N.C.	No Internal Connection
14	18	V-	Negative Supply
13	17	GND	Ground

## Applications Information

### Operation with Supply Voltages Other Than $\pm 15V$

The DG421/DG423/DG425 switches operate with  $\pm 4.5V$  to  $\pm 20V$  bipolar supplies or with a  $+10V$  to  $+30V$  single supply. In either case, analog signals ranging from  $V+$  to  $V-$  can be switched. The *Typical Operating Characteristics* graphs illustrate typical analog-signal and supply-voltage on-resistance variations. The usual on-resistance temperature coefficient is  $0.5\%/^{\circ}C$  (typ).

### Logic Inputs

These devices operate with a single positive supply or with bipolar supplies. They maintain TTL compatibility with supplies anywhere in the  $\pm 4.5V$  to  $\pm 20V$  range as long as  $V_L = +5V$ . If  $V_L$  is connected to  $V+$  or another supply at voltages other than  $+5V$ , the devices will operate at CMOS-logic-level inputs.

### Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence  $V+$  on first, followed by  $V_L$ ,  $V-$ , and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to  $1V$  below  $V+$  and  $1V$  above  $V-$ , without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between  $V+$  and  $V-$  should not exceed  $+44V$ .

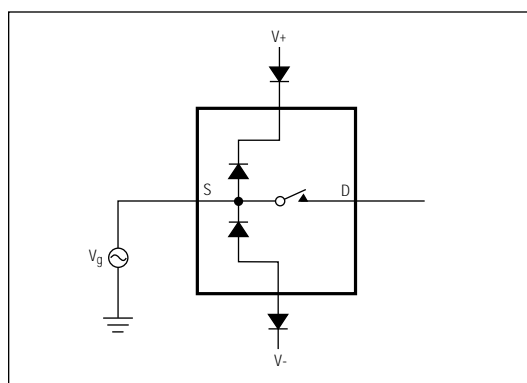


Figure 1. Overvoltage Protection Using External Blocking Diodes

# Improved Low-Power, CMOS Analog Switches with Latches

## Timing Diagrams/Test Circuits

V<sub>OUT</sub> is the steady-state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

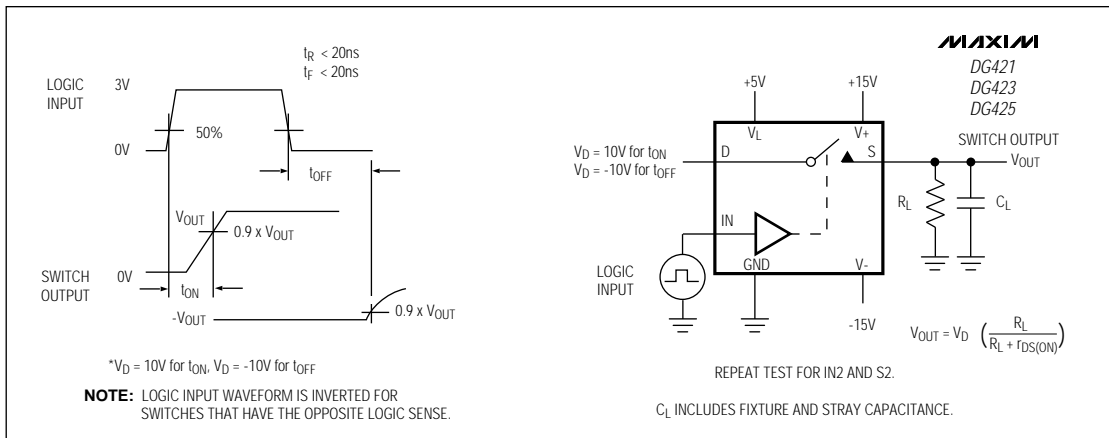


Figure 2. Switching Time

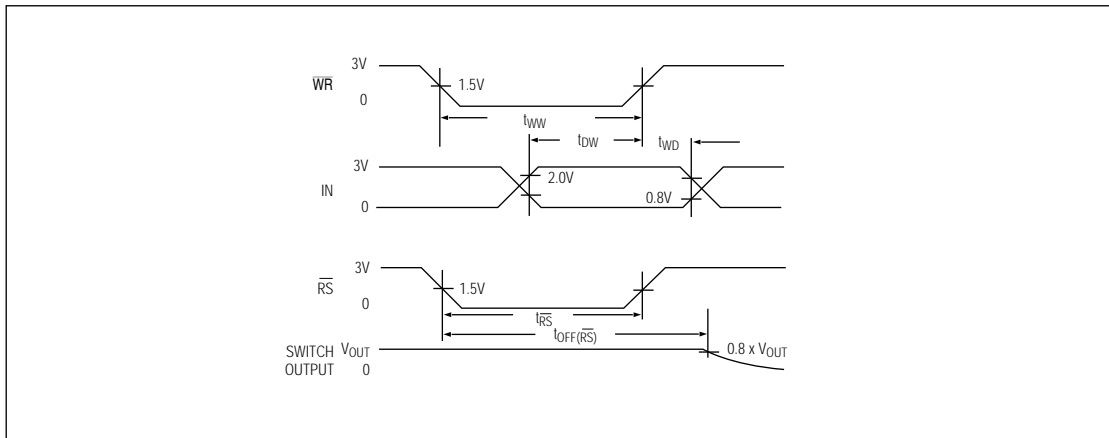


Figure 3. Latch Timing

# Improved Low-Power, CMOS Analog Switches with Latches

Timing Diagrams/Test Circuits (continued)

DG421/DG423/DG425

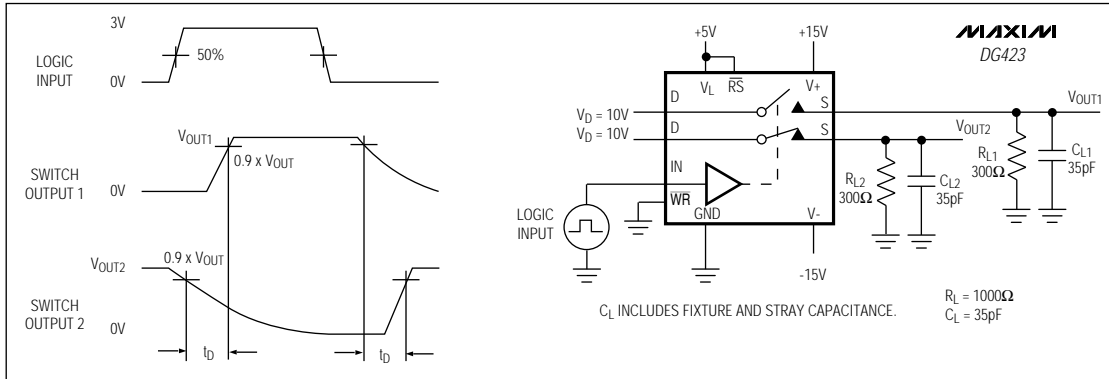


Figure 4. DG423 Break-Before-Make Interval

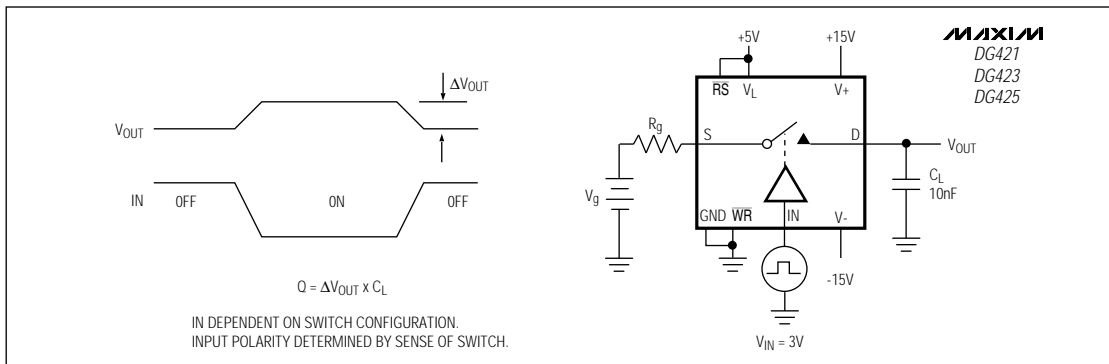


Figure 5. Charge Injection

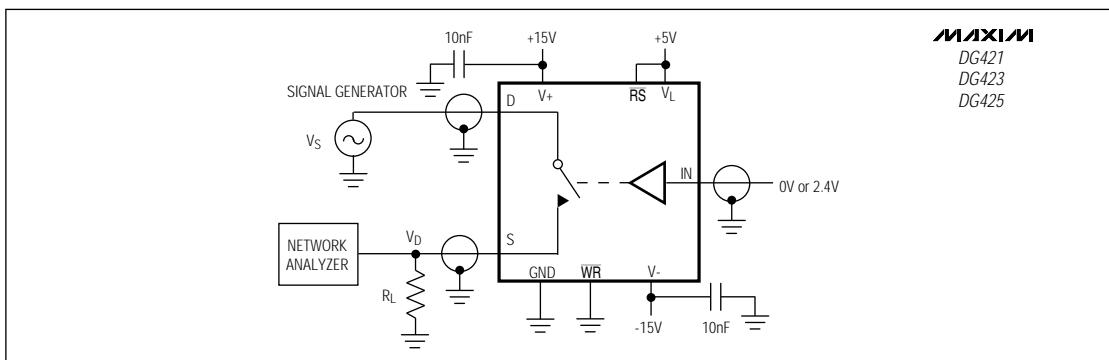


Figure 6. Off-Isolation Rejection Ratio

# Improved Low-Power, CMOS Analog Switches with Latches

Timing Diagrams/Test Circuits (continued)

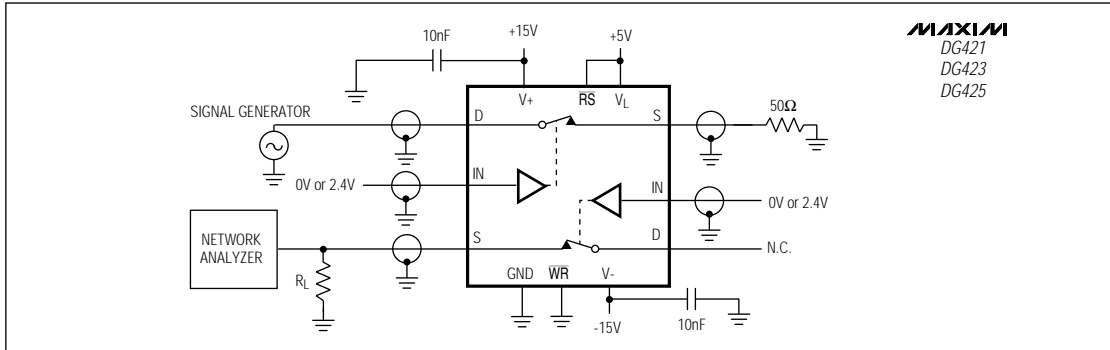


Figure 7. Crosstalk

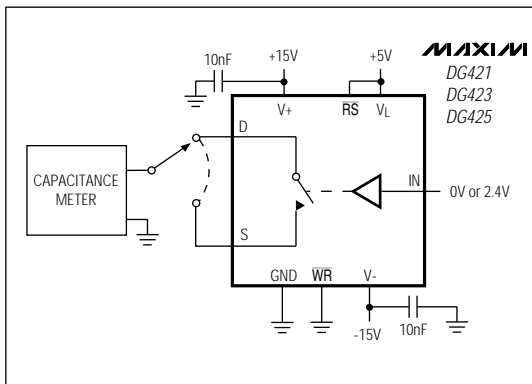


Figure 8. Drain/Source-Off Capacitance

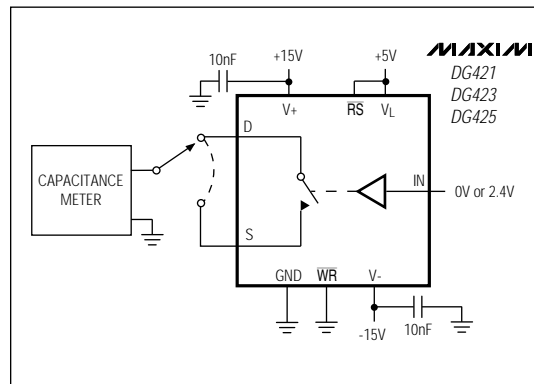
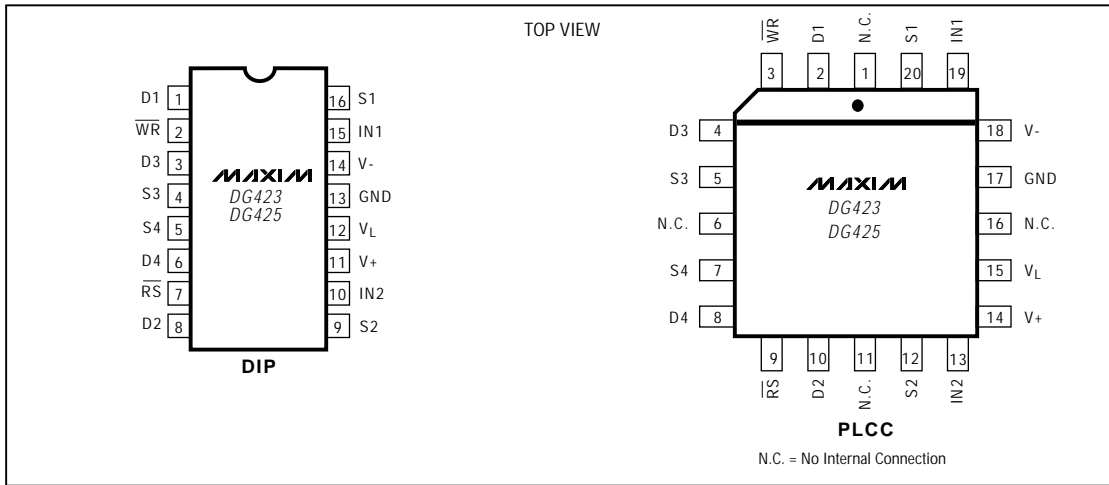


Figure 9. Drain/Source-On Capacitance

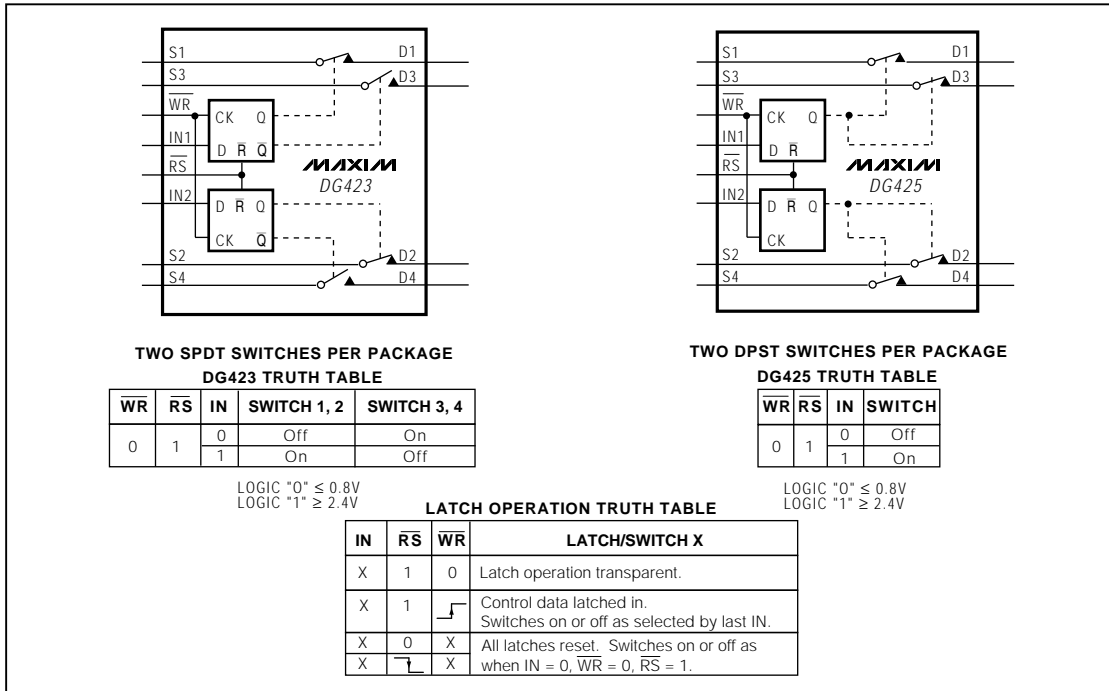
# Improved Low-Power, CMOS Analog Switches with Latches

Pin Configurations (continued)

DG421/DG423/DG425



Functional Diagrams/Truth Tables (continued)





# Improved Low-Power, CMOS Analog Switches with Latches

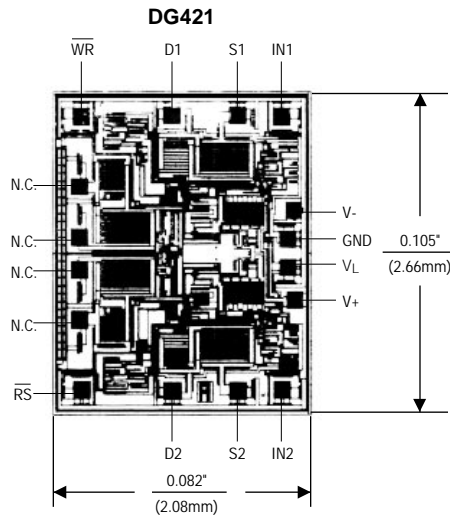
\_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
<b>DG423CJ</b>	0°C to +70°C	16 Plastic DIP
DG423CY	0°C to +70°C	16 SO
DG423C/D	0°C to +70°C	Dice*
DG423DJ	-40°C to +85°C	16 Plastic DIP
DG423DY	-40°C to +85°C	16 SO
DG423DN	-40°C to +85°C	20 PLCC
DG423DK	-40°C to +85°C	16 CERDIP
DG423AK	-55°C to +125°C	16 CERDIP**
<b>DG425CJ</b>	0°C to +70°C	16 Plastic DIP
DG425CY	0°C to +70°C	16 SO
DG425C/D	0°C to +70°C	Dice*
DG425DJ	-40°C to +85°C	16 Plastic DIP
DG425DY	-40°C to +85°C	16 SO
DG425DN	-40°C to +85°C	20 PLCC
DG425DK	-40°C to +85°C	16 CERDIP
DG425AK	-55°C to +125°C	16 CERDIP**

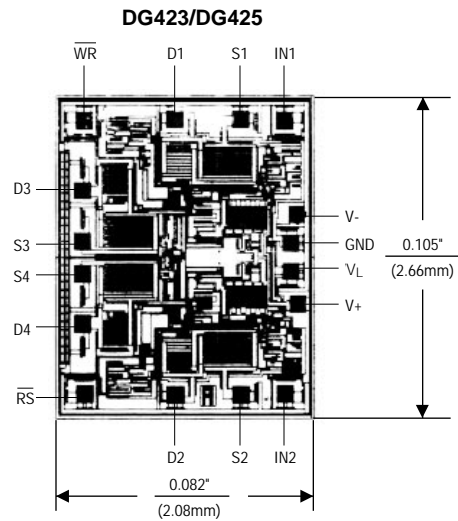
\* Contact factory for dice specifications.

\*\*Contact factory for availability and processing to MIL-STD-883B.

## Chip Topographies



TRANSISTOR COUNT: 100  
SUBSTRATE CONNECTED TO V+

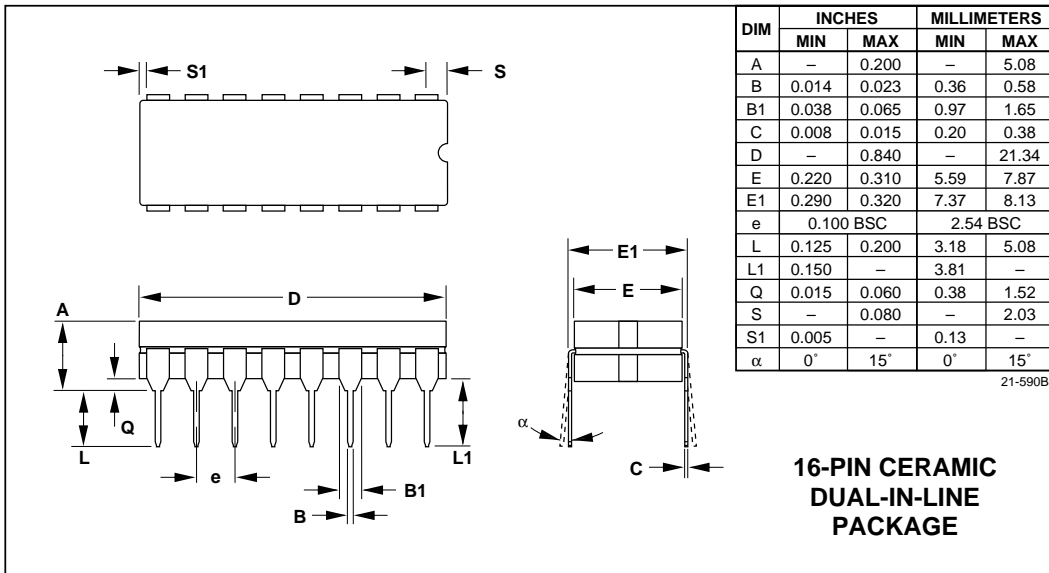
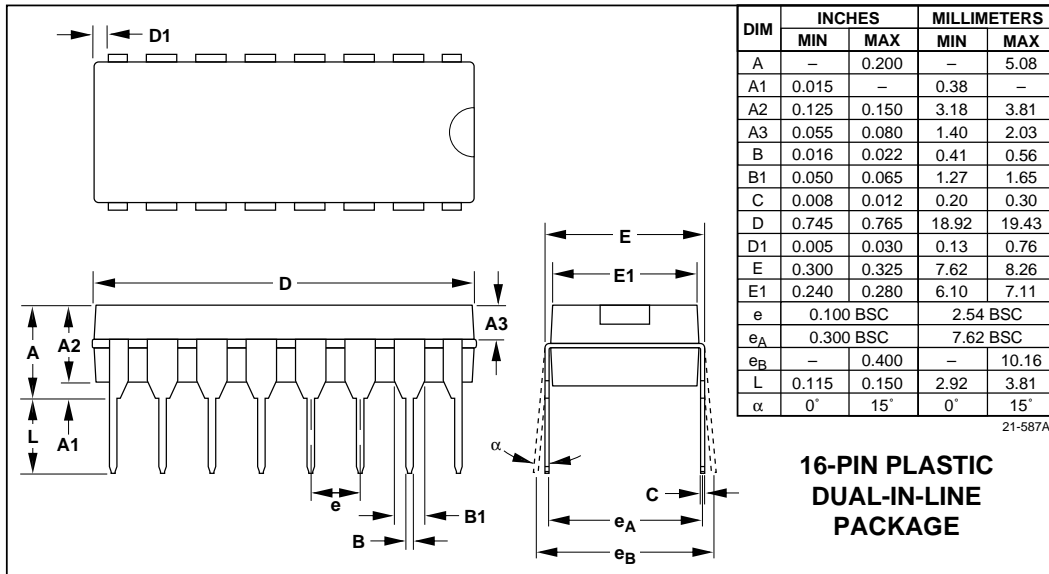


TRANSISTOR COUNT: 100  
SUBSTRATE CONNECTED TO V+

# Improved Low-Power, CMOS Analog Switches with Latches

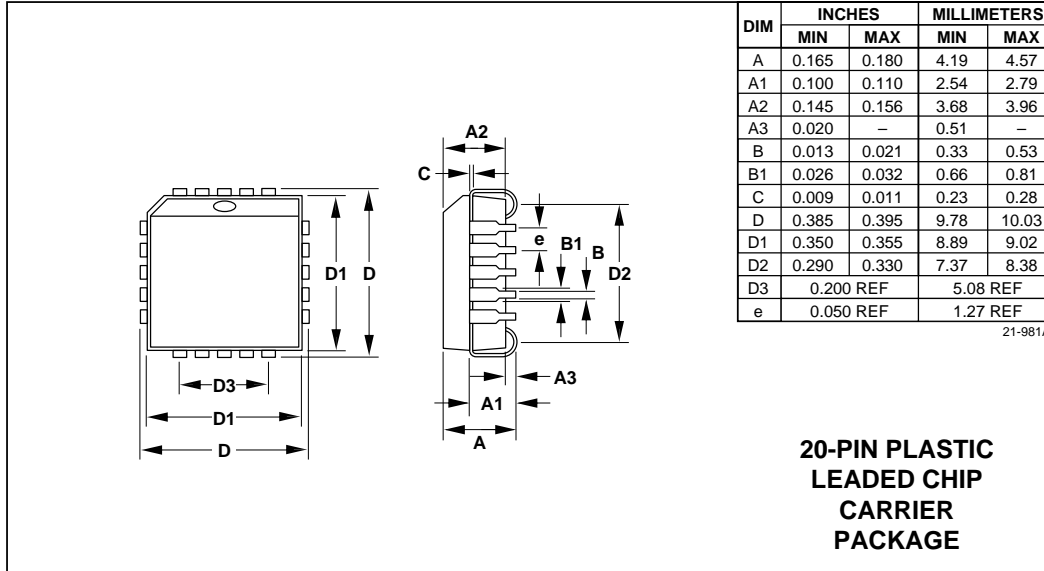
## Package Information

DG421/DG423/DG425



# Improved Low-Power, CMOS Analog Switches with Latches

Package Information (continued)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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