

# MC14517B

**FUNCTIONAL TRUTH TABLE** (X = Don't Care)

Clock	Write Enable	Data	16-Bit Tap	32-Bit Tap	48-Bit Tap	64-Bit Tap
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
$\surd$	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
$\surd$	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
$\surd$	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
$\surd$	1	X	High Impedance	High Impedance	High Impedance	High Impedance

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  "1" Level	$V_{OL}$  $V_{OH}$	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
			10	-	0.05	-	0	0.05	-	0.05	
			15	-	0.05	-	0	0.05	-	0.05	
			5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage $(V_O = 4.5$ or $0.5$ Vdc) $(V_O = 9.0$ or $1.0$ Vdc) $(V_O = 13.5$ or $1.5$ Vdc)  $(V_O = 0.5$ or $4.5$ Vdc) $(V_O = 1.0$ or $9.0$ Vdc) $(V_O = 1.5$ or $13.5$ Vdc)	"0" Level  "1" Level	$V_{IL}$  $V_{IH}$	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
			10	-	3.0	-	4.50	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
			5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
Output Drive Current $(V_{OH} = 2.5$ Vdc) $(V_{OH} = 4.6$ Vdc) $(V_{OH} = 9.5$ Vdc) $(V_{OH} = 13.5$ Vdc)  $(V_{OL} = 0.4$ Vdc) $(V_{OL} = 0.5$ Vdc) $(V_{OL} = 1.5$ Vdc)	Source  Sink	$I_{OH}$  $I_{OL}$	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
			5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
			10	-1.6	-	-1.3	-2.25	-	-0.9	-	
			15	-4.2	-	-3.4	-8.8	-	-2.4	-	
			5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
			10	1.6	-	1.3	2.25	-	0.9	-	
			15	4.2	-	3.4	8.8	-	2.4	-	
Input Current		$I_{in}$	15	-	$\pm 0.1$	-	$\pm 0.00001$	$\pm 0.1$	-	$\pm 1.0$	$\mu$ Adc
Input Capacitance ( $V_{in} = 0$ )		$C_{in}$	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		$I_{DD}$	5.0	-	5.0	-	0.005	5.0	-	150	$\mu$ Adc
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) $(C_L = 50$ pF on all outputs, all buffers switching)		$I_T$	5.0	$I_T = (4.2 \mu A/kHz) f + I_{DD}$						$\mu$ Adc	
	10	$I_T = (8.8 \mu A/kHz) f + I_{DD}$									
	15	$I_T = (13.7 \mu A/kHz) f + I_{DD}$									
Three-State Leakage Current		$I_{TL}$	15	-	$\pm 0.1$	-	$\pm 0.0001$	$\pm 0.1$	-	$\pm 3.0$	$\mu$ Adc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:  $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$  where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.004$ .

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## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.65 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 390 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 177 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 115 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	- - -	475 210 140	770 300 215	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	330 125 100	170 75 60	- - -	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	- - -	3.0 6.7 8.3	1.5 4.0 5.3	MHz
Clock Pulse Rise and Fall Time	$t_{TLH}, t_{THL}$	5.0 10 15	See (Note 7)			-
Data to Clock Setup Time	$t_{su}$	5.0 10 15	0 10 15	-40 -15 0	- - -	ns
Data to Clock Hold Time	$t_h$	5.0 10 15	150 75 35	75 25 10	- - -	ns
Write Enable to Clock Setup Time	$t_{su}$	5.0 10 15	400 200 110	170 65 50	- - -	ns
Write Enable to Clock Release Time	$t_{rel}$	5.0 10 15	380 180 100	160 55 40	- - -	ns

- The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .
- Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
- When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

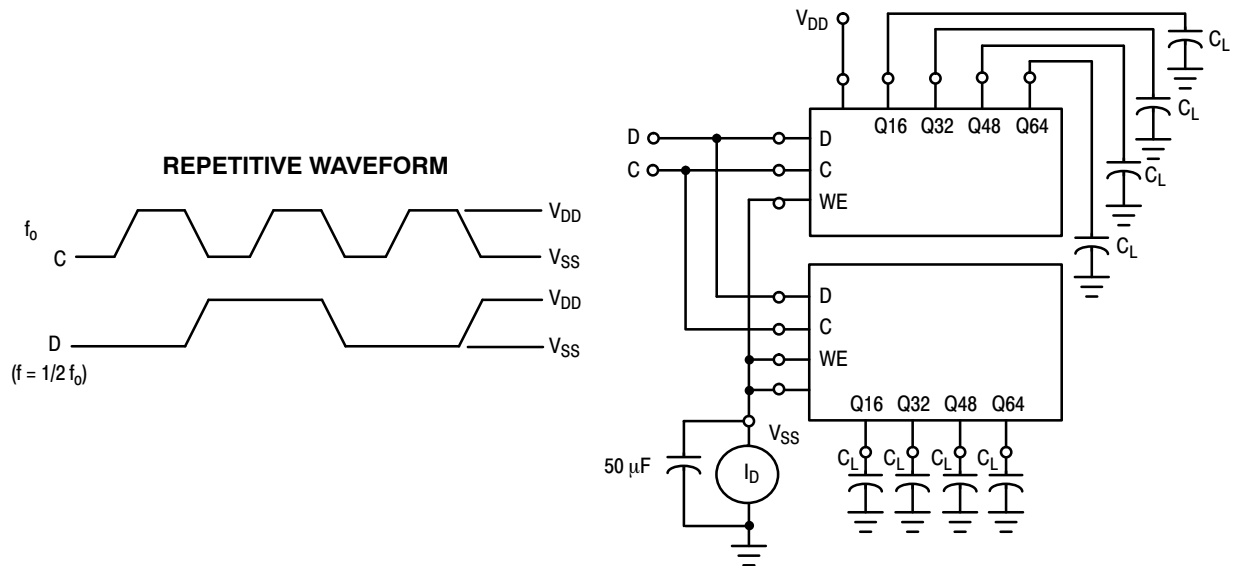
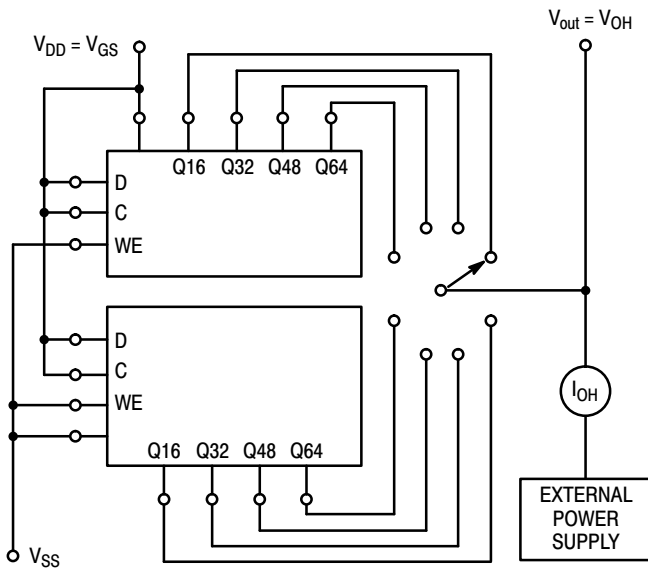


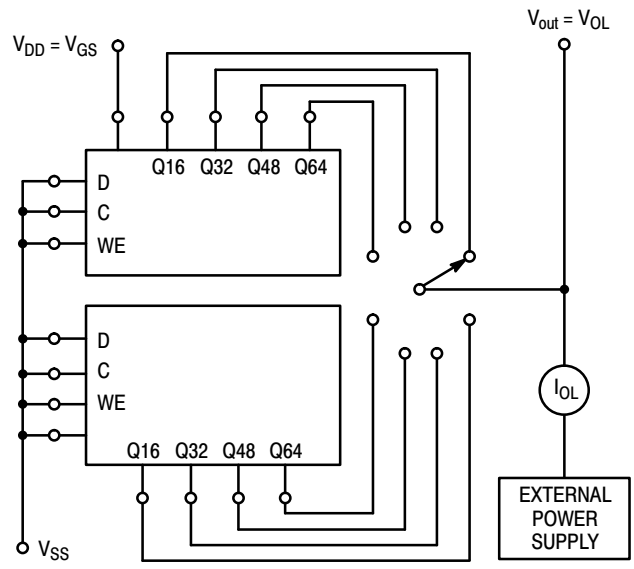
Figure 1. Power Dissipation Test Circuit and Waveform

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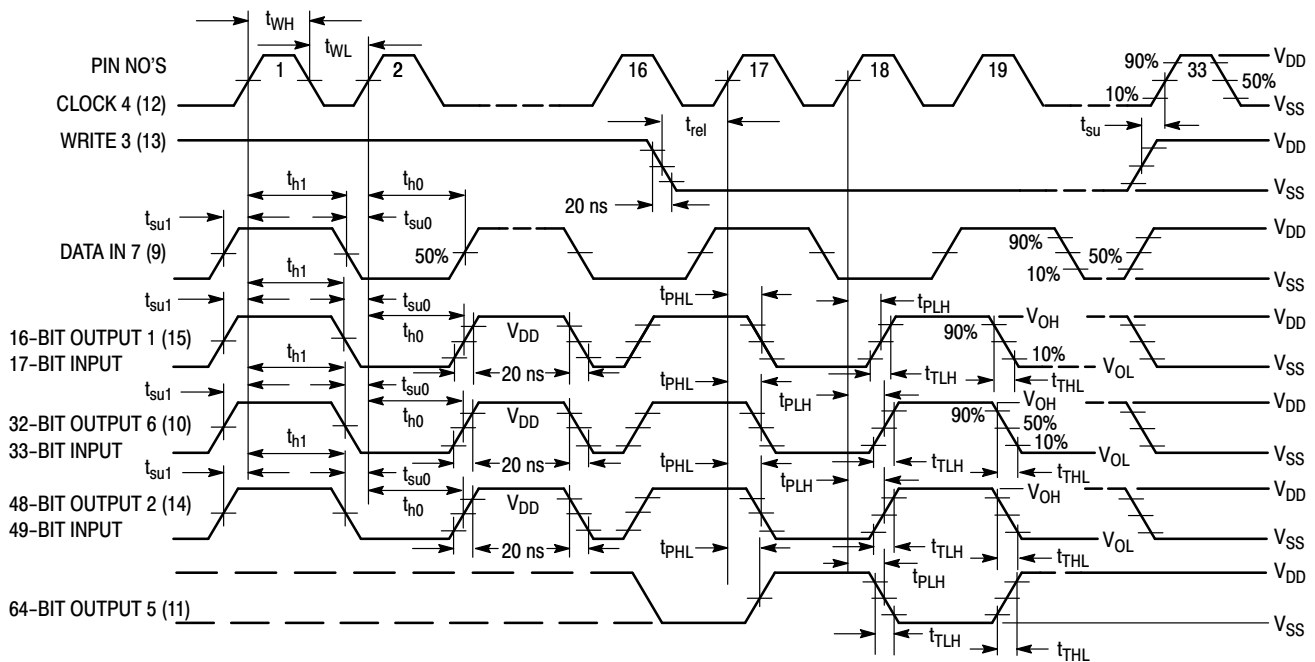
(Output being tested should be in the high-logic state)

**Figure 2. Typical Output Source Current Characteristics Test Circuit**



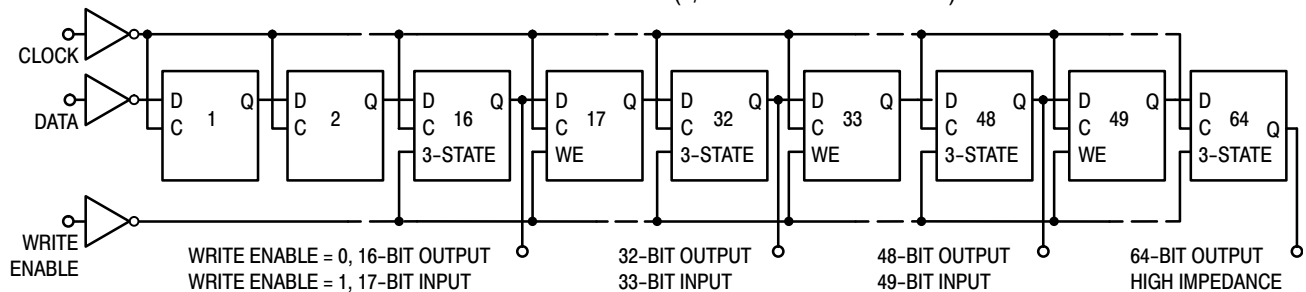
(Output being tested should be in the low-logic state)

**Figure 3. Typical Output Sink Current Characteristics Test Circuit**



**Figure 4. AC Test Waveforms**

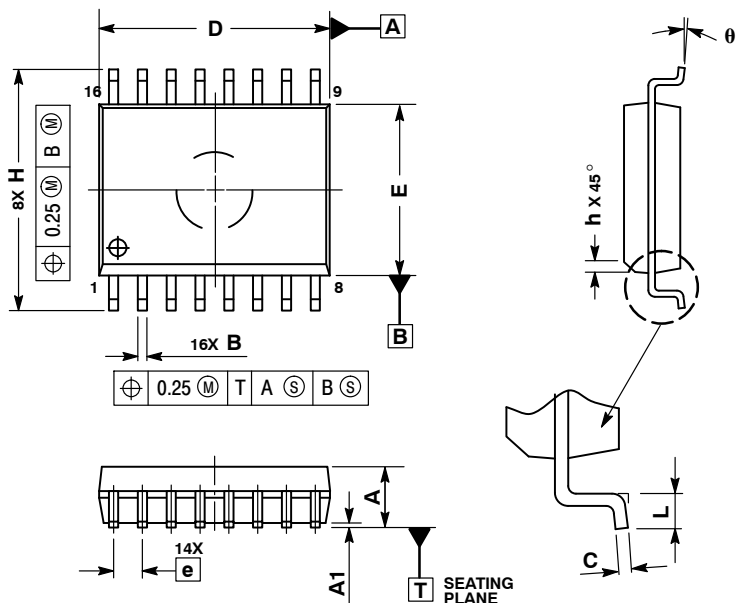
## EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



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## PACKAGE DIMENSIONS

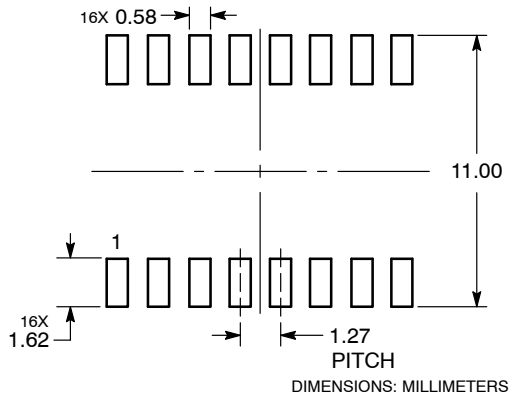
SOIC-16 WB  
CASE 751G-03  
ISSUE D



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

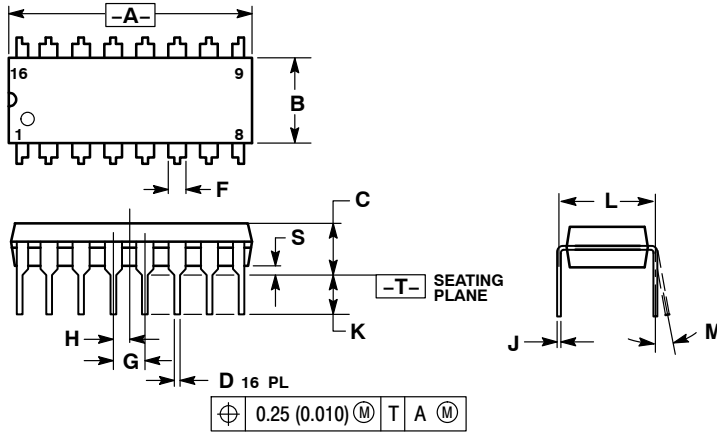
### SOLDERING FOOTPRINT



# MC14517B

## PACKAGE DIMENSIONS

PDIP-16  
CASE 648-08  
ISSUE T



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 <sup>o</sup>	10 <sup>o</sup>	0 <sup>o</sup>	10 <sup>o</sup>
S	0.020	0.040	0.51	1.01

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