

TCP-3082H

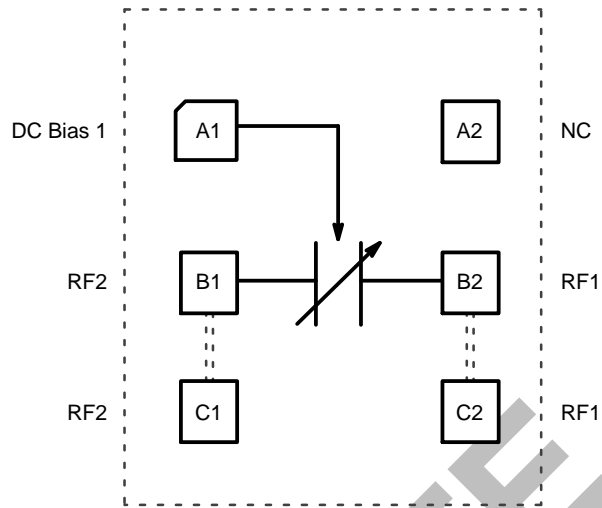


Figure 1. PTIC Functional Block Diagram (Top Level View)

Table 1. SIGNAL DESCRIPTIONS

| Ball / Pad Number | Pin Name | Description |
|-------------------|-----------|-------------------|
| A1 | DC Bias 1 | DC Bias Voltage |
| B1 | RF2 | RF Input / Output |
| C1* | RF2 | RF Input / Output |
| A2 | NC | Not Connected |
| B2 | RF1 | RF Input / Output |
| C2* | RF1 | RF Input / Output |

*Ball/pad contains multiple connections. Please see packaging information on last page for more information.

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TYPICAL SPECIFICATIONS

Representative Performance Data at 25°C

Table 2. PERFORMANCE DATA

| Parameter | Min | Typ | Max | Units |
|-------------------------------------------------|------|------|------|---------------|
| Operating Bias Voltage | 2.0 | | 20 | V |
| Capacitance ($V_{bias} = 2\text{ V}$) | 7.38 | 8.20 | 9.02 | pF |
| Capacitance ($V_{bias} = 20\text{ V}$) | 2.05 | 2.16 | 2.27 | pF |
| Tuning Range (2 V - 20 V) | 3.40 | 3.80 | 4.20 | |
| Tuning Range (20 V - 2 V) | | 3.60 | | |
| Leakage Current (WLCSP) | | | 2.0 | μA |
| Operating Frequency | 700 | | 2700 | MHz |
| Quality Factor @ 700 MHz, 10 V | | 100 | | |
| Quality Factor @ 2.4 GHz, 10 V | | 70 | | |
| IP3 ($V_{bias} = 2\text{ V}$) [1,3] | | 70 | | dBm |
| IP3 ($V_{bias} = 20\text{ V}$) [1,3] | | 85 | | dBm |
| 2nd Harmonic ($V_{bias} = 2\text{ V}$) [2,3] | | -75 | | dBm |
| 2nd Harmonic ($V_{bias} = 20\text{ V}$) [2,3] | | -85 | | dBm |
| 3rd Harmonic ($V_{bias} = 2\text{ V}$) [2,3] | | -40 | | dBm |
| 3rd Harmonic ($V_{bias} = 20\text{ V}$) [2,3] | | -70 | | dBm |
| Transition Time (Cmin \rightarrow Cmax) [4] | | 80 | | μs |
| Transition Time (Cmax \rightarrow Cmin) [4] | | 70 | | μs |

1. $f_1 = 850\text{ MHz}$, $f_2 = 860\text{ MHz}$, Pin 25 dBm/Tone

2. 850 MHz, Pin +34 dBm

3. IP3 and Harmonics are measured in the shunt configuration in a 50 Ω environment

4. RF_{IN} and RF_{OUT} are both connected to DC ground

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Representative performance data at 25°C for 8.2 pF WLCSP Package

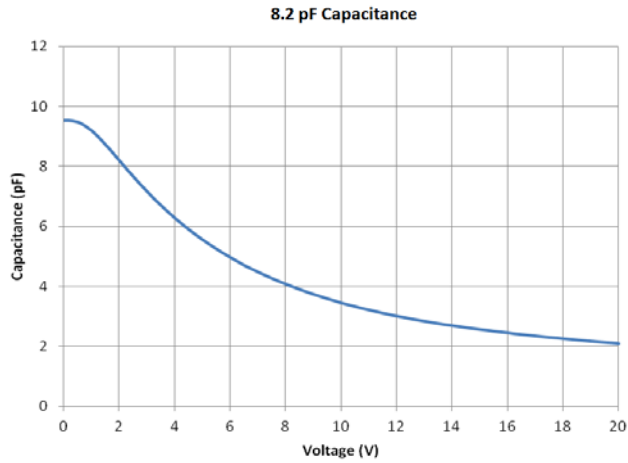


Figure 2. Capacitance

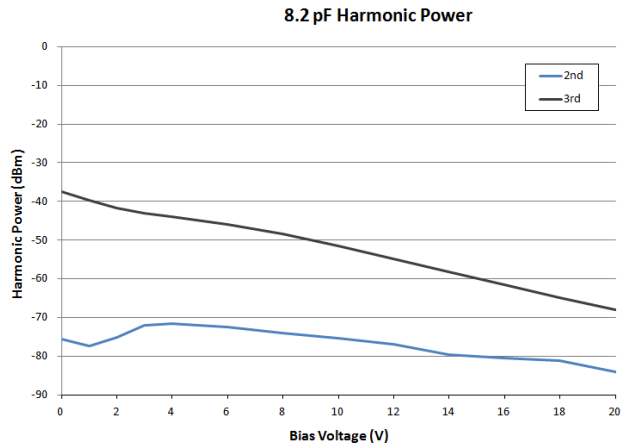


Figure 3. Harmonic Power*

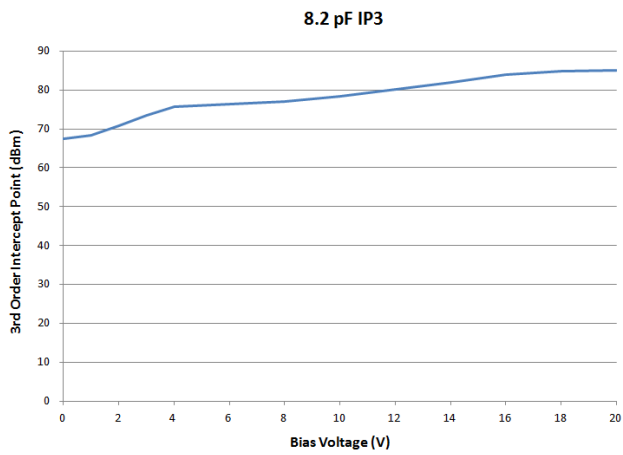


Figure 4. IP3*

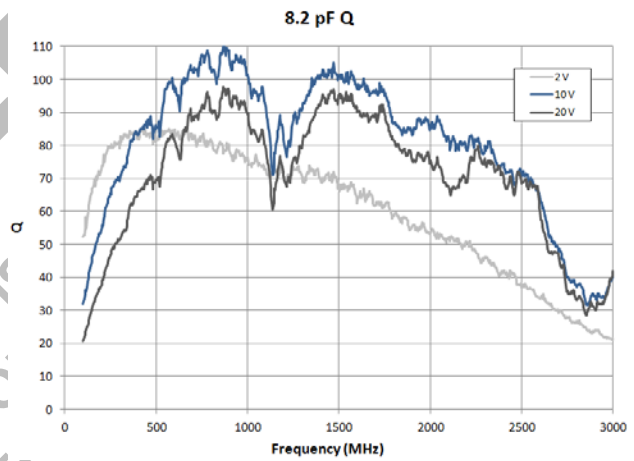


Figure 5. Q*

*The data shown is based on the TCP-1082N device performance, for reference only. The TCP-3082H performance data will be available in the Production Datasheet.

Table 3. ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Units |
|-----------------------------|--------------------------------------|-------|
| Input Power | +40 | dBm |
| Bias Voltage | +25 (Note 5) | V |
| Operating Temperature Range | -30 to +85 | °C |
| Storage Temperature Range | -55 to +125 | °C |
| ESD – Human Body Model | Class 1A JEDEC HBM Standard (Note 6) | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5. WLCSP: Recommended Bias Voltage not to exceed 20 V

6. Class 1A defined as passing 250 V, but may fail after exposure to 500 V ESD pulse

ASSEMBLY CONSIDERATIONS AND REFLOW PROFILE

The following assembly considerations should be observed:

Cleanliness

These chips should be handled in a clean environment.

Electro-static Sensitivity

ON Semiconductor’s PTICs are ESD Class 1A sensitive. The proper ESD handling procedures should be used.

Mounting

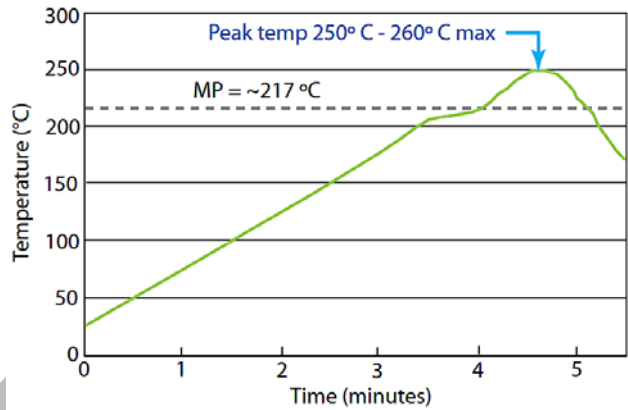
The WLCSP PTIC is fabricated for Flip Chip solder mounting. Connectivity to the RF and Bias terminations on the PTIC die is established through copper pillar posts (53 μm nominal height) topped with lead-free SAC351 solder caps (28 μm nominal height). The PTIC die is RoHS-compliant and compatible with lead-free soldering profile.

Post-reflow Cleaning

Use of ultrasonic cleaning is not recommended for pillared devices as it may lead to premature fatigue failure of the pillars.

Molding

The PTIC die is compatible for over-molding or under-fill.



This reflow profile is a guideline for Pb-free solder materials. Adjustments to this profile are necessary based on specific process requirements and board size, thickness and density. Not to exceed 260° C for 5 seconds.

Figure 6. Reflow Profile

ORIENTATION OF THE PTIC FOR OPTIMUM LOSSES

When configuring the PTIC in your specific circuit design, at least one of the RF terminals must be connected to DC ground. If minimum transition times are required, DC ground on both RF terminals is recommended. To minimize losses, the PTIC should be oriented such that RF2 is at the lower RF impedance of the two RF nodes. A shunt PTIC, for example, should have RF2 connected to RF ground.

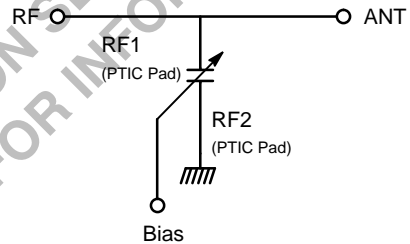


Figure 7. PTIC Orientation Functional Block Diagram

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PART NUMBER DEFINITION

Example: TCP-3082H-DT

| | | | | | | | |
|-----------------------|----------|------------------------------|----------------------------------------------------------------------------------------------------------------------|------------------------|----------|-------------------------|----------------|
| TCP | - | 30 | 82 | H | - | D | T |
| Product Family | | Process Generation | Capacitor Value | Tuning | | Package / Format | Packing |
| TCP | | 10 = Gen 1.0 30 = Gen 3.0 | 12 = 1.2 pF 27 = 2.7 pF 33 = 3.3 pF 39 = 3.9 pF 47 = 4.7 pF 56 = 5.6 pF 68 = 6.8 pF 82 = 8.2 pF | N = Normal H = High | | D = WLCSP Q = QFN | T = T&R |

Table 4. PART NUMBERS

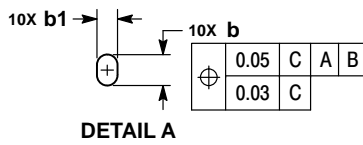
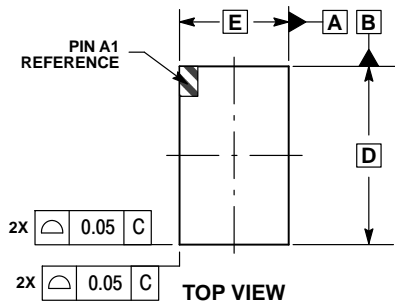
| Part Number | Capacitance | | Package |
|--------------|-------------|------|-----------------|
| | 2 V | 20 V | |
| TCP-3082H-DT | 8.20 | 2.09 | 12-Pillar WLCSP |
| TCP-3082H-QT | 8.20 | 2.09 | 6-Pin QFN |

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

TCP-3082H

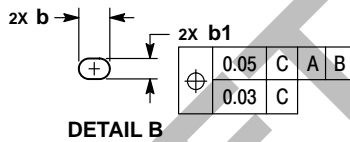
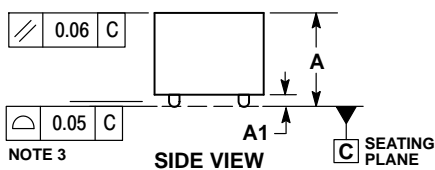
PACKAGE DIMENSIONS

WLCSP12, 1.18x0.72
CASE 567KE
ISSUE O

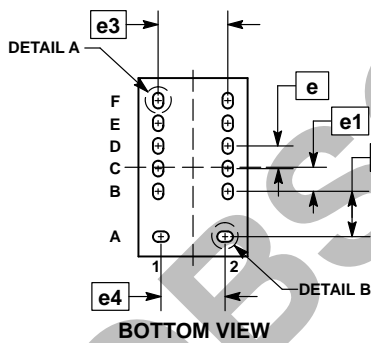
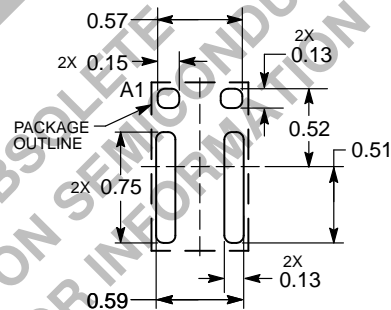


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 0.590 | 0.639 |
| A1 | 0.069 | 0.093 |
| b | 0.079 | 0.129 |
| b1 | 0.044 | 0.094 |
| D | 1.179 BSC | |
| E | 0.722 BSC | |
| e | 0.150 BSC | |
| e1 | 0.159 BSC | |
| e2 | 0.300 BSC | |
| e3 | 0.460 BSC | |
| e4 | 0.425 BSC | |



RECOMMENDED SOLDERING FOOTPRINT*

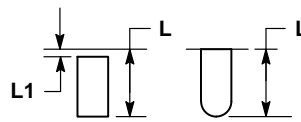
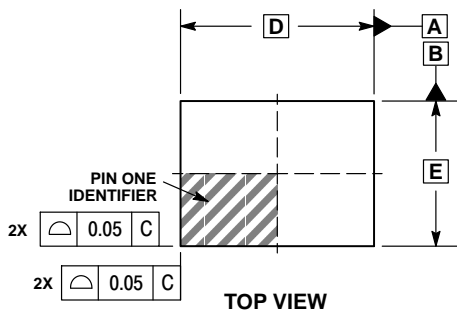


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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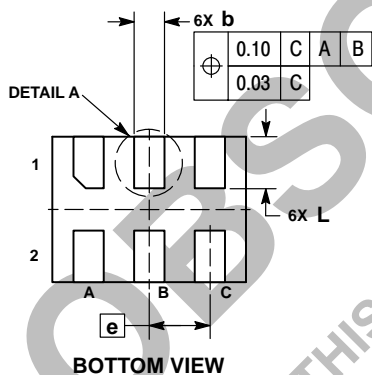
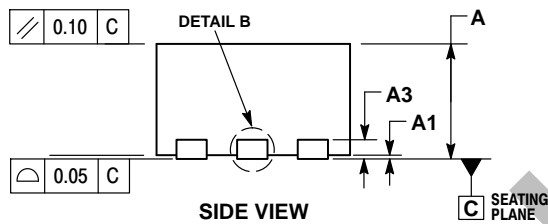
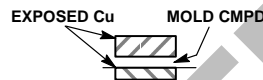
PACKAGE DIMENSIONS

QFN6 1.6x1.2, 0.5P
CASE 485DX
ISSUE A

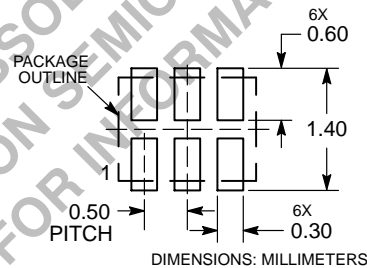


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.90 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.15 REF | |
| b | 0.22 | 0.28 |
| D | 1.60 BSC | |
| E | 1.20 BSC | |
| e | 0.50 BSC | |
| L | 0.39 | 0.46 |
| L1 | — | 0.15 |



RECOMMENDED MOUNTING FOOTPRINT*



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