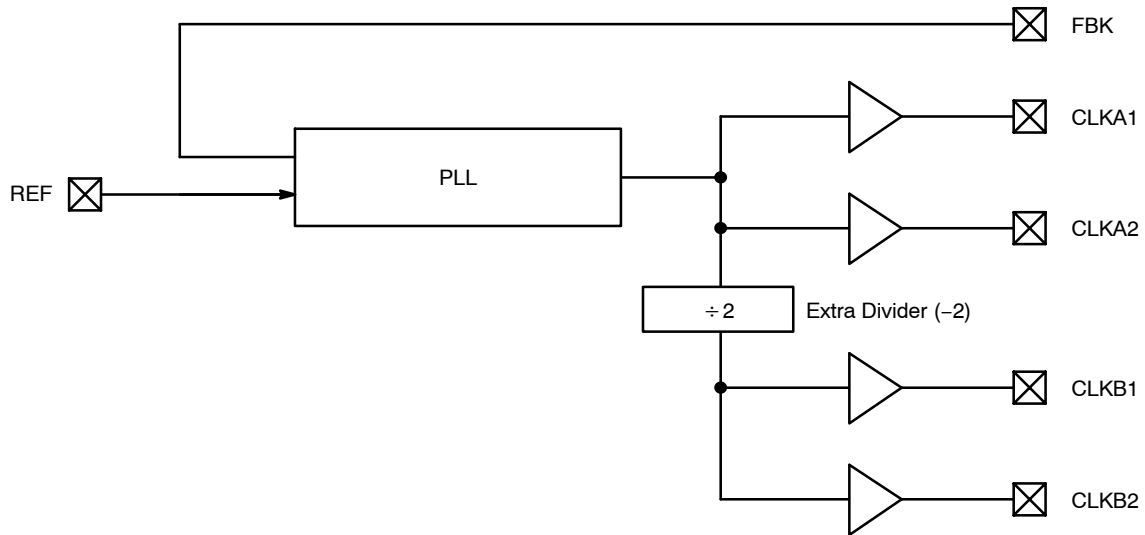


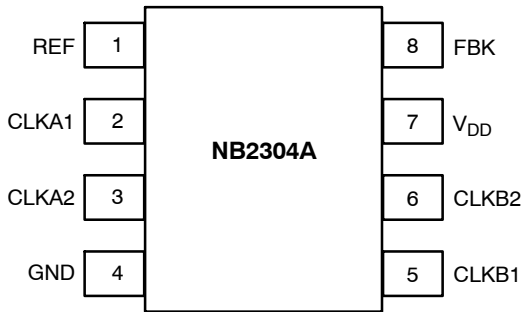
# NB2304A



**Figure 1. Basic Block Diagram**  
(see Figures 10 and 11 for device specific Block Diagrams)

**Table 1. CONFIGURATIONS**

| Device    | Feedback From    | Bank A Frequency | Bank B Frequency |
|-----------|------------------|------------------|------------------|
| NB2304AI1 | Bank A or Bank B | Reference        | Reference        |
| NB2304AI2 | Bank A           | Reference        | Reference ÷ 2    |
| NB2304AI2 | Bank B           | 2 X Reference    | Reference        |



**Figure 2. Pin Configuration**

**Table 2. PIN DESCRIPTION**

| Pin # | Pin Name        | Description                                    |
|-------|-----------------|--|
| 1     | REF (Note 1)    | Input reference frequency, 5 V tolerant input. |
| 2     | CLKA1 (Note 2)  | Buffered clock output, Bank A.                 |
| 3     | CLKA2 (Note 2)  | Buffered clock output, Bank A.                 |
| 4     | GND             | Ground.  |
| 5     | CLKB1 (Note 2)  | Buffered clock output, Bank B.                 |
| 6     | CLKB2 (Note 2)  | Buffered clock output, Bank B.                 |
| 7     | V <sub>DD</sub> | 3.3 V supply.                                  |
| 8     | FBK             | PLL feedback input.                            |

1. Weak pulldown.
2. Weak pulldown on all outputs.

# NB2304A

**Table 3. MAXIMUM RATINGS**

| Parameter   | Min  | Max            | Unit |
|---|------|----------------|------|
| Supply Voltage to Ground Potential                      | -0.5 | +7.0           | V    |
| DC Input Voltage (Except REF)                           | -0.5 | $V_{DD} + 0.5$ | V    |
| DC Input Voltage (REF)                                  | -0.5 | 7              | V    |
| Storage Temperature                                     | -65  | +150           | °C   |
| Maximum Soldering Temperature (10 sec)                  |      | 260            | °C   |
| Junction Temperature                                    |      | 150            | °C   |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) |      | > 2000         | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. OPERATING CONDITIONS**

| Parameter | Description                                 | Min                                  | Max      | Unit |
|-----------|---|--------------------------------------|----------|------|
| $V_{DD}$  | Supply Voltage                              | 3.0                                  | 3.6      | V    |
| $T_A$     | Operating Temperature (Ambient Temperature) | Industrial<br>Commercial<br>-40<br>0 | 85<br>70 | °C   |
| $C_L$     | Load Capacitance, 15 MHz to 100 MHz         |                                      | 30       | pF   |
| $C_L$     | Load Capacitance, from 100 MHz to 133 MHz   |                                      | 15       | pF   |
| $C_{IN}$  | Input Capacitance (Note 3)                  |                                      | 7        | pF   |

3. Applies to both REF Clock and FBK.

**Table 5. ELECTRICAL CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

| Parameter | Description         | Test Conditions  | Min | Max   | Unit          |
|-----------|---------------------|--|-----|-------|---------------|
| $V_{IL}$  | Input LOW Voltage   |  |     | 0.8   | V             |
| $V_{IH}$  | Input HIGH Voltage  |  | 2.0 |       | V             |
| $I_{IL}$  | Input LOW Current   | $V_{IN} = 0\text{ V}$  |     | 50.0  | $\mu\text{A}$ |
| $I_{IH}$  | Input HIGH Current  | $V_{IN} = V_{DD}$  |     | 100.0 | $\mu\text{A}$ |
| $V_{OL}$  | Output LOW Voltage  | $I_{OL} = 8\text{ mA } (-1, -2)$                                 |     | 0.4   | V             |
| $V_{OH}$  | Output HIGH Voltage | $I_{OH} = -8\text{ mA } (-1, -2)$                                | 2.4 |       | V             |
| $I_{DD}$  | Supply Current      | Unloaded outputs 100 MHz REF<br>Select inputs at $V_{DD}$ or GND |     | 45    | mA            |
|           |                     | Unloaded outputs, 66 MHz REF (-1, -2)                            |     | 35    |               |
|           |                     | Unloaded outputs, 33 MHz REF (-1, -2)                            |     | 20    |               |

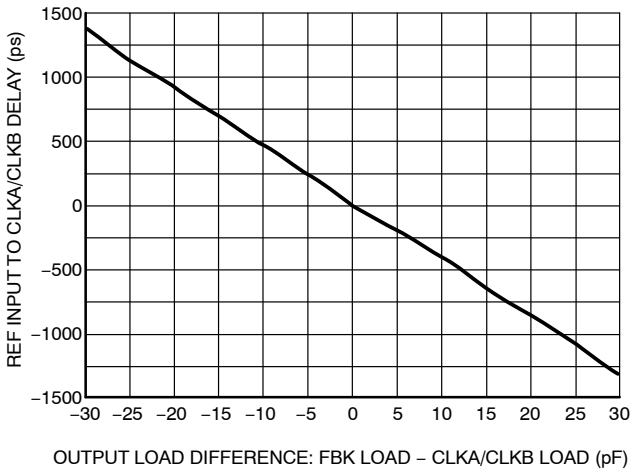
# NB2304A

**Table 6. SWITCHING CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$   
 (All parameters are specified with loaded outputs)

| Parameter  | Description                                       | Test Conditions  | Min      | Typ  | Max          | Unit |
|--|---|--|----------|------|--------------|------|
| $t_1$  | Output Frequency                                  | 30 pF load (all devices)<br>15 pF load (-1, -2)                  | 15<br>15 |      | 100<br>133.3 | MHz  |
| $t_1$  | Duty Cycle = $(t_2 / t_1) * 100$<br>(all devices) | Measured at 1.4 V, $F_{OUT} \leq 66.66\text{ MHz}$<br>30 pF load | 40.0     | 50.0 | 60.0         | %    |
|  |   | Measured at 1.4 V, $F_{OUT} \leq 50\text{ MHz}$<br>15 pF load    | 45.0     | 50.0 | 55.0         |      |
| $t_3$  | Output Rise Time<br>(-1, -2)                      | Measured between 0.8 V and 2.0 V<br>30 pF load                   |          |      | 2.50         | ns   |
|  |   | Measured between 0.8 V and 2.0 V<br>15 pF load                   |          |      | 1.50         |      |
| $t_4$  | Output Fall Time<br>(-1, -2)                      | Measured between 2.0 V and 0.8 V<br>30 pF load                   |          |      | 2.50         | ns   |
|  |   | Measured between 2.0 V and 0.8 V<br>15 pF load                   |          |      | 1.50         |      |
| $t_5$  | Output-to-Output Skew on same Bank<br>(-1, -2)    | All outputs equally loaded                                       |          |      | 200          | ps   |
|  | Output Bank A-to-Output Bank B skew<br>(-1)       | All outputs equally loaded                                       |          |      | 200          |      |
|  | Output Bank A-to-Output Bank B skew<br>(-2)       | All outputs equally loaded                                       |          |      | 400          |      |
| $t_6$  | Delay, REF Rising Edge to FBK Rising Edge         | Measured at $V_{DD}/2$   |          | 0    | $\pm 250$    | ps   |
| $t_7$  | Device-to-Device Skew                             | Measured at $V_{DD}/2$ on the FBK pins of the device             |          | 0    | 500          | ps   |
| $t_J$  | Cycle-to-Cycle Jitter<br>(-1)                     | Measured at 66.67 MHz, loaded outputs,<br>15 pF load             |          |      | 180          | ps   |
|  |   | Measured at 66.67 MHz, loaded outputs,<br>30 pF load             |          |      | 200          |      |
|  |   | Measured at 133.3 MHz, loaded outputs,<br>15 pF load             |          |      | 100          |      |
|  | Cycle-to-Cycle Jitter<br>(-2)                     | Measured at 66.67 MHz, loaded outputs,<br>30 pF load             |          |      | 400          | ps   |
| Measured at 66.67 MHz, loaded outputs,<br>15 pF load |   |  |          | 380  |              |      |
| $t_{LOCK}$   | PLL Lock Time                                     | Stable power supply, valid clock presented on REF and FBK pins   |          |      | 1.0          | ms   |

**Zero Delay and Skew Control**

For applications requiring zero input-output delay, all outputs must be equally loaded.

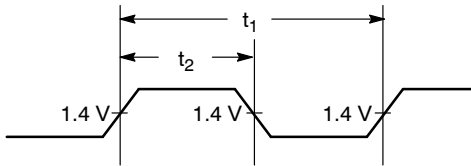


**Figure 3. REF Input to CLKA/CLKB Delay vs. Difference in Loading between FBK Pin and CLKA/CLKB Pins**

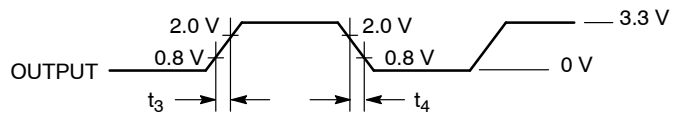
To close the feedback loop of the NB2304A, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input output delay. This is shown in Figure 3.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use Figure 3 to calculate loading differences between the feedback output and remaining outputs. For zero output-output skew, be sure to load outputs equally.

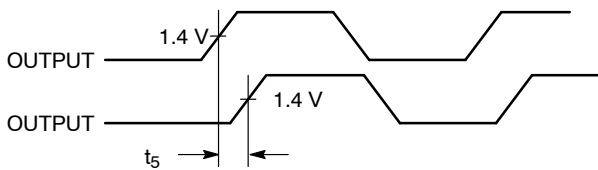
**SWITCHING WAVEFORMS**



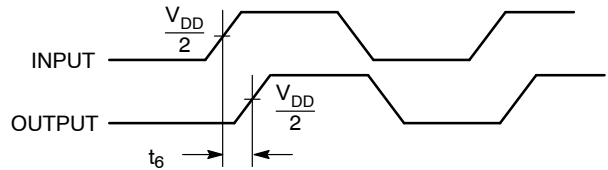
**Figure 4. Duty Cycle Timing**



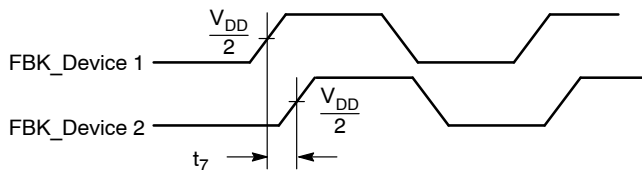
**Figure 5. All Outputs Rise/Fall Time**



**Figure 6. Output - Output Skew**



**Figure 7. Input - Output Propagation Delay**



**Figure 8. Device - Device Skew**

# NB2304A

## TEST CIRCUITS

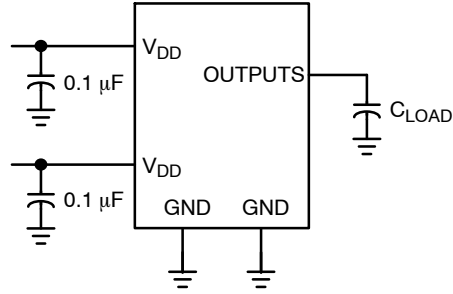


Figure 9. Test Circuit #1

## BLOCK DIAGRAMS

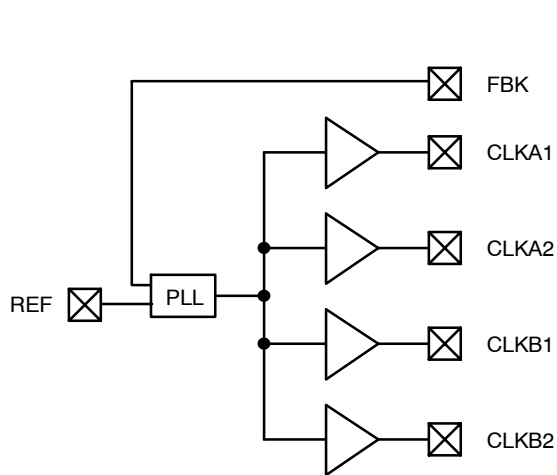


Figure 10. NB2304AI1

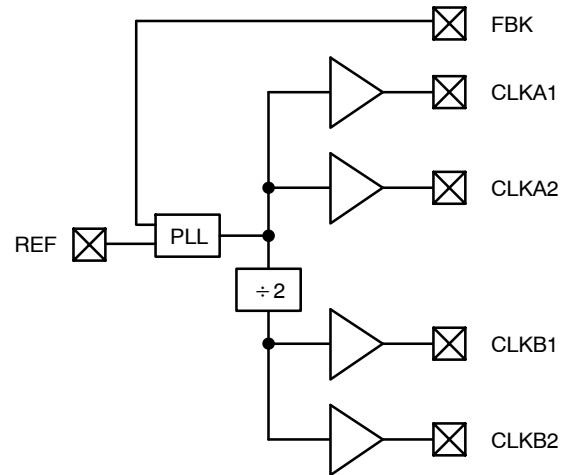


Figure 11. NB2304AI2

## ORDERING INFORMATION

| Device        | Marking | Operating Range         | Package          | Shipping†        | Availability |
|---------------|---------|-------------------------|------------------|------------------|--------------|
| NB2304AI1DR2G | 4I1     | Industrial & Commercial | SOIC-8 (Pb-Free) | 2500 Tape & Reel | Now          |
| NB2304AI2DG   | 4I2     | Industrial & Commercial | SOIC-8 (Pb-Free) | 98 Units / Tube  | Now          |
| NB2304AI2DR2G | 4I2     | Industrial & Commercial | SOIC-8 (Pb-Free) | 2500 Tape & Reel | Now          |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

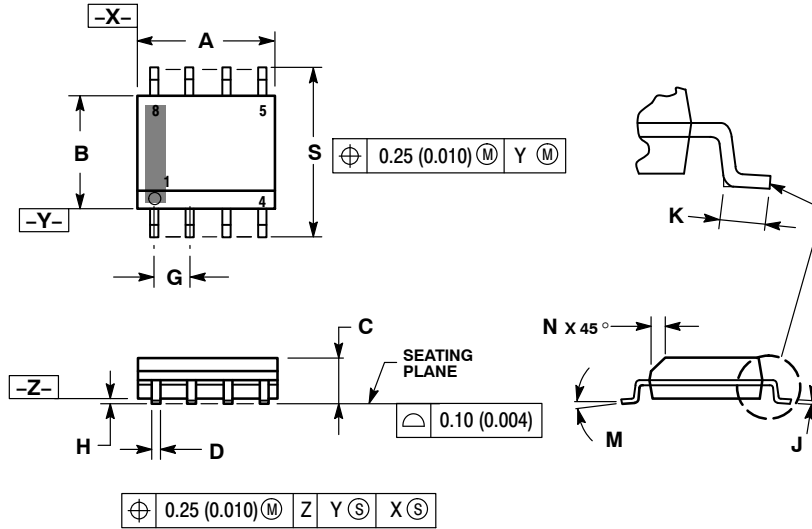
ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

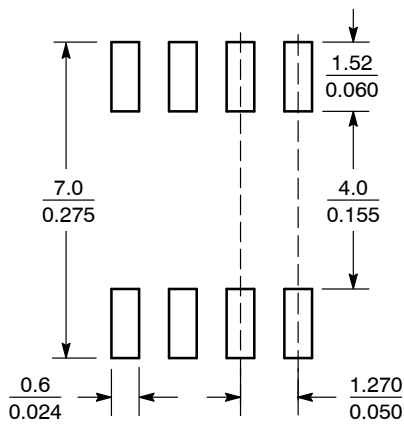
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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