Absolute Maximum Ratings

IN to GND .....-0.3V to +45V
DIM, OUT, EN to GND .....-0.3V to (V_{IN} + 0.3V)
IN Slew Rate (20V < V_{IN} < 45V).....250mV/µs
SDA, SCL (MAX16805), TFN/SDA,
TFP/SCL (MAX16806) to GND.....-0.3V to +6V
CFD, CS+, V5 to GND .....-0.3V to +6V
DGND and CS- to GND .....-0.3V to +0.3V
OUT Short Circuited to GND Duration (V_{IN} < +16V) ..... hour
Maximum Current Into Any Pin (except IN and OUT).....±20mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin Thin QFN
(derate 34.5mW/°C above +70°C) 2758.6mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = V_{EN} = 12V, C_{V5} = 0.1µF, I_{V5} = 0, CS- = GND, R_{SENSE} = 0.56Ω, V_{DIM} = 4V, DGND = GND, TFP/SCL = 5V, TFN/SDA = 0V, SW = CFD = Open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}	(Note 2)		5.5		40	V
Ground Current	I_G	I_{LOAD} = 350mA			2.5	4.5	mA
Shutdown Supply Current	I_{SHDN}	V_{EN} ≤ 0.3V			12	40	µA
Guaranteed Output Current	I_{OUT}	R_{SENSE} = 0.55Ω		350			mA
Output Current Accuracy		35mA < I_{OUT} < 350mA, R_{SENSE} tolerance not included				3.0	%
Dropout Voltage (Note 3)	ΔV_{DO}	I_{OUT} = 350mA, 12V < V_{IN} < 40V			0.4	1.2	V
		I_{OUT} = 350mA, 6.5V < V_{IN} < 12V			0.5	1.5	
Output Current Slew Rate (External PWM Signal at DIM)		Current rising, DIM rising to 4V			17		mA/µs
		Current falling, DIM falling to 0.6V			17		
Short-Circuit Current		V_{OUT} = 0V			600		mA
ENABLE INPUT							
EN Input Current	I_{EN}					100	nA
EN Input-Voltage High	V_{IH}			2.8			V
EN Input-Voltage Low	V_{IL}					0.6	V
Enable Turn-On Time	t_{ON}	EN rising edge to 90% of OUT			225		µs
5V REGULATOR							
Output Voltage Regulation (MAX16806)	V5	6.5V < V_{IN} < 40V	0 < I_{V5} < 0.5mA, SW = GND	4.9	5.1	5.3	V
			0 < I_{V5} < 2mA, SW = open	4.9	5.1	5.3	
Output Voltage Regulation (MAX16805)	V5	0 < I_{V5} < 2mA, 6.5V < V_{IN} < 40V		4.9	5.1	5.3	V
CURRENT SENSE							
Regulated R_{SENSE} Voltage	V_{RSNS}	V_{SENSE} = [V_{CS+} - V_{CS-}], Binning Adjustment register at factory default (0x0F)		192	198	204	mV
Input Current (CS+)		V_{CS+} = 210mV		12			µA

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, C_{V5} = 0.1µF, I_{V5} = 0, CS- = GND, R_{SENSE} = 0.56Ω, V_{DIM} = 4V, DGND = GND, TFP/SCL = 5V, TFN/SDA = 0V, SW = CFD = Open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current (CS-)		V_{CS+} = 210mV			-75	µA
Minimum Regulated V_{SENSE} Programming Range	$V_{SENSE(MIN)}$		99.4	103	106.6	mV
Maximum Regulated V_{SENSE} Programming Range	$V_{SENSE(MAX)}$		192	198	204	
Regulated V_{SENSE} Default Voltage	$V_{SENSE(DEF)}$	Binning Adjustment register at factory default (0x0F)		198		mV
EXTERNAL PWM DIMMING INPUT						
DIM Input Current					0.5	µA
Turn-On Time	t_{ON}	After DIM rising to 4V (Note 4)		28	52	µs
Turn-Off Time	t_{OFF}	After DIM falling to 0.6V (Note 4)		19	38	µs
THERMAL FOLDBACK (MAX16806 with MAX6613)						
Maximum Thermal Foldback Knee Point Programming Range	$TF_{KNEE(MAX)}$		326	335	354	mV
Minimum Thermal Foldback Knee Point Programming Range	$TF_{KNEE(MIN)}$		1143	1174	1213	
Minimum Thermal Foldback Temperature Programming Range	$TF_{(MIN)}$			+60		°C
Maximum Thermal Foldback Temperature Programming Range	$TF_{(MAX)}$			+135		
Thermal Foldback Default Threshold Temperature	V_{TH}	Thermal Foldback Knee Point register at factory default (0x00)		+60		°C
Thermal Foldback Default Threshold Voltage	TF_{VTH}			1.174		V
Minimum Thermal Foldback Slope	$TF_{SL(MIN)}$		3.88	4	4.12	V/V
Maximum Thermal Foldback Slope	$TF_{SL(MAX)}$		15.52	16	16.48	V/V
Thermal Foldback Default Slope		Thermal Foldback Slope Gain register at factory default (0x03)		4		V/V
TFP/SCL (SCL for MAX16805) Voltage Compliance Range	V_{TFP}	I²C interface active	-0.3		V5	V
		Remote thermal sensor active	+0.3		V5	
TFN/SDA (SDA for MAX16805) Voltage Compliance Range	V_{TFN}		-0.3		V5	V
Minimum Thermal Foldback Clamp Current Reduction Range	$TF_{C(MIN)}$	+25°C ≤ T_A ≤ +125°C		40		%

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, C_{V5} = 0.1µF, I_{V5} = 0, CS- = GND, R_{SENSE} = 0.56Ω, V_{DIM} = 4V, DGND = GND, TFP/SCL = 5V, TFN/SDA = 0V, SW = CFD = Open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Thermal Foldback Clamp Current Reduction Range	$TF_{C(MAX)}$	+25°C ≤ T_A ≤ +125°C		100		%
Default Thermal Foldback Clamp Current Reduction Range	TF_{DEF}	Thermal Foldback Clamp register at factory default (0x07), +25°C ≤ T_A ≤ +125°C		40		%
THERMAL PROTECTION						
Thermal Shutdown Temperature	$T_{J(SHDN)}$			+155		°C
Thermal Shutdown Hysteresis				+23		°C
LED CURRENT FOLDBACK						
Minimum Input LED Current Foldback Range	$V_{CFD(MIN)}$			11.4		V
Maximum Input LED Current Foldback Range	$V_{CFD(MAX)}$			16.4		V
LED Current Foldback Default Level	V_{CFD}	LED Current Foldback Threshold register at factory default (0x00)		16.4		V
LED Current Foldback Voltage Step Size		V_{IN} > 11V, CFD register bit 3 = 0		0.71		V/step
		V_{IN} > 11V, CFD register bit 3 = 1		0.355		
INTERNAL RAMP GENERATOR						
Internal RAMP Frequency	f_{RAMP}		176	200	224	Hz
External Sync Frequency Range	f_{DIM}		80		2000	Hz
External Sync Voltage Low					0.4	V
External Sync Voltage High			2.8			V
Output Current Duty Cycle	I_{DC}	V_{DIM} = 0V		0		%
		V_{DIM} > (V_{RAMP} + 0.4V) (MAX16806), V_{DIM} > +3.3V (MAX16805)		100		
Minimum Ramp Peak Programming Range	$V_{RAMP(MIN)}$		1.49	1.55	1.60	V
Maximum Ramp Peak Programming Range	$V_{RAMP(MAX)}$		2.77	2.88	3.00	V
Ramp Peak Default Voltage		Ramp Peak register at factory default (0x07)		2.88		V
Ramp Offset Voltage				210		mV
MOMENTARY SWITCH INTERFACE (SW) (MAX16806)						
SW Pullup Current	I_{SW}	V_{SW} = 0V	1		3	mA
SW Input-Voltage High	V_{IH}	I_{SW} = 100µA	4			V
SW Input-Voltage Low	V_{IL}				0.4	V
Minimum Pulse Width			120			ms
Minimum Debounce Time			40			ms

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 12V, C_{V5} = 0.1µF, I_{V5} = 0, CS- = GND, R_{SENSE} = 0.56Ω, V_{DIM} = 4V, DGND = GND, TFP/SCL = 5V, TFN/SDA = 0V, SW = CFD = Open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM						
V_{IN} Voltage for EEPROM Programming			20	22	24	V
EEPROM Data-Retention Time			10			Years
I²C DIGITAL INPUTS (TFP/SCL, TFN/SDA) (Note 5)						
Logic Input-Voltage High	V_{IH}		2.8			V
Logic Input-Voltage Low	V_{IL}				0.8	V
Input Capacitance				5		pF
SDA Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
I²C INTERFACE TIMING (Figure 1)						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Repeat START Condition Setup Time	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Receive SCL/SDA Rise Time	t_R				300	ns
Receive SCL/SDA Fall Time	t_F				250	ns
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Pulse Width of Spike Suppressed	t_{SP}			50		ns
Transmit SDA Fall Time		I_{SINK} ≤ 6mA, C_B ≤ 400pF (Note 6)			250	ns

Note 1: All devices 100% production tested at T_J = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: Resistors were added from OUT to CS+ to aid with the power dissipation during testing.

Note 3: Dropout is measured as follows: Connect a resistor from OUT to CS+. Connect R_{SENSE} = 0.56Ω from CS+ to CS-. Set V_{IN} = V_{OUT} +3V (record V_{OUT} as V_{OUT1}). Reduce V_{IN} until V_{OUT} = 0.97 x V_{OUT1} (record as V_{IN2} and V_{OUT2}). ΔV_{DO} = V_{IN2} - V_{OUT2}.

Note 4: t_{ON} time includes the delay and the rise time needed for I_{OUT} to reach 90% of its final value. t_{OFF} time is the time needed for I_{OUT} to drop below 10%. See the *Typical Operating Characteristics*. t_{ON} and t_{OFF} are tested with 13Ω from OUT to CS+.

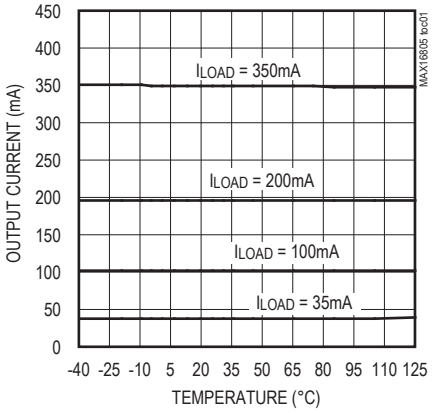
Note 5: TPF/SCL (SCL for MAX16805) and TPN/SDA (SDA for the MAX16805) are I²C interface compatible only when the MAX16805/MAX16806 are the only parts on the bus for production programming.

Note 6: C_B is the total bus capacitance.

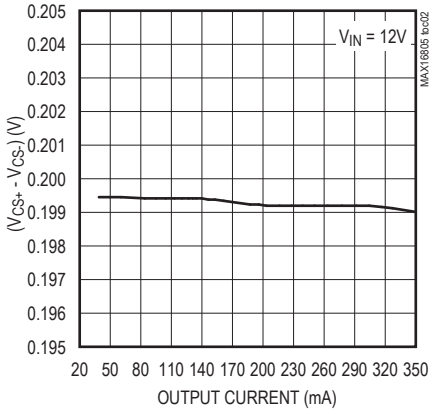
Typical Operating Characteristics

(V_{IN} = 12V, V_{EN} = V_{IN}, C_{V5} = 0.1µF, I_{V5} = 0, CS- = GND, R_{SENSE} = 0.56Ω, connect OUT to CS+, V_{DIM} = 4V, SW = V_{FD} = open, $V_{TFP/SC}$ = 5V, $V_{TFN/SD}$ = GND, DGND = GND. T_A = +25°C, unless otherwise noted.)

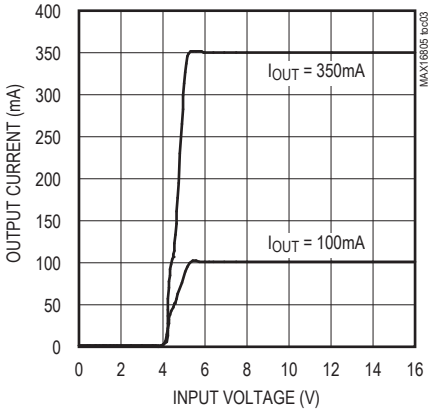
OUTPUT CURRENT vs. TEMPERATURE



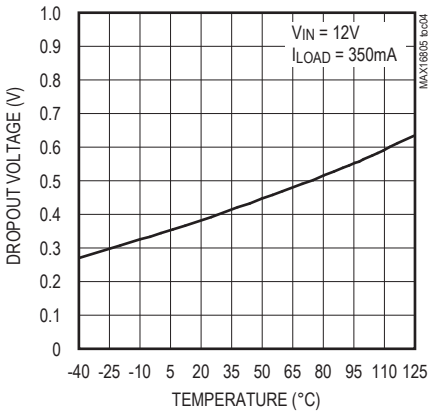
(V_{CS+} - V_{CS-}) vs. OUTPUT CURRENT



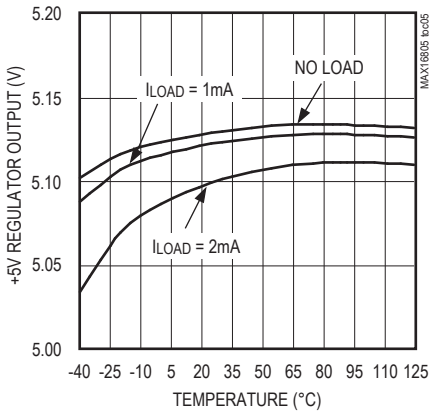
OUTPUT CURRENT vs. INPUT VOLTAGE



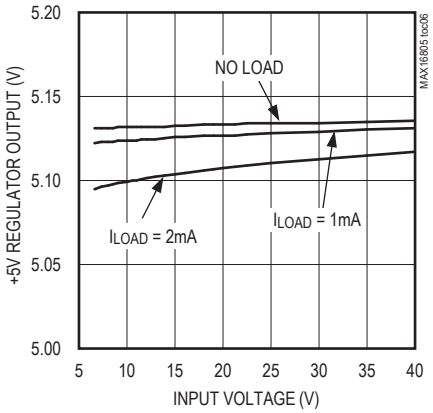
DROPOUT VOLTAGE vs. TEMPERATURE



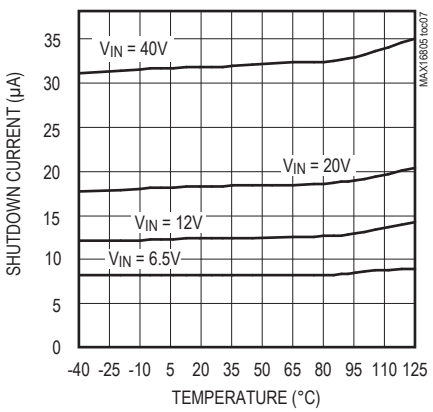
+5V REGULATOR OUTPUT vs. TEMPERATURE



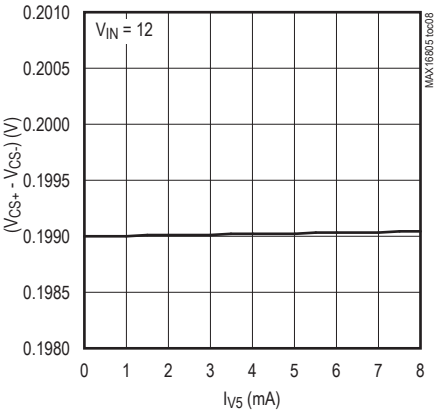
+5V REGULATOR OUTPUT vs. INPUT VOLTAGE



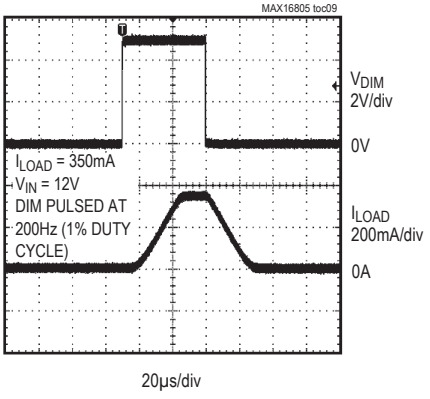
SHUTDOWN CURRENT vs. TEMPERATURE



(V_{CS+} - V_{CS-}) vs. I_{V5}



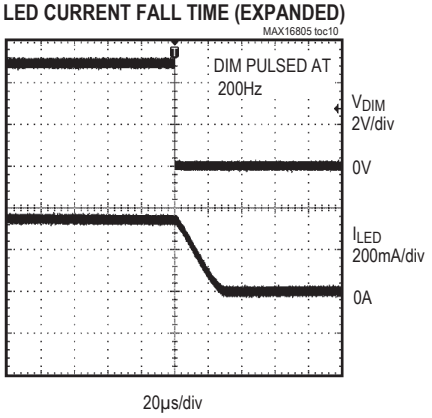
200Hz DIMMED OPERATION



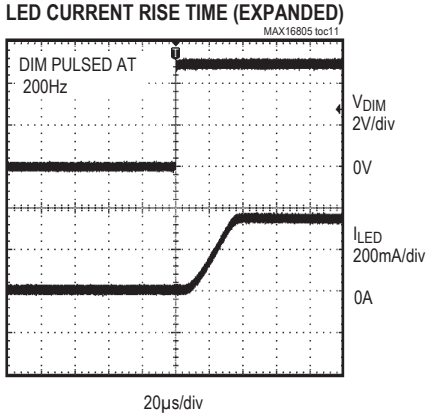
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{EN} = V_{IN}, C_{V5} = 0.1µF, I_{V5} = 0, CS- = GND, R_{SENSE} = 0.56Ω, connect OUT to CS+, V_{DIM} = 4V, SW = V_{FD} = open, $V_{TFP/SC}$ = 5V, $V_{TFN/SD}$ = GND, DGND = GND. T_A = +25°C, unless otherwise noted.)

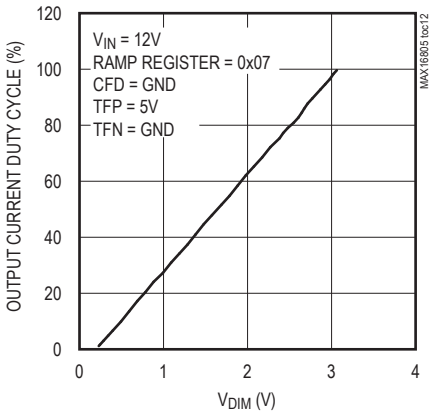
LED CURRENT FALL TIME (EXPANDED)



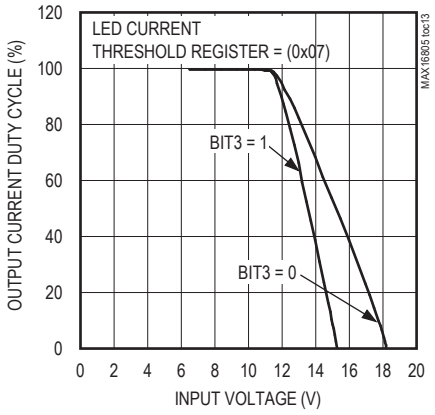
LED CURRENT RISE TIME (EXPANDED)



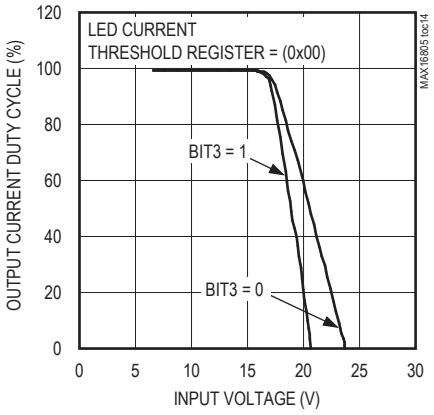
OUTPUT CURRENT DUTY CYCLE vs. ANALOG DIM VOLTAGE



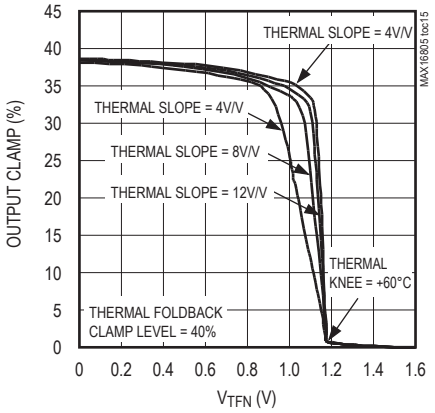
OUTPUT CURRENT DUTY CYCLE vs. INPUT VOLTAGE



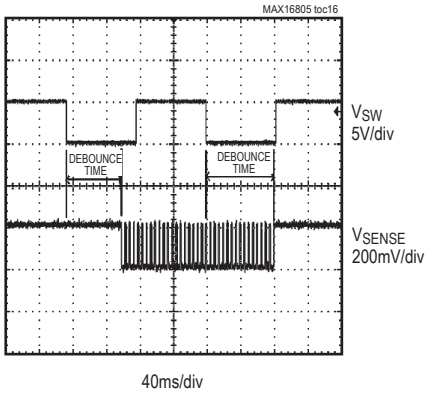
OUTPUT CURRENT DUTY CYCLE vs. INPUT VOLTAGE



OUTPUT CLAMP vs. THERMAL FOLDBACK SLOPE



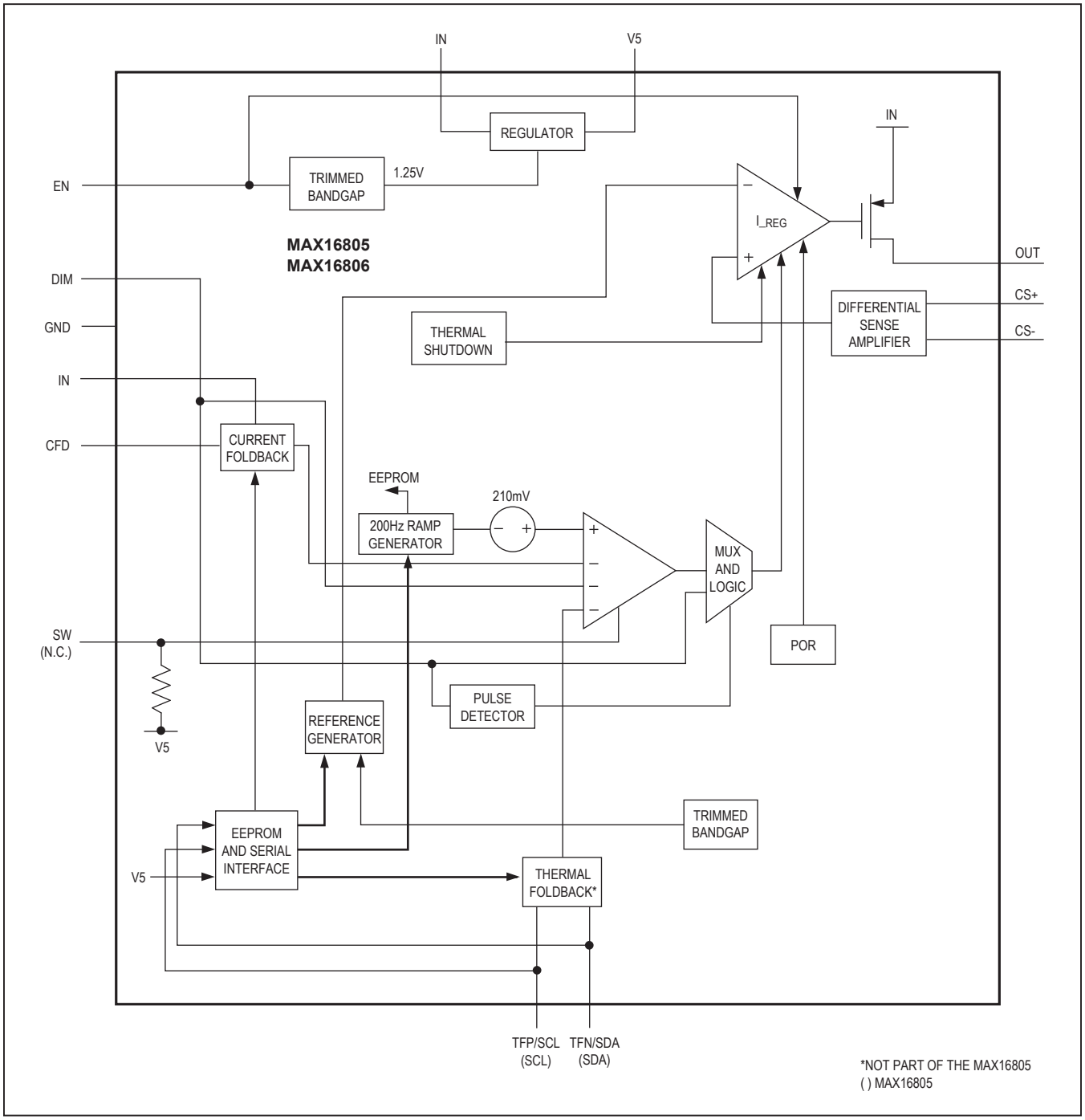
OUTPUT RESPONSE TO SW INPUT



Pin Description

PIN		NAME	FUNCTION
MAX16805	MAX16806		
1, 20	1, 20	OUT	Current Regulated Output. Connect pins 1 and 20.
2, 3	2, 3	IN	Input Supply. Bypass IN with a 0.1µF (min) capacitor to GND. Connect pins 2 and 3.
4	4	CFD	LED Current Foldback Dimming Enable Input. Leave CFD unconnected to enable the current foldback dimming function. Drive CFD low to disable the LED current foldback dimming function.
5	5	DGND	Digital Ground. Connect to GND.
6	—	SCL	I^2C Serial Clock Input
7	—	SDA	I^2C Serial-Data Input/Output
8, 10, 16	8, 10,16	GND	Ground
9, 11, 18	9, 18	N.C.	No Connection. Leave unconnected (internal connection).
12, 15	12, 15	V5	5V Regulated Output. Connect a 0.1µF capacitor from V5 to GND. Connect pin 12 to 15.
13	13	CS+	Positive Input of the Internal Differential Amplifier. Connect the current-sense resistor between CS+ and CS- to program the output current level.
14	14	CS-	Negative Input of the Internal Differential Amplifier. Connect the current-sense resistor between CS- and CS+ to program the output current level.
17	17	DIM	Dimming Input. See the *Dimming Input (DIM)* section.
19	19	EN	Enable Input. Drive EN high to enable the output and the 5V regulator.
—	11	SW	Momentary Switch Interface. See the *Momentary Switch Interface (SW)* section.
—	6	TFP/SCL	Thermal Foldback Positive Input/I^2C Serial Clock Input. See the *Thermal Sensor Inputs/I^2C Interface (TFP/SCL and TFN/SDA)* section.
—	7	TFN/SDA	Thermal Foldback Negative Input/I^2C Serial-Data Input/Output. See the *Thermal Sensor Inputs/I^2C Interface (TFP/SCL and TFN/SDA)* section.
EP	EP	EP	Exposed Pad. Connect to the ground plane for improved power dissipation. Do not use as a ground connection for the part.

Functional Diagram



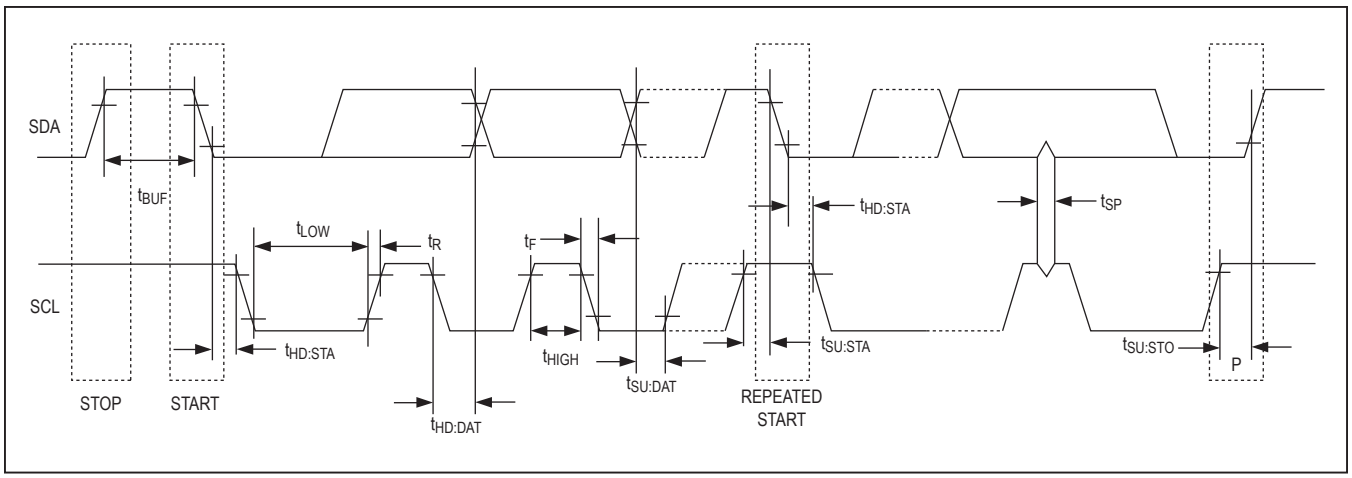


Figure 1. I²C Serial Interface Timing Diagram

Detailed Description

The MAX16805/MAX16806 are constant-current regulators that provide up to 350mA of current to one or more strings of high-brightness LEDs, and have a wide 5.5V to 40V operating input voltage range. The devices feature the I²C interface that allows communication with the internal dynamic registers and EEPROM.

Dynamic registers control the MAX16805/MAX16806 functions and can be updated in real time through the I²C interface. See Table 2 for register addresses. Turning off the input voltage clears the dynamic register contents. To save settings, store them into the EEPROM. The MAX16805/MAX16806 load the stored settings into the dynamic registers at power-up. In addition, during normal operation a write command to the EEPROM Content Transfer register loads the stored settings into the dynamic register. Information stored can be transferred into dynamic registers after issuing a "write" command to the EEPROM Content Transfer register.

The MAX16805/MAX16806's 5V regulator (V5) provides up to 2mA of current to external circuitry. However, the MAX16806's 5V regulator can deliver 2mA of output current only when the momentary switch is not used. When the momentary switch is active, the MAX16806 achieves up to 0.5mA of current. In addition, the MAX16805/MAX16806 feature thermal and output shortcircuit protection. The wide operating voltage range helps protect the device against large transients up to 45V such as those found in load dump situations.

The MAX16805/MAX16806 use a feedback loop to control the output current. The differential voltage across the sense resistor is compared to a fixed reference voltage and the error is amplified to serve as the drive to the internal pass device, see the *Functional Diagram*. The MAX16805/MAX16806 offer a programmable LED current reference using the Binning Adjustment register.

These devices are current controllers internally optimized for driving the impedance range expected from 1 to 10 (or more) high-brightness LEDs.

Dimming Input (DIM)

The MAX16805/MAX16806's dimming input operates with either an analog or PWM control signal. If the pulse detector detects three edges of a PWM signal with a frequency range between 80Hz to 2kHz, the MAX16805/MAX16806 synchronize to external PWM input signal and pulse-width-modulate the LED current. If an analog control signal is applied to DIM, the MAX16805/MAX16806 compare the DC input to an internally generated 200Hz ramp to pulse-width-modulate the LED current. The maximum peak value of the 200Hz ramp can be programmed using the Ramp Peak register. This allows the LED current to be adjusted through the I²C interface from 50% (typ) to 100% in real time when V_{DIM} is 1.54V.

The output current duty cycle is adjustable from 0% to 100% ($0.21V < V_{DIM} < 3.1V$).

Use the following formula to calculate the output current duty cycle:

$$\text{Duty cycle} = (V_{DIM} - 0.21V) / V_{RAMP}$$

The dimming feature can be used for LED brightness adjustment (see the *Typical Operating Circuits*) and theater dimming. If the external PWM signal is used, theater dimming can be achieved by varying the PWM duty cycle. Figure 2 shows a simple circuit that implements theater dimming with a DC input signal.

Thermal Sensor Inputs/I²C Interface (TFP/SCL and TFN/SDA)

The MAX16806 features dual-function inputs, TFP/SCL and TFN/SDA. In programming mode, TFP/SCL and TFN/SDA serve as the I²C serial communication interface. TFP/SCL and TFN/SDA also serve as inputs for analog signals generated by an external temperature sensor such as the MAX6613. When the thermal sensor is not used, connect TFP/SCL and TFN/SDA through 50kΩ resistors to V5 and GND, respectively.

The MAX16805 does not offer dual-function inputs. SCL and SDA are used only to communicate with the MAX16805 through the I²C interface.

Momentary Switch Interface (SW)

The MAX16806 offers a momentary switch (SW) that overrides the analog dimming signal by latching the output current to 100% duty cycle. The MAX16806 does not override external PWM signal at DIM or dimming caused by thermal or LED current foldback. To latch the output current into a 100% duty cycle, press SW once. To restore the initial duty cycle determined by the DC level at DIM, press SW again. The MAX16806 provides a minimum of 1mA of wetting current to the momentary switch.

Overtemperature Protection

The MAX16805/MAX16806 enter a thermal shutdown in the event of overheating. This typically occurs in overload or output short-circuit conditions. When the junction temperature exceeds T_J = +155°C (typ), the internal thermal protection circuitry turns off the pass device. The MAX16805/MAX16806 recover from thermal shutdown once the junction temperature drops by +23°C (typ). This feature allows self-protection by thermally cycling in the event of a short-circuit or overload condition.

Digital Interface

The MAX16805/MAX16806 feature an I²C, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX16805/MAX16806 and the master device at rates up to 400kHz.

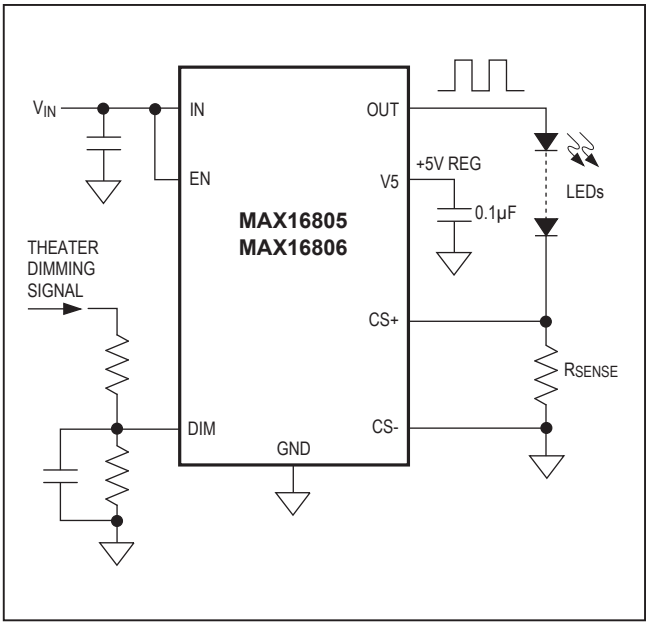


Figure 2. Theater Dimming Light

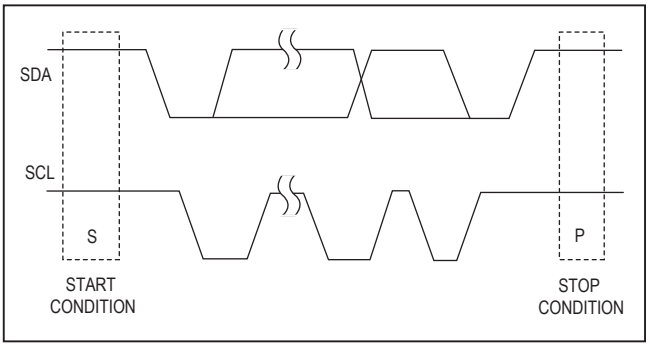


Figure 3. I²C Communication Start and Stop Conditions

The master (typically a microcontroller) initiates data transfer on the bus and generates SCL.

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master controller signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. The master controller issues a STOP condition by transitioning the SDA from low to high while SCL is high, when it finishes communicating with the slave. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt each byte of data (Figure 5). Therefore, each byte effectively transferred requires 9 bits. The master controller generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line remains stable low during the high period of the clock pulse.

Slave Address

The MAX16805/MAX16806 have a 7-bit-long slave address (Figure 6, Table 1). The 8th bit following the 7- bit slave address is the R/$\overline{W}$ bit. Set the R/$\overline{W}$ bit low for a write command and high for a read command.

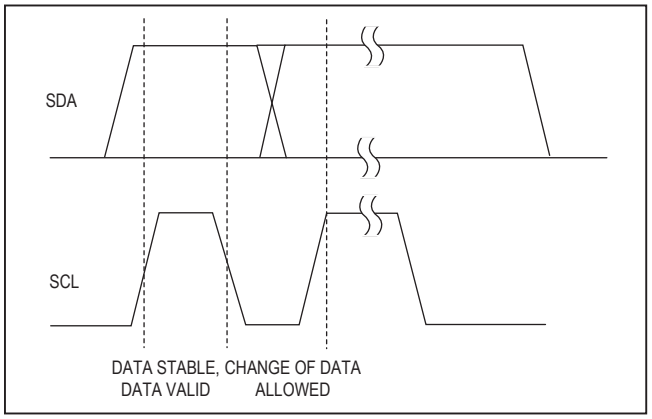


Figure 4. Bit Transfer

Table 1. Slave Address

WRITE ADDRESS (HEX)	READ ADDRESS (HEX)
0xEE	0xEF

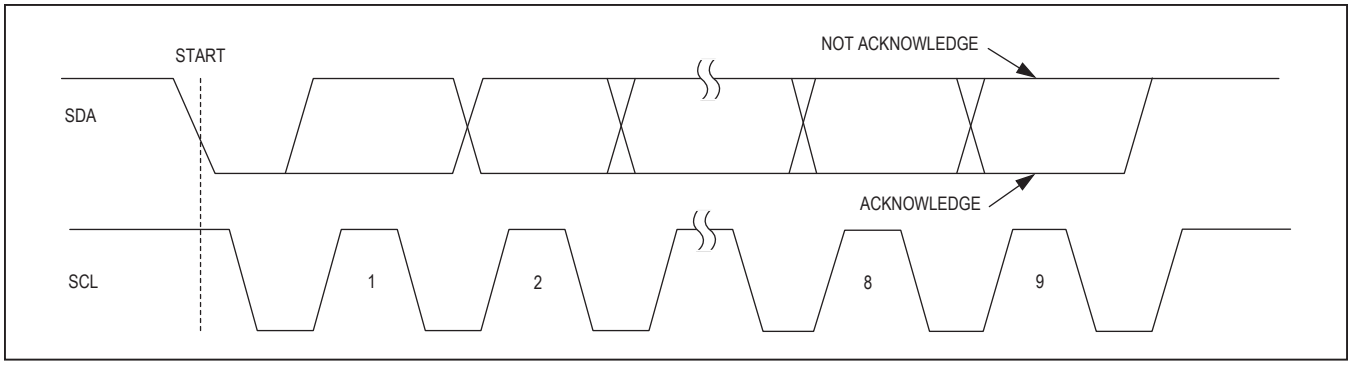


Figure 5. Acknowledge

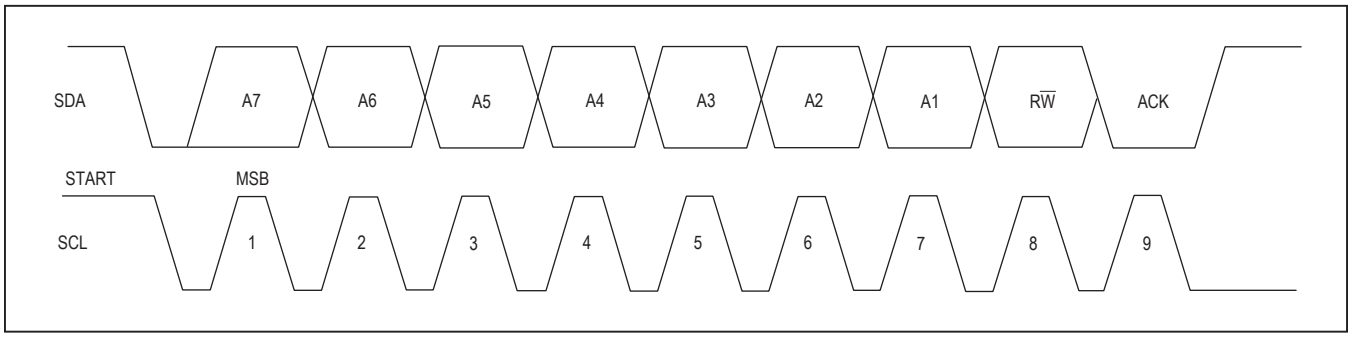


Figure 6. Slave Address

Message Format

Write to the MAX16805/MAX16806 by transmitting the device's slave address with R/$\overline{W}$, 8th bit set to zero followed by at least 1 byte of information (Figure 7). The first byte of information is the command byte. The bytes received after the command byte are the data bytes. The first data byte goes into the internal register as selected by the command byte (Figure 8). If there is more than one data byte, the MAX16805/MAX16806 auto-increment to the next register address locations to write the subsequent data bytes. The MAX16805/MAX16806 auto-increment up to the register address 0x05, EEPROM Content Transfer register.

A read operation is performed as follows:

After the START condition (S), a 7-bit slave ID is sent followed by an 8th bit (R/$\overline{W}$) set to zero. A register address is then sent to specify the address location from which the read has to take place. To complete a read operation, the master needs to generate a repeated START (Sr) followed by the 7-bit slave ID but with the 8th bit (R/$\overline{W}$) set to "1" this time indicating a read operation. On the other hand, a read operation can be performed by sending in the 7-bit slave ID followed by an 8th bit (R/$\overline{W}$) set to "1" if the current address location happens to be the address location from which data needs to be read.

Table 2. Registers Address

REGISTER NAME	REGISTER ADDRESS	NO. OF BITS/ REGISTER
Binning Adjustment	0x00	4
Ramp Peak	0x01	3
LED Current Foldback Threshold (LED_CFT)	0x02	4
Thermal Foldback Knee Point	0x03	4
Thermal Foldback Slope Gain	0x04	2
Thermal Foldback Clamp Level	0x05	3
EEPROM Content Transfer	0x06	—
EEPROM Program Enable	0x08	—
Password Register	0xFF	—

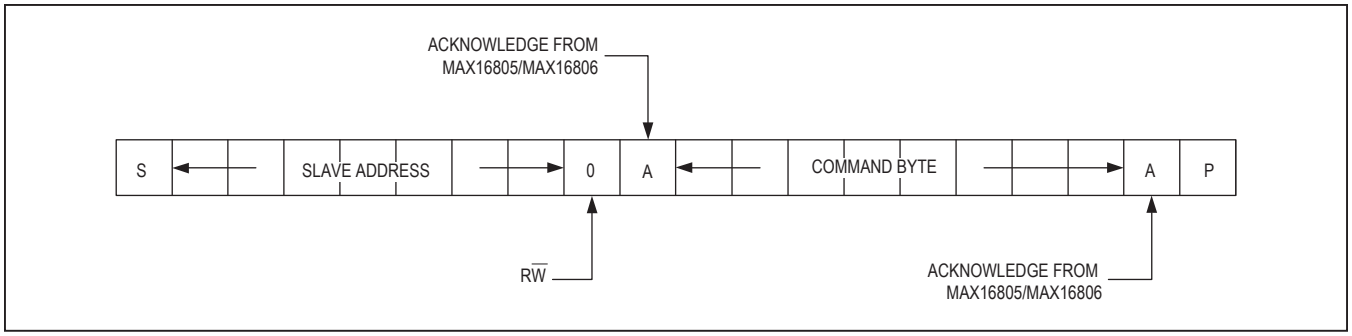


Figure 7. Command Byte Received

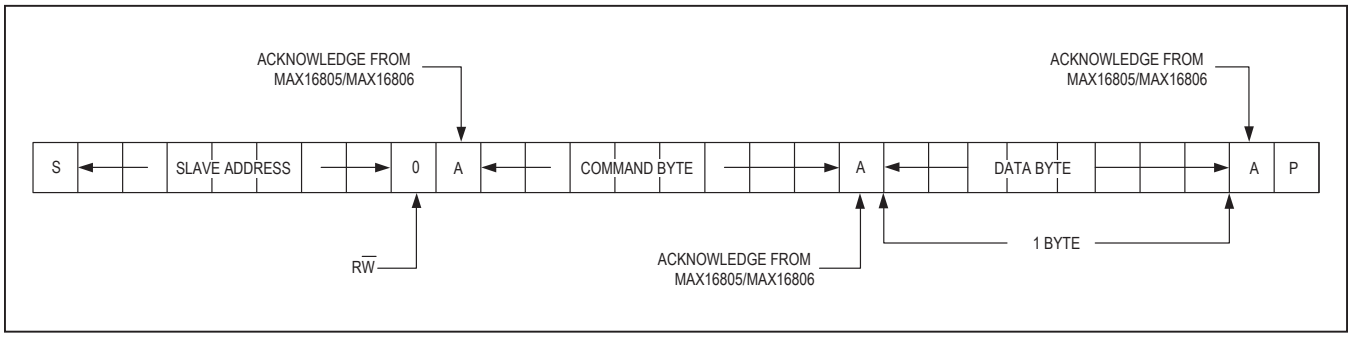


Figure 8. Command and a Single Data Byte Received

Binning Adjustment Register (0x00)

The Binning Adjustment register is a 4-bit register that sets the differential regulation voltage reference between CS+ and CS-. Only the first 4 bits of the data byte update the Binning Adjustment register. The remaining 4 bits are ignored. See Table 3. The factorydefault register value is 198mV.

Ramp Peak Register (0x01), MAX16806

The Ramp Peak register is a 3-bit register that sets the maximum peak value of an internally 200Hz generated ramp. The ramp signal can be programmed for a peak value of 1.55V to 2.88V. Only the first 3 bits of the data byte update the Ramp Peak register. The remaining 5 bits are ignored (see Table 4). The factory-default register value is 2.88V.

LED Current Foldback Threshold (LED_CFT) Register (0x02)

LED_CFT is a 4-bit register that sets the threshold for the onset of the LED current foldback operation. Only the first 3 bits of the data byte program the LED_CFT register. Bit 3, not shown in Table 5, sets the LED current foldback range. The MAX16805/MAX16806 start dimming the LED current when the input voltage exceeds the LED current foldback threshold. For bit 3 = 0, the dimming range is 1.2 times the programmed ramp peak voltage. For bit 3 = 1, the dimming range is 2.4 times the programmed ramp peak. To disable the LED current foldback feature of the MAX16805/MAX16806 connect CFT to GND. The factory-default register value is 16V.

Table 3. Binning Adjustment

REGULATION VOLTAGE (mV)	BIT 3	BIT 2	BIT 1	BIT 0	HEX
103.0	0	0	0	0	(0x00)
109.0	0	0	0	1	(0x01)
115.4	0	0	1	0	(0x02)
121.8	0	0	1	1	(0x03)
128.2	0	1	0	0	(0x04)
134.6	0	1	0	1	(0x05)
141.0	0	1	1	0	(0x06)
147.4	0	1	1	1	(0x07)
153.7	1	0	0	0	(0x08)
160.1	1	0	0	1	(0x09)
166.5	1	0	1	0	(0x0A)
173.0	1	0	1	1	(0x0B)
179.3	1	1	0	0	(0x0C)
185.7	1	1	0	1	(0x0D)
192.1	1	1	1	0	(0x0E)
198.0	1	1	1	1	(0x0F)

Table 4. Ramp Peak Value

RAMP END POINT (V)	BIT 2	BIT 1	BIT 0	HEX
1.55	0	0	0	(0x00)
1.74	0	0	1	(0x01)
1.93	0	1	0	(0x02)
2.12	0	1	1	(0x03)
2.32	1	0	0	(0x04)
2.51	1	0	1	(0x05)
2.70	1	1	0	(0x06)
2.88	1	1	1	(0x07)

Table 5. LED Current Foldback Threshold

CURRENT FOLDBACK THRESHOLD (V)	BIT 2	BIT 1	BIT 0	HEX
16.4	0	0	0	(0x00)
15.7	0	0	1	(0x01)
15.0	0	1	0	(0x02)
14.3	0	1	1	(0x03)
13.5	1	0	0	(0x04)
12.8	1	0	1	(0x05)
12.1	1	1	0	(0x06)
11.4	1	1	1	(0x07)

Thermal Foldback Knee Point (TFK) Register (0x03), MAX16806

The TFK register is a 4-bit register that sets the thermal knee. Only the first 4 bits of the data byte program the TFK register. The remaining 4 bits are ignored (see Table 6). The MAX16806 initiates dimming once the differential voltage between TFP/SCL and TFN/SDA drops below the programmed thermal foldback knee. The factory-default register value is 1.174V, which corresponds to the MAX6613 thermal sensor output to +60°C.

Thermal Foldback Slope Gain Register (0x04), MAX16806

Thermal Foldback Slope Gain register is a 2-bit register that sets the gain after the thermal foldback knee. Only the first 2 bits of the data byte program the Thermal Foldback Slope Gain register. The remaining 6 bits are ignored (see Table 7). The factory-default register value is 4V/V.

Table 6. Thermal Foldback Knee

THERMAL FOLDBACK KNEE POINT (°C) (MAX6613)	THERMAL FOLDBACK KNEE POINT (mV)	BIT 3	BIT 2	BIT 1	BIT 0	HEX
60	1174	0	0	0	0	(0x00)
65	1118	0	0	0	1	(0x01)
70	1062	0	0	1	0	(0x02)
75	1006	0	0	1	1	(0x03)
80	950	0	1	0	0	(0x04)
85	894	0	1	0	1	(0x05)
90	838	0	1	1	0	(0x06)
96	782	0	1	1	1	(0x07)
101	726	1	0	0	0	(0x08)
106	670	1	0	0	1	(0x09)
111	615	1	0	1	0	(0x0A)
116	559	1	0	1	1	(0x0B)
121	503	1	1	0	0	(0x0C)
126	447	1	1	0	1	(0x0D)
131	391	1	1	1	0	(0x0E)
136	335	1	1	1	1	(0x0F)

Table 7. Thermal Foldback Slope Gain

THERMAL FOLDBACK SLOPE GAIN (V/V)	BIT 1	BIT 0	HEX
16	0	0	(0x00)
12	0	1	(0x01)
8	1	0	(0x02)
4	1	1	(0x03)

Thermal Foldback Clamp Level Register (0x05), MAX16806

Thermal Foldback Clamp Level is a 3-bit register that sets the minimum percentage of the LED current. Only the first 3 bits of the data byte program the Thermal Foldback Clamp Level register. The remaining 5 bits are ignored. See Table 8. The factory-default register value is 40%.

EEPROM Content Transfer Register (0x06)

The MAX16805/MAX16806 use the EEPROM Content Transfer register to transfer data from the EEPROM to the dynamic registers. A write command issued to this register transfers data from the EEPROM to the dynamic registers. Data bytes written to the EEPROM Content Transfer register do not have any significance. At power-up, the EEPROM content is automatically loaded into the dynamic registers.

EEPROM Program Enable Register (0x08)

The EEPROM Program Enable register enables the EEPROM for programming. Write to the EEPROM Programming Enable register to initiate the EEPROM programming cycle. Data written to the register does not have any significance, however, it must be issued following a write command **[(0xFF), (0xCA)]** to the Password register.

Table 8. Thermal Foldback Clamp Level

THERMAL FOLDBACK CLAMP LEVEL (%)	BIT 2	BIT 1	BIT 0	HEX
100	0	0	0	(0x00)
91	0	0	1	(0x01)
83	0	1	0	(0x02)
74	0	1	1	(0x03)
66	1	0	0	(0x04)
57	1	0	1	(0x05)
49	1	1	0	(0x06)
40	1	1	1	(0x07)

Applications Information

Programming the LED Current

The MAX16805/MAX16806 use a sense resistor across CS+ and CS- to set the LED current. The differential sense amplifier connected across R_{SENSE} provides ground-loop immunity and low-frequency noise rejection. The LED current is given by the equation below:

$$I_{LED} = V_{SENSE} / R_{SENSE}$$

V_{SENSE} is programmable from 103mV to 198mV using I^2C.

Programming EEPROM

Set V_{IN} to 22V before initiating the EEPROM programming. The MAX16805/MAX16806 use dynamic registers to program the EEPROM. Once the desired dynamic registers have been updated with a setting, write the data byte (0xCA) to the Password register (0xFF). The data byte (0xCA) enables the EEPROM programming mode. Any other data byte except the (0xCA) disables the EEPROM programming mode. To transfer data from dynamic registers to the EEPROM, write to EEPROM Program Enable register (0x08).

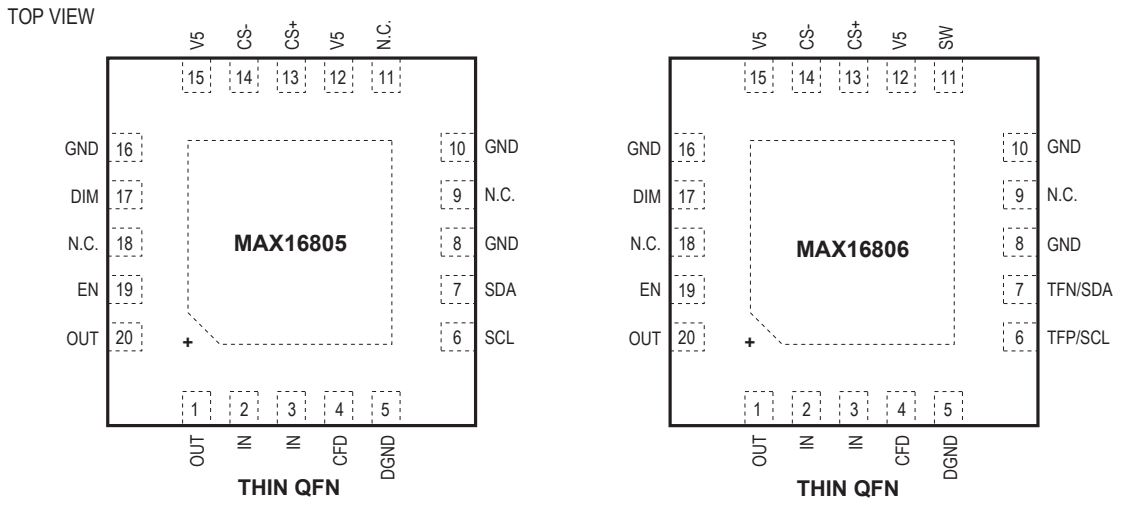
Input Voltage Considerations

For proper operation, the minimum input voltage must always be:

$$V_{IN(MIN)} > V_{SENSE} + V_{FT(MAX)} + \Delta V_{DO(MAX)}$$

where $V_{FT(MAX)}$ is the total forward voltage of all series connected LEDs and $\Delta V_{DO(MAX)}$ is the maximum drop output voltage.

Pin Configurations



Chip Information

PROCESS: BiCMOS-DMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2055MN+5	21-0140	90-0011

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	9/14	Removed automotive references from the *General Description, Applications,* and *Detailed Description* sections	1, 10

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