

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 68\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 200\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.5	2.2	2.5	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_D = 610\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	2	2.8	4	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ )	$V_{DS(on)}$	0.2	0.3	0.4	Vdc

**Dynamic Characteristics** <sup>(1)</sup>

Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	1.5	—	pF
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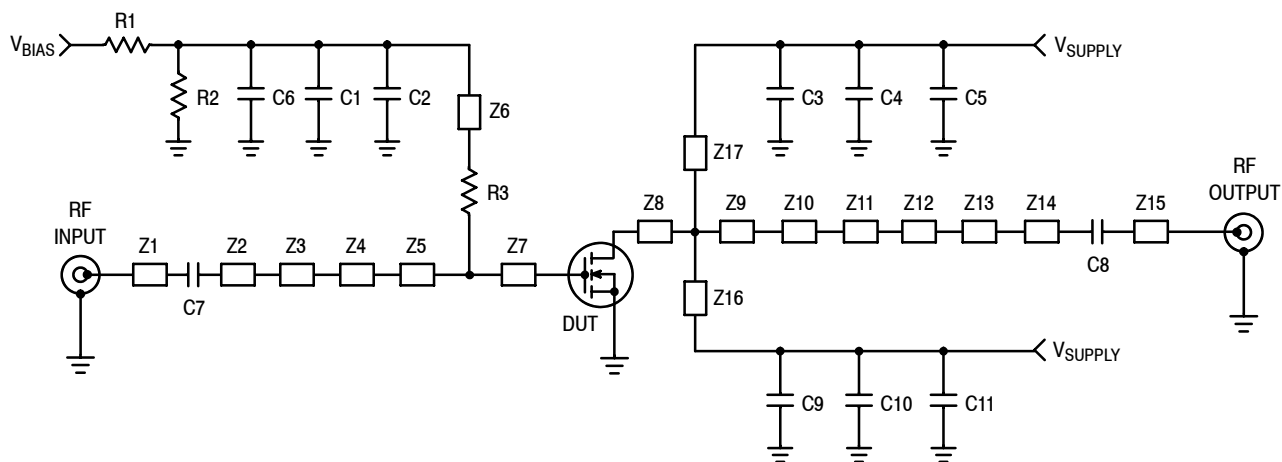
**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 610\text{ mA}$ ,  $P_{out} = 12\text{ W Avg.}$ ,  $f_1 = 1930\text{ MHz}$ ,  $f_2 = 1932.5\text{ MHz}$ , 2-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carriers. ACPR measured in 30 kHz Channel Bandwidth @  $\pm 885\text{ kHz}$  Offset. IM3 measured in 1.2288 MHz Channel Bandwidth @  $\pm 2.5\text{ MHz}$  Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF.

Power Gain	$G_{ps}$	14.5	16	18.5	dB
Drain Efficiency	$\eta_D$	24.5	26	—	%
Intermodulation Distortion	IM3	—	-37	-35	dBc
Adjacent Channel Power Ratio	ACPR	—	-51	-48	dBc
Input Return Loss	IRL	—	-12	-10	dB

1. Part is internally matched both on input and output.

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Z1	0.250" x 0.083" Microstrip	Z11	0.225" x 0.083" Microstrip
Z2	0.750" x 0.083" Microstrip	Z12	0.325" x 0.500" Microstrip
Z3	0.375" x 0.425" Microstrip	Z13	0.450" x 0.083" Microstrip
Z4	0.370" x 0.083" Microstrip	Z14	0.300" x 0.245" Microstrip
Z5	0.365" x 1.000" Microstrip	Z15	0.195" x 0.083" Microstrip
Z6	0.650" x 0.080" Microstrip	Z16	1.150" x 0.070" Microstrip
Z7, Z8	0.115" x 1.000" Microstrip	Z17	1.150" x 0.083" Microstrip
Z9	0.240" x 1.000" Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$
Z10	0.310" x 0.315" Microstrip		

Figure 1. MRF6S19060NR1(NBR1) Test Circuit Schematic

Table 6. MRF6S19060NR1(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	100 nF Chip Capacitor	CDR33BX104AKYS	Kemet
C2, C3, C7, C8, C9	6.8 pF Chip Capacitors	ATC100B6R8BT250XT	ATC
C4, C5, C6, C10, C11	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
R1	1 k $\Omega$ , 1/4 W Chip Resistor	CRCW12061001FKEA	Vishay
R2	10 k $\Omega$ , 1/4 W Chip Resistor	CRCW12061002FKEA	Vishay
R3	10 $\Omega$ , 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

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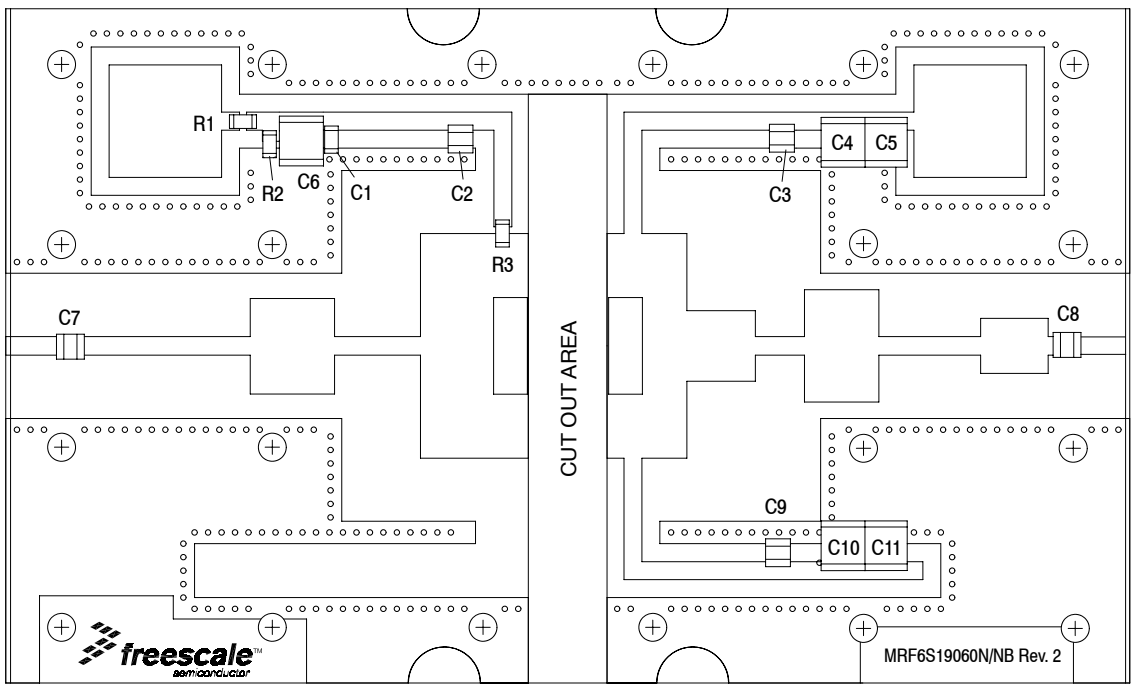


Figure 2. MRF6S19060NR1(NBR1) Test Circuit Component Layout

### TYPICAL CHARACTERISTICS

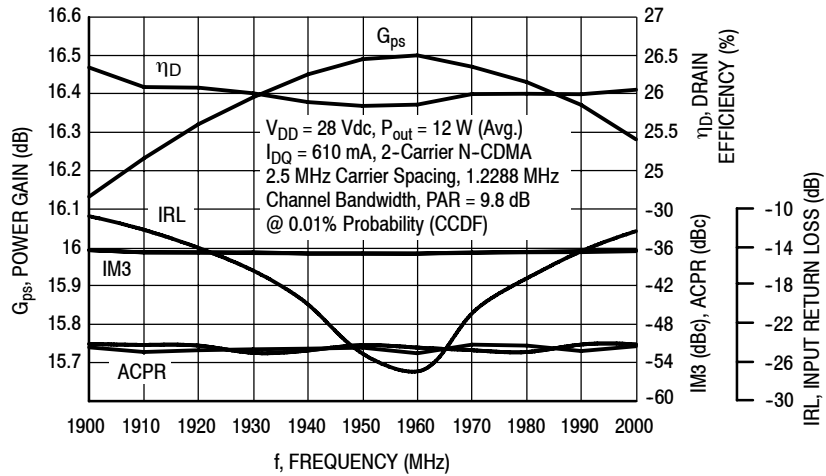


Figure 3. 2-Carrier N-CDMA Broadband Performance @  $P_{out} = 12$  Watts Avg.

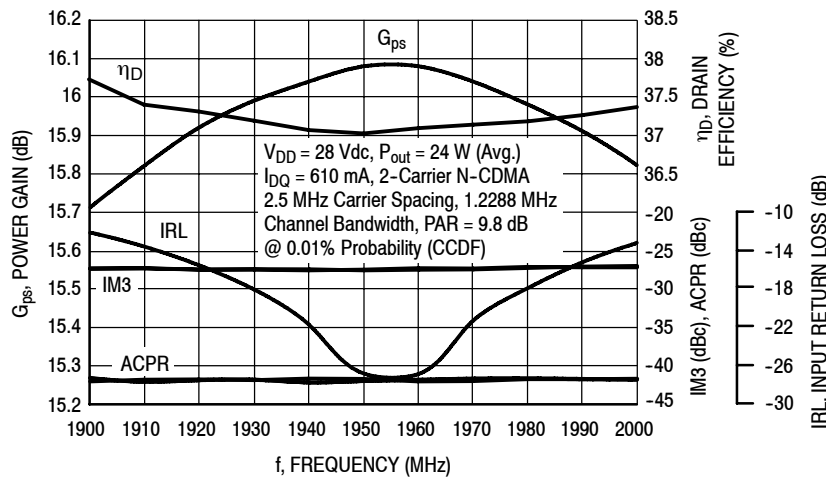


Figure 4. 2-Carrier N-CDMA Broadband Performance @  $P_{out} = 24$  Watts Avg.

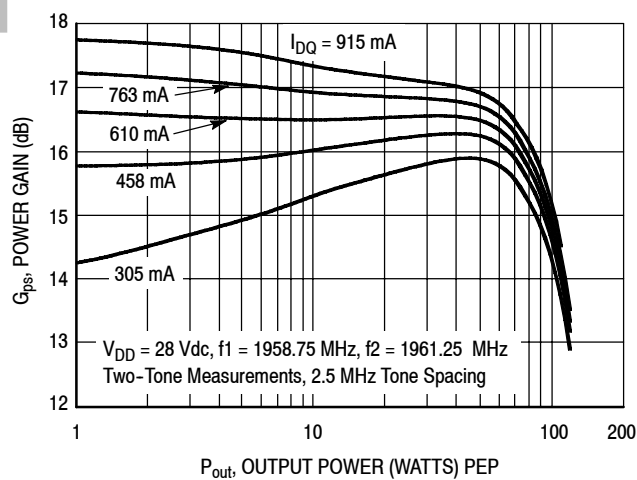


Figure 5. Two-Tone Power Gain versus Output Power

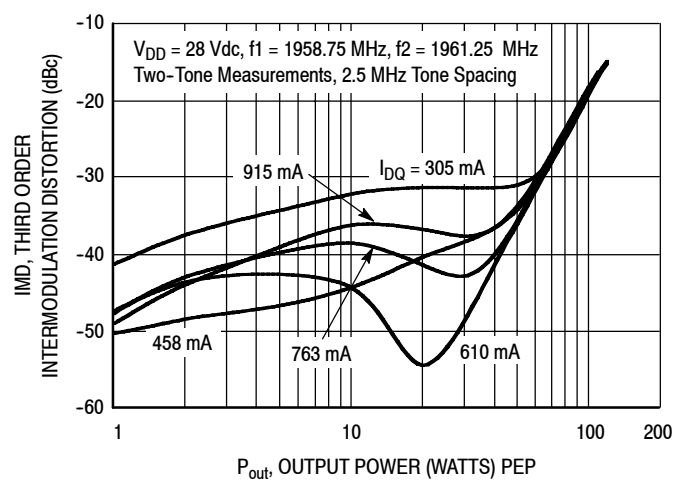
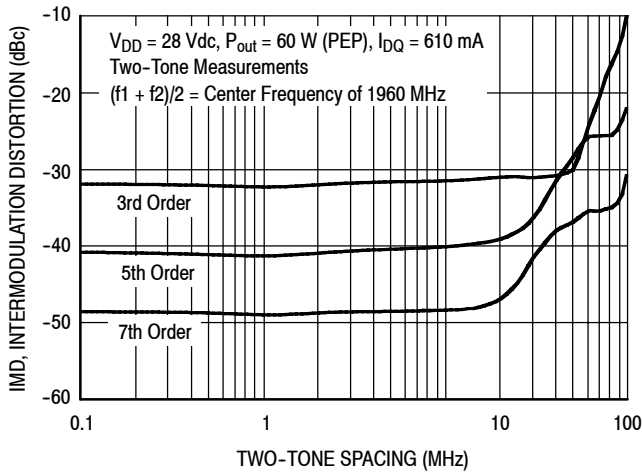


Figure 6. Third Order Intermodulation Distortion versus Output Power

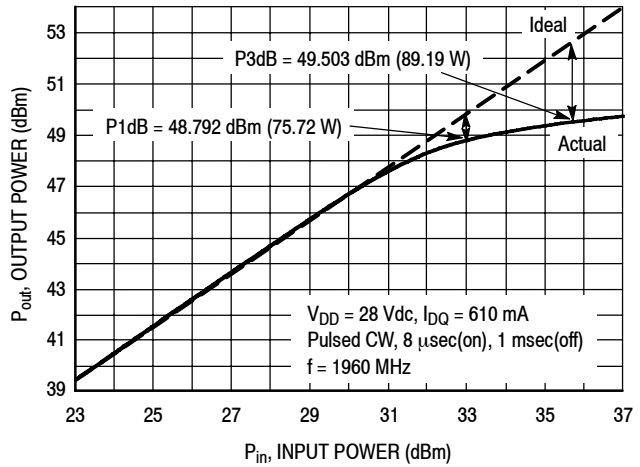
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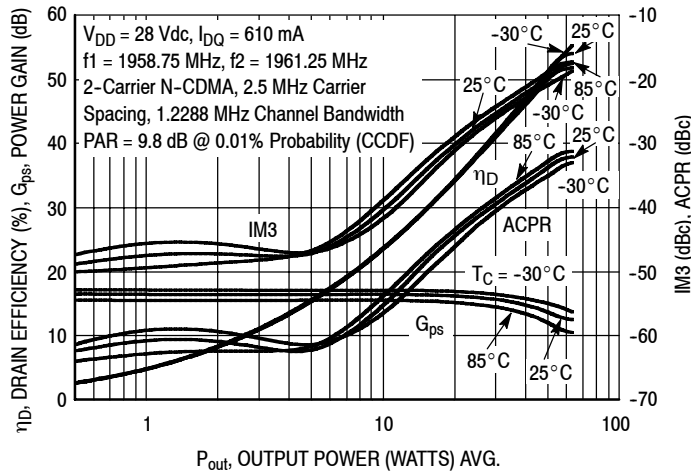
### TYPICAL CHARACTERISTICS



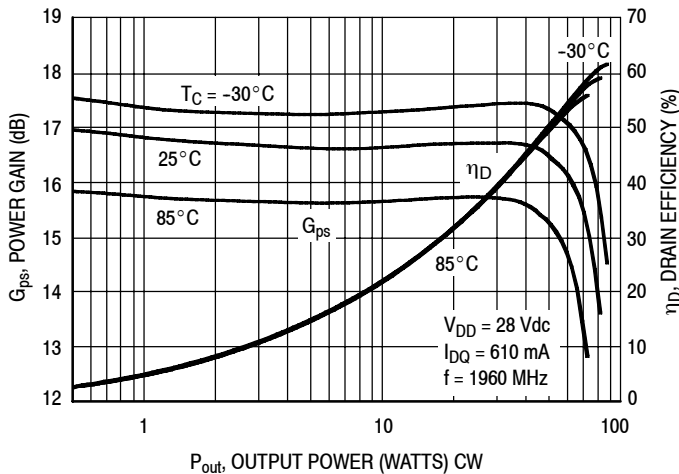
**Figure 7. Intermodulation Distortion Products versus Tone Spacing**



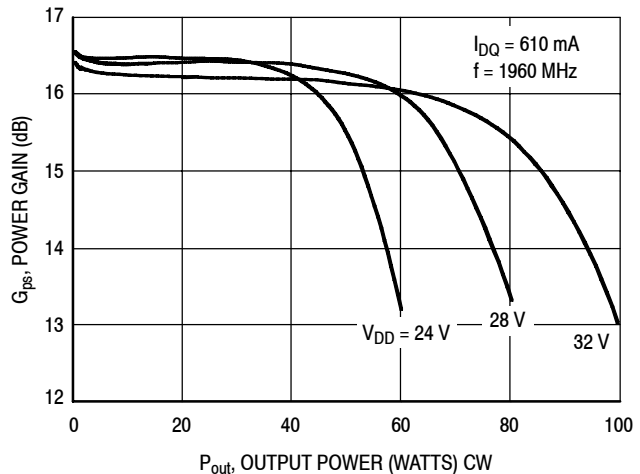
**Figure 8. Pulsed CW Output Power versus Input Power**



**Figure 9. 2-Carrier N-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power**



**Figure 10. Power Gain and Drain Efficiency versus CW Output Power**

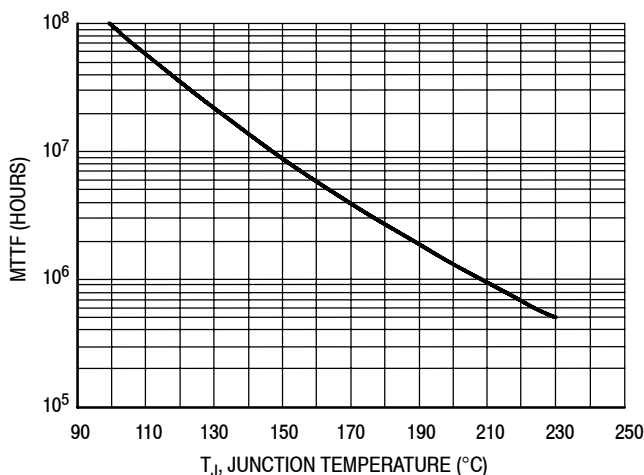


**Figure 11. Power Gain versus Output Power**

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## TYPICAL CHARACTERISTICS



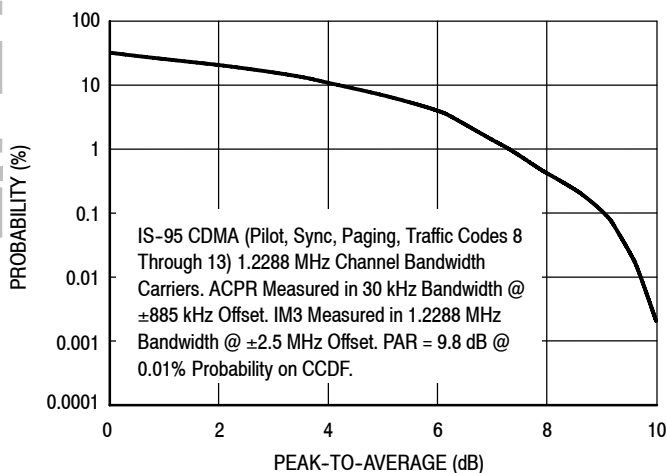
This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 28$  Vdc,  $P_{out} = 12$  W Avg., and  $\eta_D = 26\%$ .

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

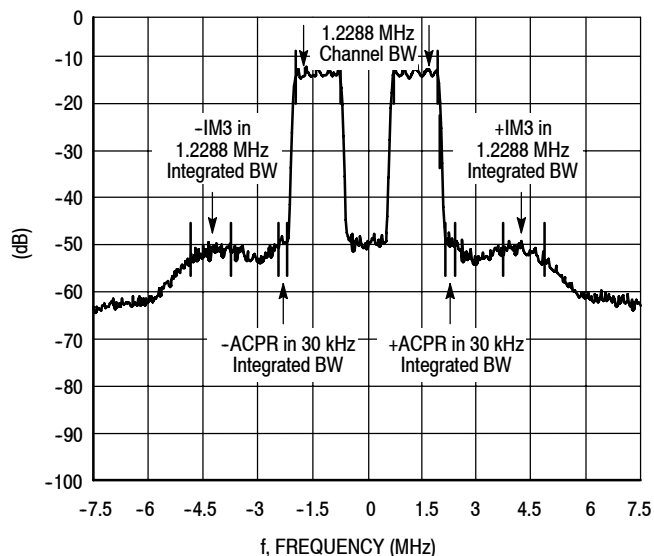
**Figure 12. MTTF versus Junction Temperature**

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## N-CDMA TEST SIGNAL

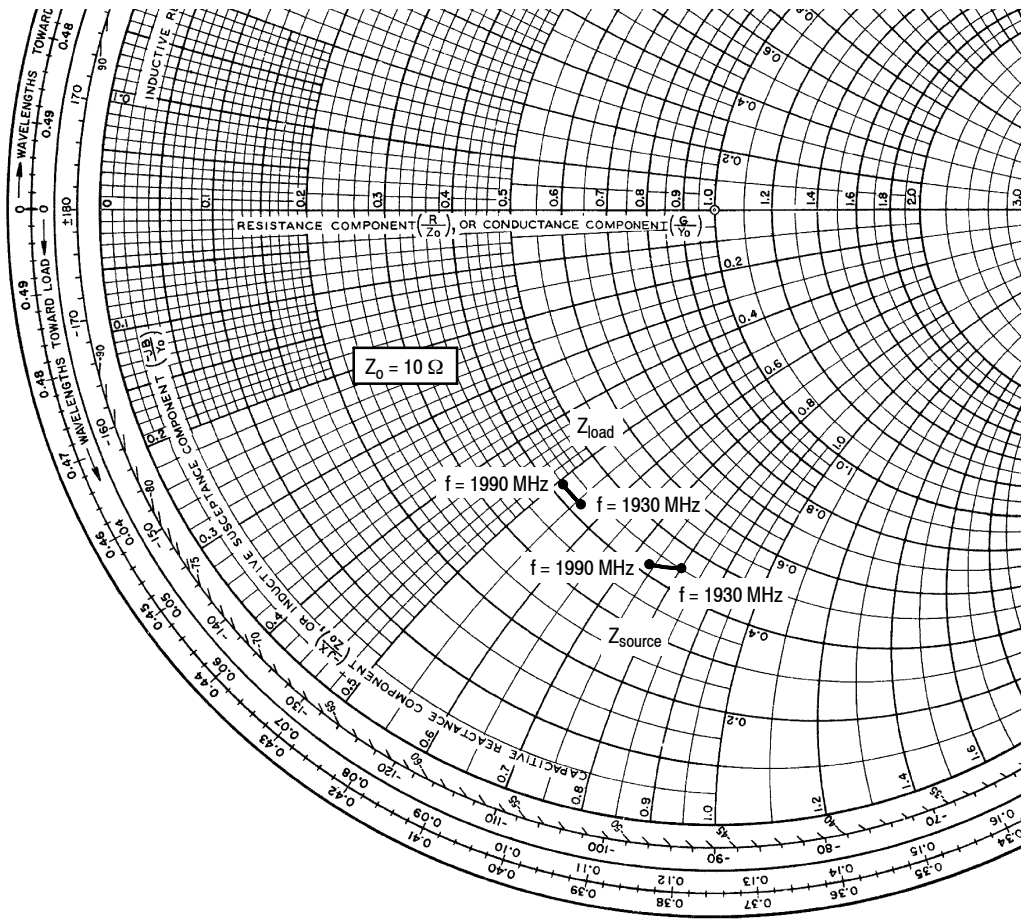


**Figure 13. 2-Carrier CCDF N-CDMA**



**Figure 14. 2-Carrier N-CDMA Spectrum**

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$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 610 \text{ mA}$ ,  $P_{out} = 12 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
1930	$4.54 - j7.95$	$4.15 - j5.58$
1960	$4.33 - j7.74$	$4.17 - j5.34$
1990	$4.20 - j7.43$	$4.22 - j5.10$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

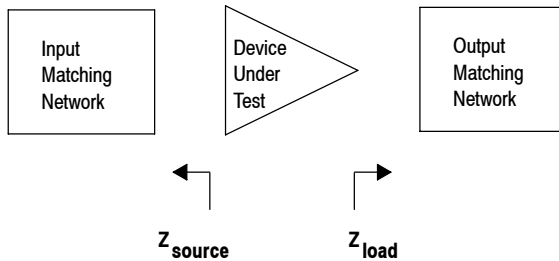
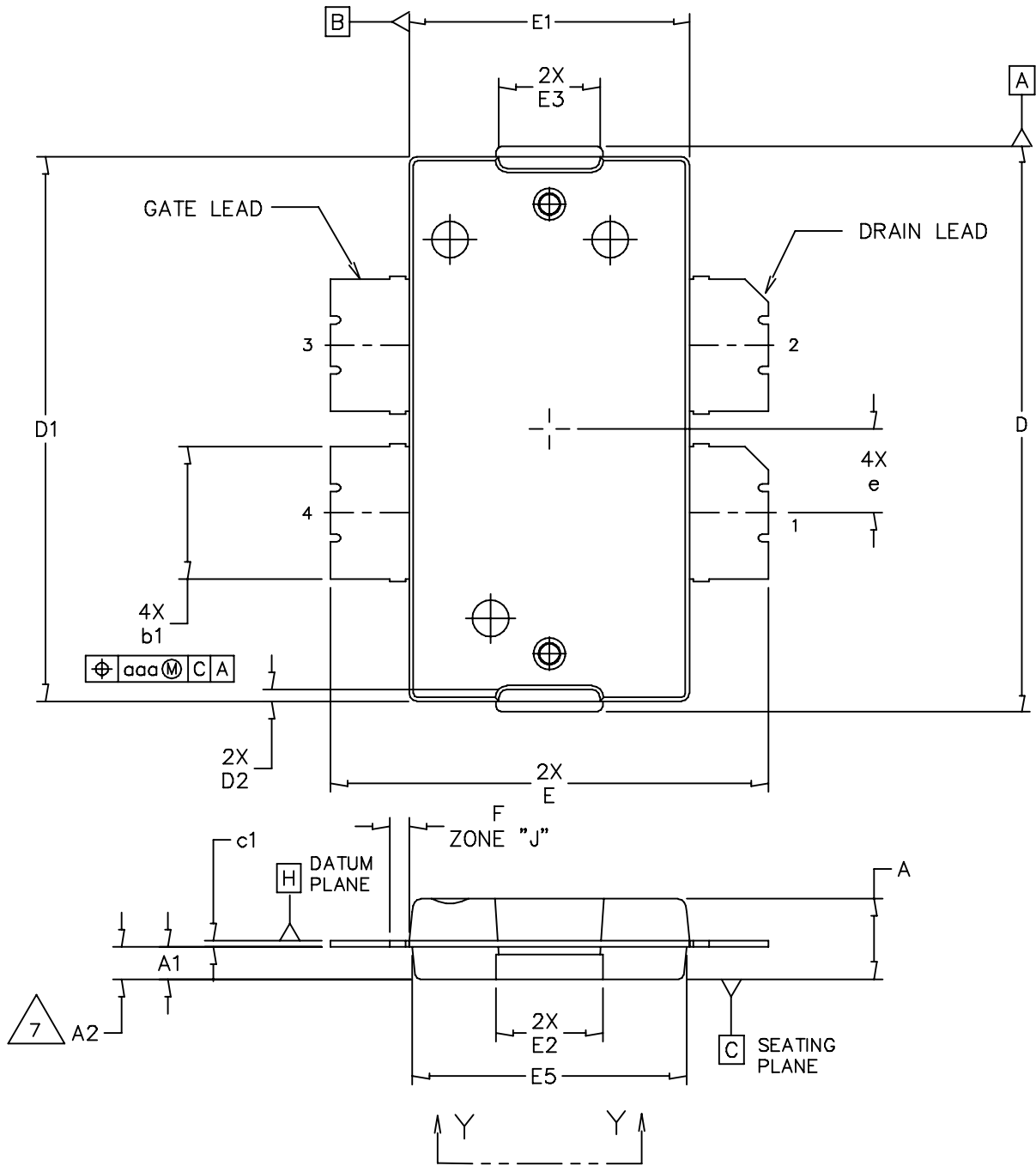


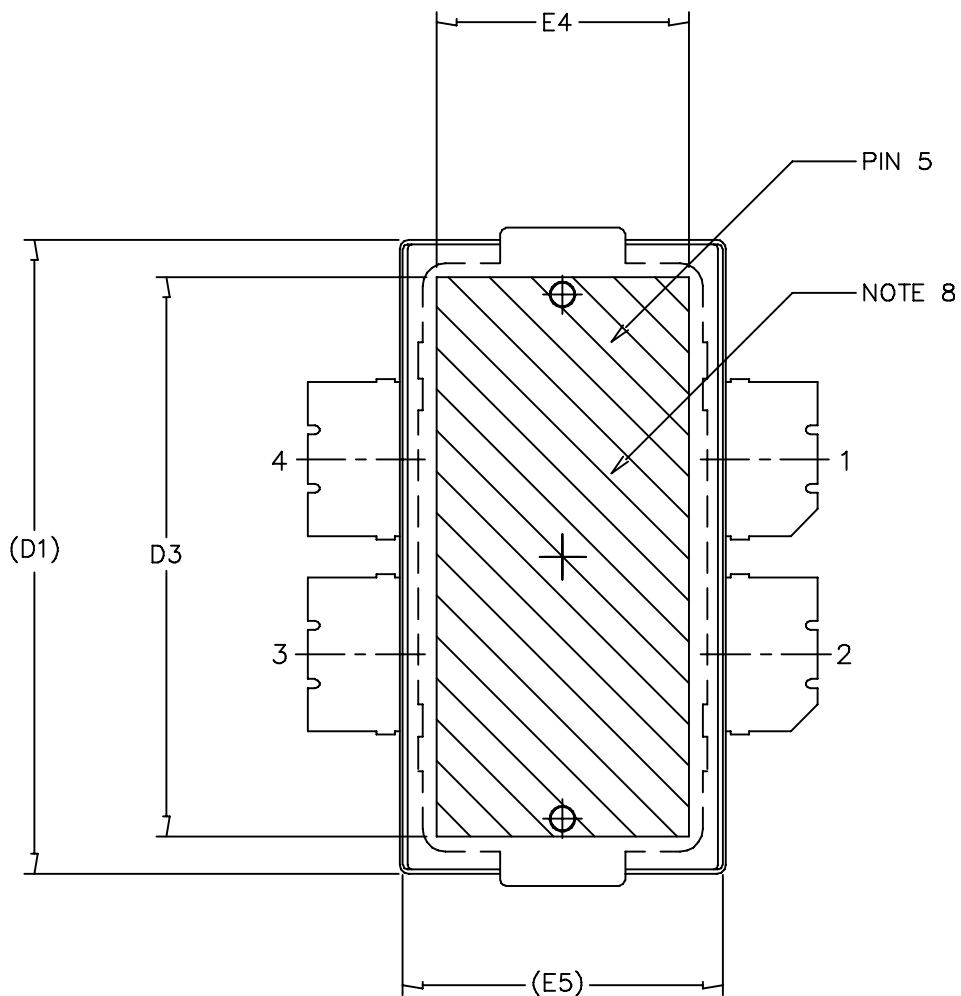
Figure 15. Series Equivalent Source and Load Impedance

**PACKAGE DIMENSIONS**



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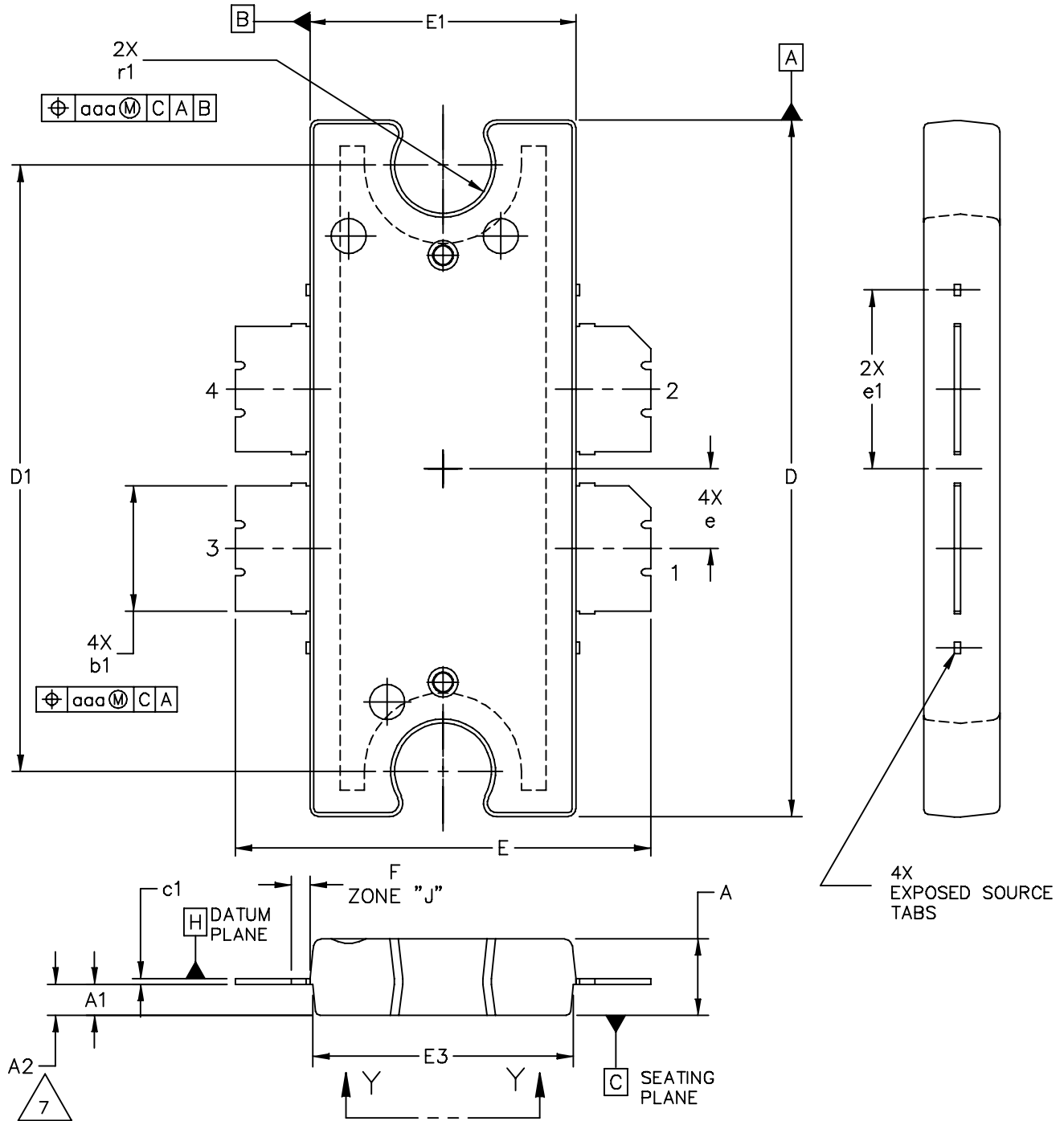
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

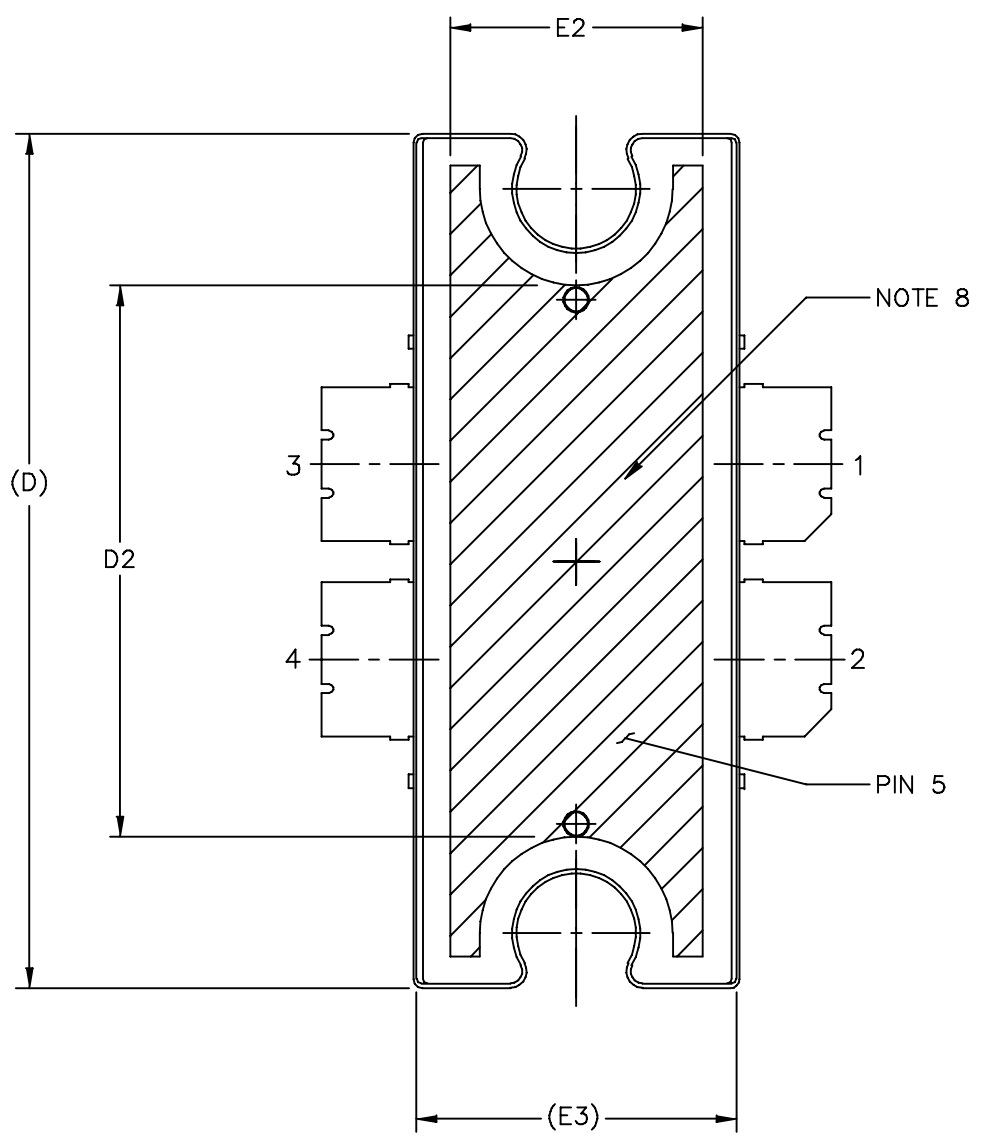
STYLE 1:

PIN 1 - DRAIN      PIN 2 - DRAIN  
 PIN 3 - GATE      PIN 4 - GATE  
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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	CASE NUMBER: 1484-04	31 AUG 2007	
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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:  
 PIN 1 - DRAIN      PIN 2 - DRAIN  
 PIN 3 - GATE      PIN 4 - GATE  
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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	CASE NUMBER: 1484-04		31 AUG 2007
	STANDARD: NON-JEDEC		

Refer to the following documents to aid your design process.

**Application Notes**

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

**Engineering Bulletins**

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

**REVISION HISTORY**

The following table summarizes revisions to this document.

Revision	Date	Description
4	Dec. 2008	<ul style="list-style-type: none"> <li>• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13232, p. 1, 2</li> <li>• Changed Storage Temperature Range in Max Ratings table from -65 to +175 to -65 to +150 for standardization across products, p. 1</li> <li>• Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 1</li> <li>• Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table, related “Continuous use at maximum temperature will affect MTTF” footnote added and changed 220°C to 225°C in Capable Plastic Package bullet, p. 1</li> <li>• Corrected <math>V_{DS}</math> to <math>V_{DD}</math> in the RF test condition voltage callout for <math>V_{GS(Q)}</math>, and added “Measured in Functional Test”, On Characteristics table, p. 2</li> <li>• Updated PCB information to show more specific material details, Fig. 1, Test Circuit Schematic, p. 3</li> <li>• Updated Part Numbers in Table 6, Component Designations and Values, to latest RoHS compliant part numbers, p. 3</li> <li>• Removed lower voltage tests from Fig. 11, Power Gain versus Output Power, due to fixed tuned fixture limitations, p. 6</li> <li>• Replaced Fig. 12, MTTF versus Junction Temperature with updated graph. Removed Amps<sup>2</sup> and listed operating characteristics and location of MTTF calculator for device, p. 7</li> <li>• Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p. 9-11. Added pin numbers 1 through 4 on Sheet 1.</li> <li>• Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 12-14. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations.</li> <li>• Added Product Documentation and Revision History, p. 15</li> </ul>
5	Dec. 2010	<ul style="list-style-type: none"> <li>• Corrected data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13232, and Product Discontinuance Notification number, PCN14260, adding applicable overlay, p. 1, 2</li> </ul>

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