65Msps, 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +3.6V
OV_{DD} to GND........-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
INP, INN to GND ...-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
REFIN, REFOUT, REFP, REFN,
COM to GND.....-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
CLKP, CLKN, CLKTYP, G/$\overline{T}$, DCE,
PD to GND ....-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
D11–D0, I. C., DAV, DOR to GND ....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN 6mm x 6mm x 0.8mm
(derated 26.3mW/°C above +70°C)........................2105.3mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, C_L ≈ 5pF at digital outputs, V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL	f_{IN} = 20MHz (Note 2)		±0.4	±0.7	LSB
Differential Nonlinearity	DNL	f_{IN} = 20MHz, no missing codes over temperature (Note 2)		±0.3	±0.7	LSB
Offset Error		V_{REFIN} = 2.048V		±0.2	±0.9	%FS
Gain Error		V_{REFIN} = 2.048V		±0.3	±4.9	%FS
ANALOG INPUT (INP, INN)						
Differential Input Voltage Range	V_{DIFF}	Differential or single-ended inputs		±1.024		V
Common-Mode Input Voltage				V_{DD} / 2		V
Input Resistance	R_{IN}	Switched capacitor load		15		kΩ
Input Capacitance	C_{IN}			4		pF
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		65			MHz
Minimum Clock Frequency					5	MHz
Data Latency		Figure 5		8.5		Clock cycles
DYNAMIC CHARACTERISTICS (Differential inputs, 4096-point FFT)						
Signal-to-Noise Ratio	SNR	f_{IN} = 3MHz at -0.5dBFS		68.5		dB
		f_{IN} = 32.5MHz at -0.5dBFS (Note 2)	67.1	68.5		
Signal-to-Noise and Distortion	SINAD	f_{IN} = 3MHz at -0.5dBFS		68.4		dB
		f_{IN} = 32.5MHz at -0.5dBFS (Note 2)	67.0	68.4		
Single-Tone Spurious-Free Dynamic Range	SFDR	f_{IN} = 3MHz at -0.5dBFS		90.4		dBc
		f_{IN} = 32.5MHz at -0.5dBFS (Note 2)	82.2	88.7		
Total Harmonic Distortion	THD	f_{IN} = 3MHz at -0.5dBFS		-89.3		dBc
		f_{IN} = 32.5MHz at -0.5dBFS (Note 2)		-86.4	-80.7	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, C_L ≈ 5pF at digital outputs, V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic	HD2	f_{IN} = 3MHz at -0.5dBFS		-93.6		dBc
		f_{IN} = 32.5MHz at -0.5dBFS (Note 3)		-89.4	-82.0	
Third Harmonic	HD3	f_{IN} = 3MHz at -0.5dBFS		-96.8		dBc
		f_{IN} = 32.5MHz at -0.5dBFS (Note 3)		-92.7	-84.3	
Third-Order Intermodulation	IM3	f_{IN1} = 69MHz at -7dBFS, f_{IN2} = 71MHz at -7dBFS		-90		dBc
Two-Tone Spurious-Free Dynamic Range	$SFDR_{TT}$	f_{IN1} = 69MHz at -7dBFS, f_{IN2} = 71MHz at -7dBFS		89		dBc
Aperture Delay	t_{AD}	Figure 14		0.9		ns
Aperture Jitter	t_{AJ}	Figure 14		<0.2		ps_{RMS}
Output Noise	n_{OUT}	INP = INN = COM		0.5		LSB_{RMS}
Overdrive Recovery Time		±10% beyond full scale		1		Clock cycles
INTERNAL REFERENCE (REFIN = REFOUT; V_{REFP}, V_{REFN}, and V_{COM} are generated internally)						
REFOUT Output Voltage	V_{REFOUT}		1.988	2.048	2.080	V
COM Output Voltage	V_{COM}	V_{DD} / 2		1.65		V
Differential Reference Output Voltage	V_{REF}	V_{REF} = V_{REFP} - V_{REFN}		1.024		V
REFOUT Load Regulation				35		mV/mA
REFOUT Temperature Coefficient	TC_{REF}			+100		ppm/°C
REFOUT Short-Circuit Current		Short to V_{DD}		0.24		mA
		Short to GND		2.1		
BUFFERED EXTERNAL REFERENCE (REFIN driven externally, V_{REFIN} = 2.048V, V_{REFP}, V_{REFN}, and V_{COM} are generated internally)						
REFIN Input Voltage	V_{REFIN}			2.048		V
REFP Output Voltage	V_{REFP}	(V_{DD} / 2) + (V_{REFIN} / 4)		2.162		V
REFN Output Voltage	V_{REFN}	(V_{DD} / 2) - (V_{REFIN} / 4)		1.138		V
COM Output Voltage	V_{COM}	V_{DD} / 2	1.60	1.65	1.70	V
Differential Reference Output Voltage	V_{REF}	V_{REF} = V_{REFP} - V_{REFN}	0.970	1.024	1.070	V
Differential Reference Temperature Coefficient				+12.5		ppm/°C
Maximum REFP Current	I_{REFP}	Source		0.4		mA
		Sink		1.4		
Maximum REFN Current	I_{REFN}	Source		1.0		mA
		Sink		1.0		
Maximum COM Current	I_{COM}	Source		1.0		mA
		Sink		0.4		
REFIN Input Resistance				>50		MΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, C_L ≈ 5pF at digital outputs, V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UNBUFFERED EXTERNAL REFERENCE (REFIN = GND, V_{REFP}, V_{REFN}, and V_{COM} are applied externally)						
COM Input Voltage	V_{COM}	V_{DD} / 2		1.65		V
REFP Input Voltage		V_{REFP} - V_{COM}		0.512		V
REFN Input Voltage		V_{REFN} - V_{COM}		-0.512		V
Differential Reference Input Voltage	V_{REF}	V_{REF} = V_{REFP} - V_{REFN}		1.024		V
REFP Sink Current	I_{REFP}	V_{REFP} = 2.162V		1.1		mA
REFN Source Current	I_{REFN}	V_{REFN} = 1.138V		1.1		mA
COM Sink Current	I_{COM}			0.3		mA
REFP, REFN, Capacitance				13		pF
COM Capacitance				6		pF
CLOCK INPUTS (CLKP, CLKN)						
Single-Ended Input High Threshold	V_{IH}	CLKTYP = GND, CLKN = GND	0.8 x V_{DD}			V
Single-Ended Input Low Threshold	V_{IL}	CLKTYP = GND, CLKN = GND			0.2 x V_{DD}	V
Differential Input Voltage Swing		CLKTYP = high		1.4		V_{P-P}
Differential Input Common-Mode Voltage		CLKTYP = high		V_{DD} / 2		V
Minimum Clock Duty Cycle		DCE = OV_{DD}		20		%
		DCE = GND		45		
Maximum Clock Duty Cycle		DCE = OV_{DD}		80		%
		DCE = GND		65		
Input Resistance	R_{CLK}	Figure 4		5		kΩ
Input Capacitance	C_{CLK}			2		pF
DIGITAL INPUTS (CLKTYP, G/$\overline{T}$, PD)						
Input High Threshold	V_{IH}		0.8 x OV_{DD}			V
Input Low Threshold	V_{IL}				0.2 x OV_{DD}	V
Input Leakage Current		V_{IH} = OV_{DD}			±5	µA
		V_{IL} = 0			±5	
Input Capacitance	C_{DIN}			5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, C_L ≈ 5pF at digital outputs, V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (D0–D11, DAV, DOR)						
Output-Voltage Low	V_{OL}	D0–D11, DOR, I_{SINK} = 200µA			0.2	V
		DAV, I_{SINK} = 600µA			0.2	
Output-Voltage High	V_{OH}	D0–D11, DOR, I_{SOURCE} = 200µA	OV_{DD} - 0.2			V
		DAV, I_{SOURCE} = 600µA	OV_{DD} - 0.2			
Tri-State Leakage Current	I_{LEAK}	(Note 4)			±5	µA
D11–D0, DOR Tri-State Output Capacitance	C_{OUT}	(Note 4)		3		pF
DAV Tri-State Output Capacitance	C_{DAV}	(Note 4)		6		pF
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Digital Output Supply Voltage	OV_{DD}		1.7	2.0	V_{DD} + 0.3V	V
Analog Supply Current	I_{VDD}	Normal operating mode, f_{IN} = 32.4MHz at -0.5dBFS, CLKTYP = GND, single-ended clock		95.8		mA
		Normal operating mode, f_{IN} = 32.4MHz at -0.5dBFS, CLKTYP = OV_{DD}, differential clock		103.8	119	
		Power-down mode, clock idle, PD = OV_{DD}		0.045		
Analog Power Dissipation	P_{DISS}	Normal operating mode, f_{IN} = 32.4MHz at -0.5dBFS, CLKTYP = GND, single-ended clock		316		mW
		Normal operating mode, f_{IN} = 32.4MHz at -0.5dBFS, CLKTYP = OV_{DD}, differential clock		342	393	
		Power-down mode, clock idle, PD = OV_{DD}		0.15		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, C_L ≈ 5pF at digital outputs, V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

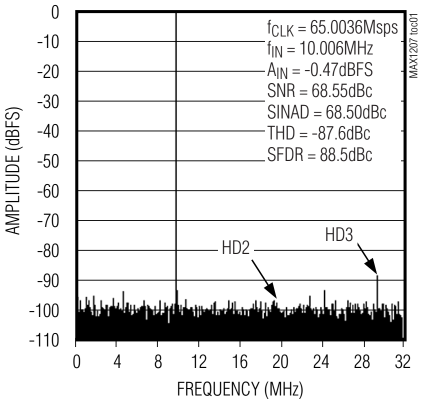
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Output Supply Current	I_{OVDD}	Normal operating mode, f_{IN} = 32.4MHz at -0.5dBFS, OV_{DD} = 2.0V, C_L ≈ 5pF		10.9		mA
		Power-down mode, clock idle, PD = OV_{DD}		6		µA
TIMING CHARACTERISTICS (Figure 5)						
Clock Pulse-Width High	t_{CH}			7.7		ns
Clock Pulse-Width Low	t_{CL}			7.7		ns
Data Valid Delay	t_{DAV}	C_L = 5pF (Note 5)		6.4		ns
Data Setup Time Before Rising Edge of DAV	t_{SETUP}	C_L = 5pF (Notes 3, 5)	8.5			ns
Data Hold Time After Rising Edge of DAV	t_{HOLD}	C_L = 5pF (Notes 3, 5)	6.3			ns
Wake-Up Time from Power-Down	t_{WAKE}	V_{REFIN} = 2.048V		10		ms

Note 1: Specifications ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization.
Note 2: Specifications guaranteed by design and characterization. Devices tested for performance during production test.
Note 3: Guaranteed by design and characterization.
Note 4: During power-down, D11–D0, DOR, and DAV are high impedance.
Note 5: Digital outputs settle to V_{IH} or V_{IL}.

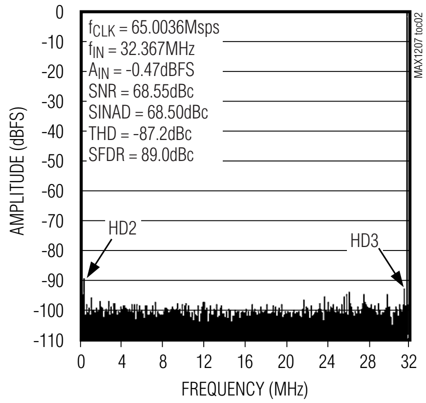
Typical Operating Characteristics

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, C_L ≈ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)

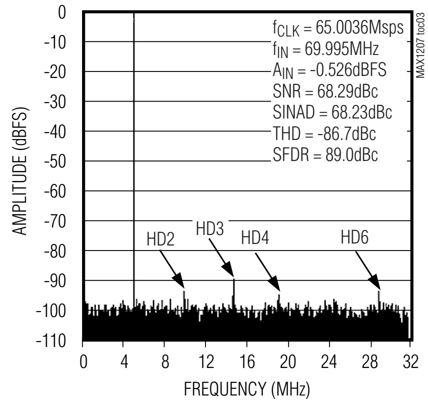
SINGLE-TONE FFT PLOT (8192-POINT DATA RECORD)



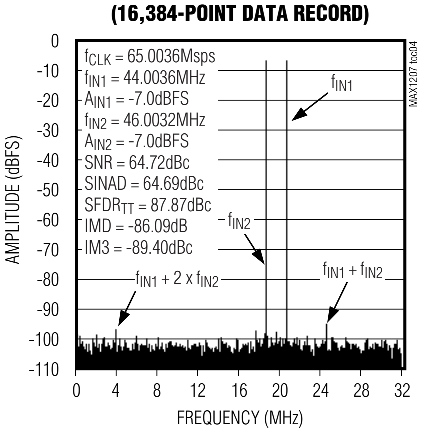
SINGLE-TONE FFT PLOT (8192-POINT DATA RECORD)



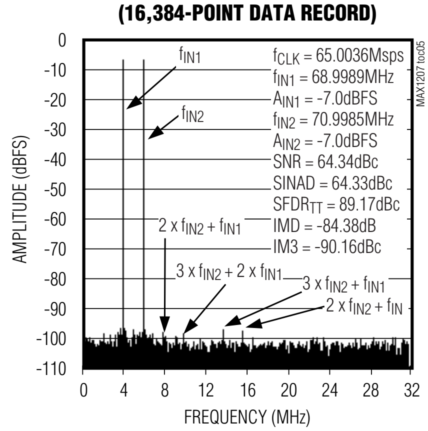
SINGLE-TONE FFT PLOT (8192-POINT DATA RECORD)



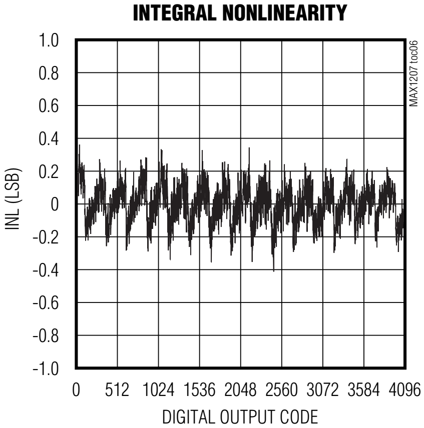
TWO-TONE FFT PLOT (16,384-POINT DATA RECORD)



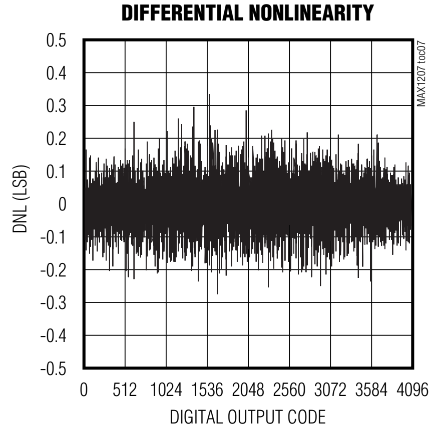
TWO-TONE FFT PLOT (16,384-POINT DATA RECORD)



INTEGRAL NONLINEARITY

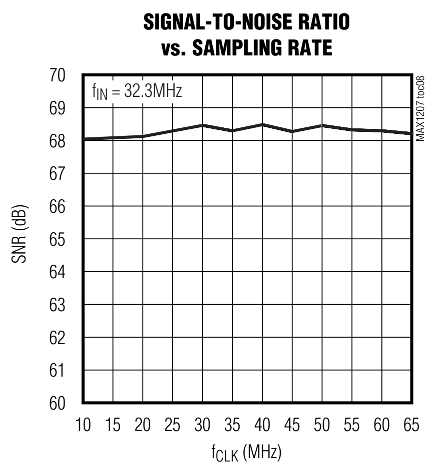


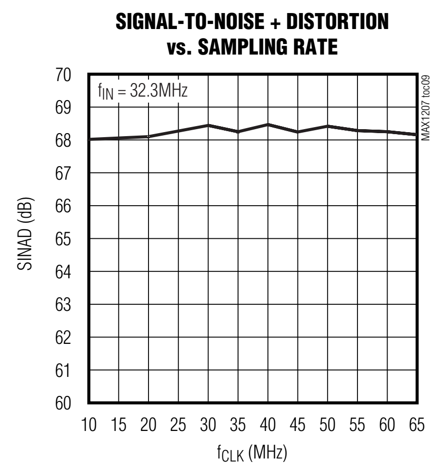
DIFFERENTIAL NONLINEARITY

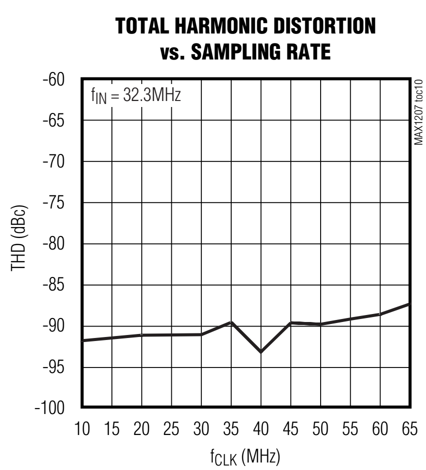


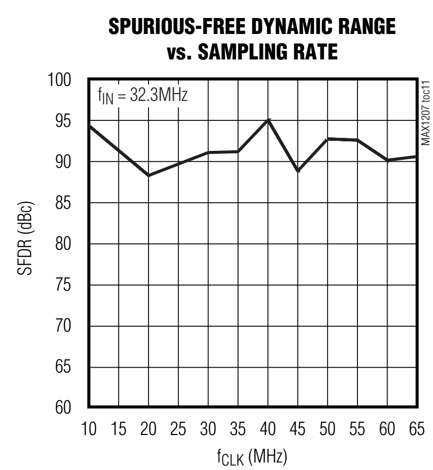
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)





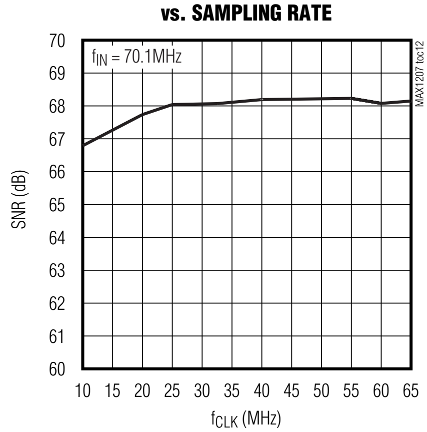




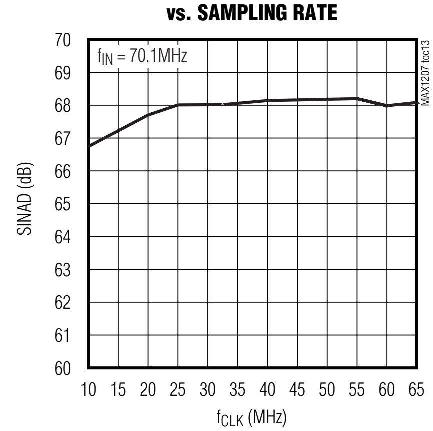
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)

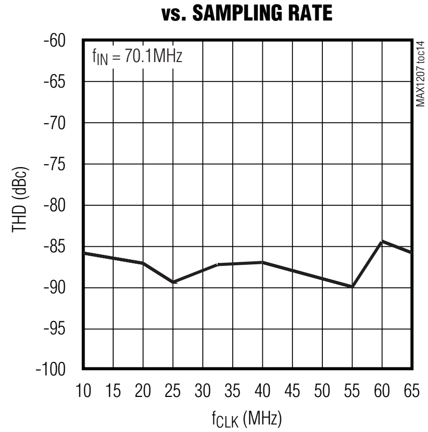
SIGNAL-TO-NOISE RATIO vs. SAMPLING RATE



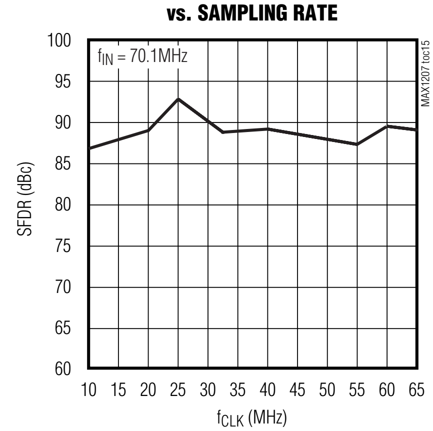
SIGNAL-TO-NOISE + DISTORTION vs. SAMPLING RATE



TOTAL HARMONIC DISTORTION vs. SAMPLING RATE

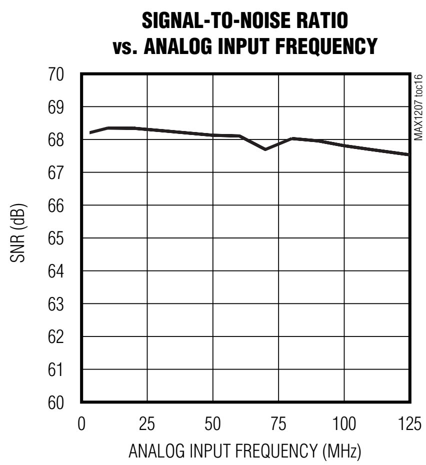


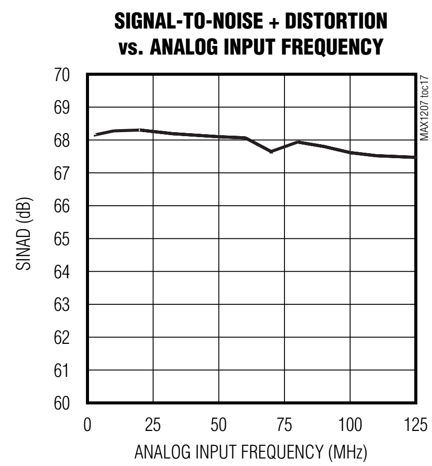
SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE

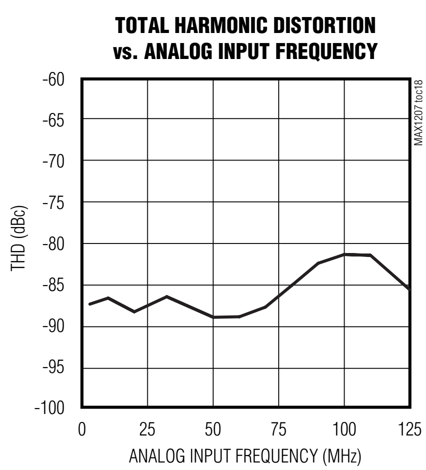


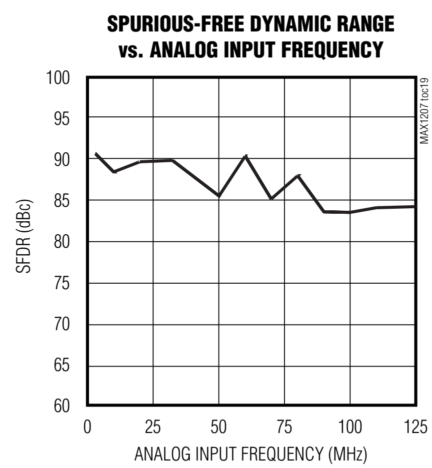
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)





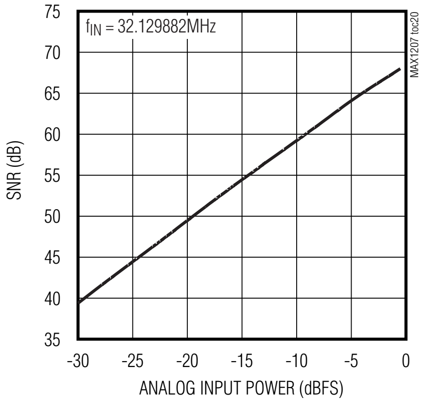




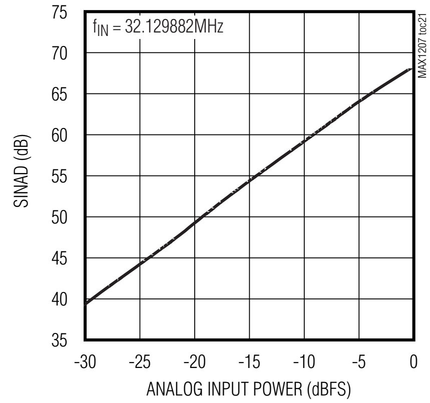
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)

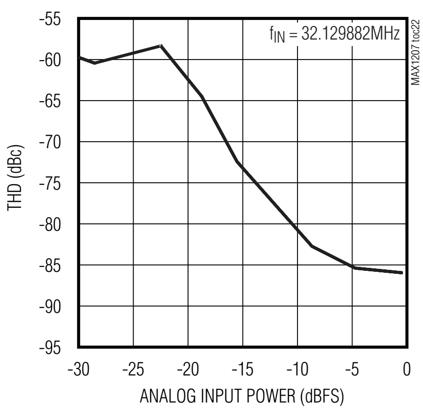
SIGNAL-TO-NOSIE RATIO vs. ANALOG INPUT POWER



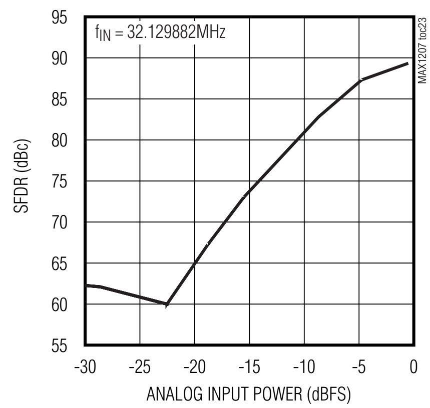
SIGNAL-TO-NOSIE + DISTORTION vs. ANALOG INPUT POWER



TOTAL HARMONIC DISTORTION vs. ANALOG INPUT POWER



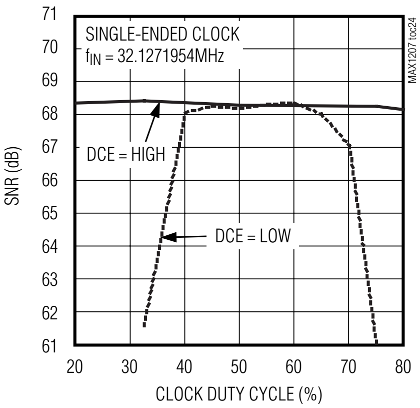
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT POWER



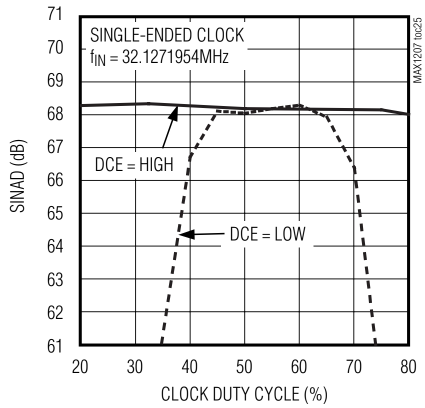
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)

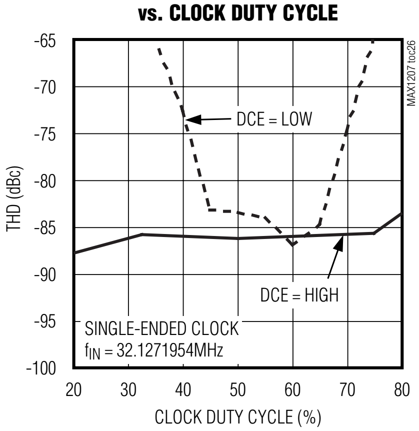
SIGNAL-TO-NOISE RATIO vs. CLOCK DUTY CYCLE



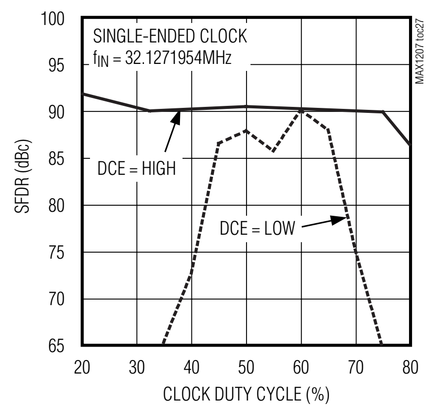
SIGNAL-TO-NOISE + DISTORTION vs. CLOCK DUTY CYCLE



TOTAL HARMONIC DISTORTION vs. CLOCK DUTY CYCLE



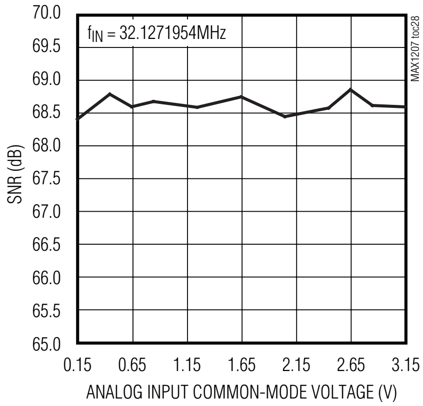
SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK DUTY CYCLE



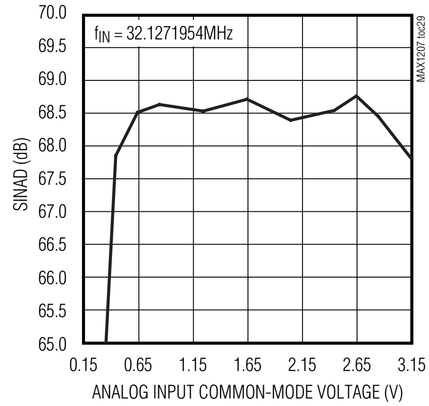
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)

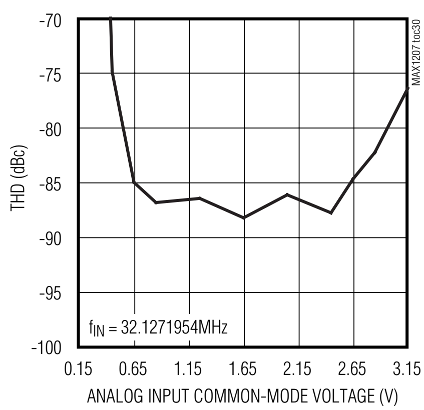
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT COMMON-MODE VOLTAGE



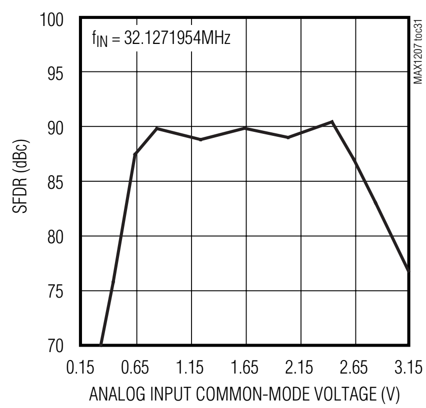
SIGNAL-TO-NOISE RATIO + DISTORTION vs. ANALOG INPUT COMMON-MODE VOLTAGE



TOTAL HARMONIC DISTORTION vs. ANALOG INPUT COMMON-MODE VOLTAGE



SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT COMMON-MODE VOLTAGE

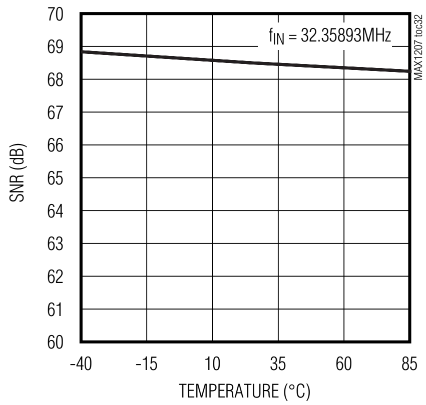


65Msps, 12-Bit ADC

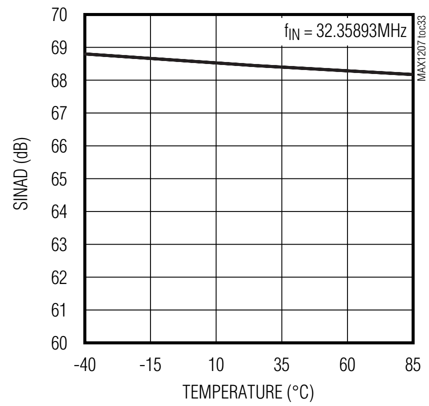
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF in parallel with 10µF to GND, 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)

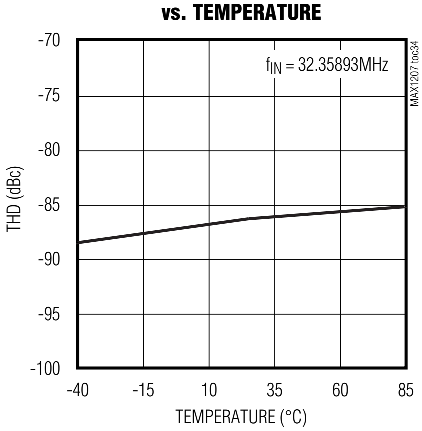
SIGNAL-TO-NOISE RATIO vs. TEMPERATURE



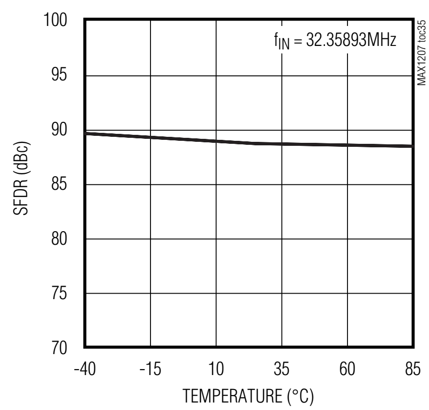
SIGNAL-TO-NOISE + DISTORTION vs. TEMPERATURE



TOTAL HARMONIC DISTORTION vs. TEMPERATURE



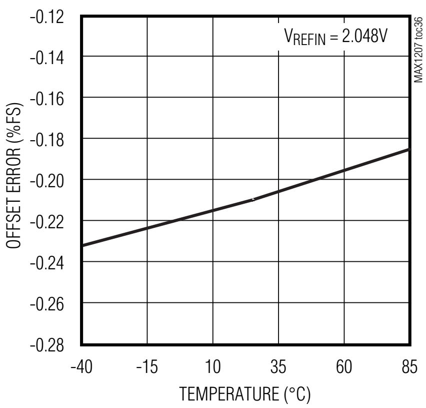
SPURIOUS-FREE DYNAMIC RANGE vs. TEMPERATURE



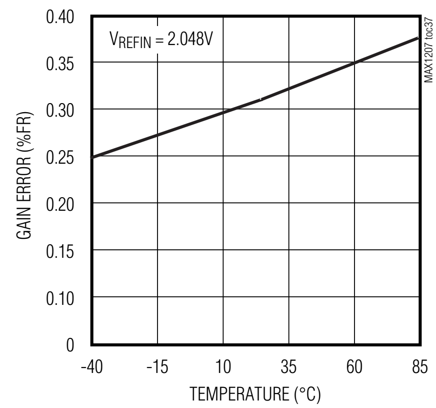
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 2.0V, GND = 0, REFIN = REFOUT (internal reference), C_{REFOUT} = 0.1µF, $C_L \approx$ 5pF at digital outputs, V_{IN} = -0.5dBFS differential input, DCE = high, CLKTYP = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 65MHz (50% duty cycle), C_{REFP} = C_{REFN} = 0.1µF to GND, 1µF in parallel with 10µF between REFP and REFN, C_{COM} = 0.1µF in parallel with 2.2µF to GND, T_A = +25°C, unless otherwise noted.)

OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	REFP	Positive Reference I/O. Conversion range is ±(V_{REFP} - V_{REFN}). Bypass REFP to GND with a 0.1µF capacitor. Connect a 1µF capacitor in parallel with a 10µF capacitor between REFP and REFN.
2	REFN	Negative Reference I/O. Conversion range is ±(V_{REFP} - V_{REFN}). Bypass REFN to GND with a 0.1µF capacitor. Connect a 1µF capacitor in parallel with a 10µF capacitor between REFP and REFN.
3	COM	Common-Mode Voltage I/O. Bypass COM to GND with a ≥2.2µF capacitor in parallel with a 0.1µF capacitor.
4, 7, 16, 35	GND	Ground. Connect all ground pins and the EP together.
5	INP	Positive Analog Input. For single-ended input operation, connect signal source to INP and connect INN to COM. For differential operation, connect the input signal between INP and INN.
6	INN	Negative Analog Input. For single-ended input operation, connect INN to COM. For differential operation, connect the input signal between INP and INN.
8	DCE	Duty-Cycle Equalizer Input. Connect DCE low (GND) to disable the internal duty-cycle equalizer. Connect DCE high (OV_{DD} or V_{DD}) to enable the internal duty-cycle equalizer.
9	CLKN	Negative Clock Input. In differential clock input mode (CLKTYP = OV_{DD} or V_{DD}), connect the clock signal between CLKP and CLKN. In single-ended clock mode (CLKTYP = GND), apply the clock signal to CLKP and connect CLKN to GND.
10	CLKP	Positive Clock Input. In differential clock input mode (CLKTYP = OV_{DD} or V_{DD}), connect the differential clock signal between CLKP and CLKN. In single-ended clock mode (CLKTYP = GND), apply the single-ended clock signal to CLKP and connect CLKN to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
11	CLKTYP	Clock Type Definition Input. Connect CLKTYP to GND to define the single-ended clock input. Connect CLKTYP to OV_{DD} or V_{DD} to define the differential clock input.
12–15, 36	V_{DD}	Analog Power Input. Connect V_{DD} to a 3.0V to 3.6V power supply. Bypass V_{DD} to GND with a parallel capacitor combination of ≥2.2µF and 0.1µF. Connect all V_{DD} pins to the same potential.
17, 34	OV_{DD}	Output Driver Power Input. Connect OV_{DD} to a 1.7V to V_{DD} power supply. Bypass OV_{DD} to GND with a parallel capacitor combination of ≥2.2µF and 0.1µF.
18	DOR	Data Out-of-Range Indicator. The DOR digital output indicates when the analog input voltage is out of range. When DOR is high, the analog input is beyond its full-scale range. When DOR is low, the analog input is within its full-scale range.
19	D11	CMOS Digital Output, Bit 11 (MSB)
20	D10	CMOS Digital Output, Bit 10
21	D9	CMOS Digital Output, Bit 9
22	D8	CMOS Digital Output, Bit 8
23	D7	CMOS Digital Output, Bit 7
24	D6	CMOS Digital Output, Bit 6
25	D5	CMOS Digital Output, Bit 5
26	D4	CMOS Digital Output, Bit 4
27	D3	CMOS Digital Output, Bit 3
28	D2	CMOS Digital Output, Bit 2
29	D1	CMOS Digital Output, Bit 1
30	D0	CMOS Digital Output, Bit 0 (LSB)
31, 32	I. C.	Internally Connected. Leave I. C. unconnected.
33	DAV	Data Valid Output. The DAV is a single-ended version of the input clock that is compensated to correct for any input clock duty-cycle variations. The MAX1211 evaluation kit (MAX1211EVKIT) utilizes DAV to latch data (D0–D11) into external back-end digital circuitry.
37	PD	Power-Down Input. Force PD high for power-down mode. Force PD low for normal operation.
38	REFOUT	Internal Reference Voltage Output. For internal reference operation, connect REFOUT directly to REFIN or use a resistive-divider from REFOUT to set the voltage at REFIN. Bypass REFOUT to GND with a ≥0.1µF capacitor.
39	REFIN	Reference Input. $V_{REFIN} = 2 \times (V_{REFP} - V_{REFN})$. Bypass REFIN to GND with a ≥0.1µF capacitor.
40	$G/\overline{T}$	Output Format Select Input. Connect $G/\overline{T}$ to GND for the two's complement digital output format. Connect $G/\overline{T}$ to OV_{DD} or V_{DD} for the Gray code digital output format.
—	EP	Exposed Paddle. EP is internally connected to GND. Externally connect EP to GND to achieve specified performance.

Detailed Description

The MAX1207 uses a 10-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. From input to output, the total clock-cycle latency is 8.5 clock cycles.

Each pipeline converter stage converts its input voltage into a digital output code. At every stage, except the last, the error between the input voltage and the digital output code is multiplied and passed along to the next pipeline stage. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. Figure 2 shows the MAX1207 functional diagram.

Input Track-and-Hold (T/H) Circuit

Figure 3 displays a simplified functional diagram of the input T/H circuits. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the operational transconductance amplifier (OTA), and open simultaneously with S1, sampling the input waveform. Switches S4a, S4b, S5a, and S5b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers charge capacitors C1a and C1b to the same values originally held on C2a and C2b. These values are then presented to the first-stage quantizers and isolate the pipelines from the fast-changing inputs. The wide input-bandwidth T/H amplifier allows the MAX1207 to track and sample/hold analog inputs of high frequencies well beyond Nyquist. Analog input INP to INN can be driven either differentially or single ended. For differential inputs, balance the input impedance of INP and INN and set the common-mode voltage to midsupply (V_{DD} / 2) for optimum performance.

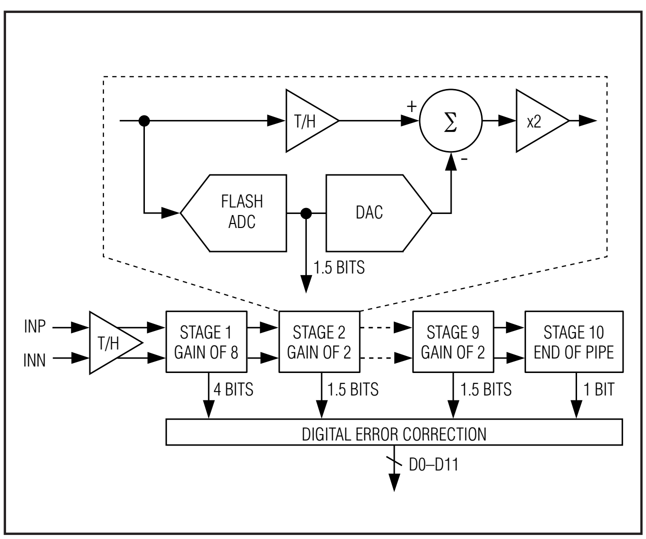


Figure 1. Pipeline Architecture—Stage Blocks

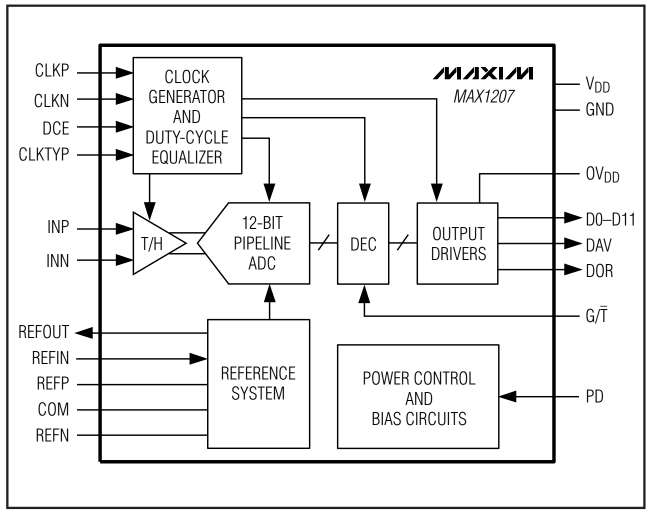


Figure 2. Functional Diagram

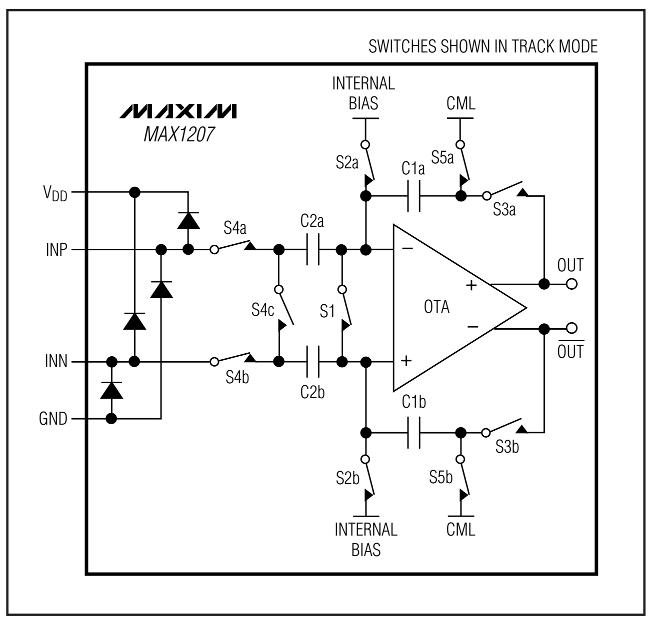


Figure 3. Internal T/H Circuit

Table 1. Reference Modes

V_{REFIN}	REFERENCE MODE
35% V_{REFOUT} to 100% V_{REFOUT}	**Internal reference mode**. REFIN is driven by REFOUT either through a direct short or a resistive divider. $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REFIN} / 4$, and $V_{REFN} = V_{DD} / 2 - V_{REFIN} / 4$.
0.7V to 2.3V	**Buffered external reference mode**. An external 0.7V to 2.3V reference voltage is applied to REFIN. $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REFIN} / 4$, and $V_{REFN} = V_{DD} / 2 - V_{REFIN} / 4$.
<0.5V	**Unbuffered external reference mode**. REFP, REFN, and COM are driven by external reference sources. V_{REF} is the difference between the externally applied V_{REFP} and V_{REFN}.

Reference Output (REFOUT)

An internal bandgap reference is the basis for all the internal voltages and bias currents used in the MAX1207. The power-down logic input (PD) enables and disables the reference circuit. REFOUT has approximately 17kΩ to GND when the MAX1207 is in power-down. The reference circuit requires 10ms to power up and settle when power is applied to the MAX1207 or when PD transitions from high to low.

The internal bandgap reference and buffer generate REFOUT to be 2.048V with a +100ppm/°C temperature coefficient. Connect an external ≥0.1µF bypass capacitor from REFOUT to GND for stability. REFOUT sources up to 1.4mA and sinks up to 100µA for external circuits with a load regulation of 35mV/mA. Short-circuit protection limits I_{REFOUT} to a 2.1mA source current when shorted to GND and a 240µA sink current when shorted to V_{DD}.

Analog Inputs and Reference Configurations

The MAX1207 full-scale analog input range is $\pm V_{REF}$ with a common-mode input range of $V_{DD} / 2 \pm 0.8V$. V_{REF} is the difference between V_{REFP} and V_{REFN}. The MAX1207 provides three modes of reference operation. The voltage at REFIN (V_{REFIN}) sets the reference operation mode (Table 1).

To operate the MAX1207 with the internal reference, connect REFOUT to REFIN either with a direct short or through a resistive-divider. In this mode, COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REFIN} / 4$, and $V_{REFN} = V_{DD} / 2 - V_{REFIN} / 4$. The REFIN input impedance is very large (>50MΩ). When driving REFIN through a resistive-divider, use resistances ≥10kΩ to avoid loading REFOUT.

Buffered external reference mode is virtually identical to internal reference mode except that the reference source is derived from an external reference and not the MAX1207 REFOUT. In buffered external reference mode, apply a stable 0.7V to 2.3V source at REFIN. COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REFIN} / 4$, and $V_{REFN} = V_{DD} / 2 - V_{REFIN} / 4$.

To operate the MAX1207 in unbuffered external reference mode, connect REFIN to GND. Connecting REFIN to GND deactivates the on-chip reference buffers for COM, REFP, and REFN. With their buffers deactivated, COM, REFP, and REFN inputs must be driven through separate, external reference sources. Drive V_{COM} to $V_{DD} / 2 \pm 5\%$, and drive REFP and REFN such that $V_{COM} = (V_{REFP} + V_{REFN}) / 2$. The analog input range is $\pm(V_{REFP} - V_{REFN})$.

All three modes of reference operation require the same bypass capacitor combination. Bypass COM with a 0.1µF capacitor in parallel with a ≥2.2µF capacitor to GND. Bypass REFP and REFN each with a 0.1µF capacitor to GND. Bypass REFP to REFN with a 1µF capacitor in parallel with a 10µF capacitor. Place the 1µF capacitor as close to the device as possible. Bypass REFIN and REFOUT to GND with a 0.1µF capacitor.

For detailed circuit suggestions, see Figures 12 and 13.

Clock Input and Clock Control Lines (CLKP, CLKN, CLKTYP, DCE)

The MAX1207 accepts both differential and single-ended clock inputs. For single-ended clock input operation, connect CLKTYP to GND, CLKN to GND, and drive CLKP with the external single-ended clock signal. For differential clock input operation, connect CLKTYP to OV_{DD} or V_{DD} and drive CLKP and CLKN with the external differential clock signal. To reduce clock jitter, the external single-ended clock must have sharp falling edges. Consider the clock input as an analog input and route it away from any other analog inputs and digital signal lines.

CLKP and CLKN are high impedance when the MAX1207 is powered down (Figure 4).

Low clock jitter is required for the specified SNR performance of the MAX1207. Analog input sampling occurs on the falling edge of the clock signal, requiring this edge to have the lowest possible jitter. Jitter limits the maximum SNR performance of any ADC according to the following relationship:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_J}\right)$$

where f_{IN} represents the analog input frequency and t_J is the total system clock jitter. Clock jitter is especially critical for undersampling applications. For example, assuming that clock jitter is the only noise source, to obtain the specified 68.5dB of SNR with an input frequency of 32.5MHz, the system must have less than 1.8ps of clock jitter.

Clock Duty-Cycle Equalizer (DCE)

The MAX1207 clock duty-cycle equalizer allows for a wide 20% to 80% clock duty cycle when enabled (DCE = OV_{DD} or V_{DD}). When disabled (DCE = GND), the MAX1207 accepts a narrow 45% to 65% clock duty cycle. See the *Typical Operating Characteristics* section for Dynamic Performance vs. Clock Duty-Cycle plots.

The clock duty-cycle equalizer uses a delay-locked loop to create internal timing signals that are duty-cycle independent. Due to this delay-locked loop, the MAX1207 requires approximately 100 clock cycles to acquire and lock to new clock frequencies.

Disabling the clock duty-cycle equalizer reduces the analog supply current by 1.5mA.

System Timing Requirements

Figure 5 shows the relationship between the clock, analog inputs, DAV indicator, DOR indicator, and the resulting output data. The analog input is sampled on the falling edge of the clock signal and the resulting data appears at the digital outputs 8.5 clock cycles later.

The DAV indicator is synchronized with the digital output and optimized for use in latching data into digital back-end circuitry. Alternatively, digital back-end circuitry can be latched with the falling edge of the clock.

Data Valid Output (DAV)

DAV is a single-ended version of the input clock (CLKP). The output data changes on the falling edge of DAV, and DAV rises once the output data is valid.

The state of the duty-cycle equalizer input (DCE) changes the waveform at DAV. With the duty-cycle equalizer disabled (DCE low), the DAV signal is the inverse of the signal at CLKP delayed by 6.4ns. With the duty-cycle equalizer enabled (DCE high), the DAV signal has a fixed pulse width that is independent of CLKP. In either case, with DCE high or low, output data at D0–D11 and DOR are valid from 8.5ns before the rising edge of DAV to 6.3ns after the rising edge of DAV, and the rising edge of DAV is synchronized to have a 6.4ns delay from the falling edge of CLKP.

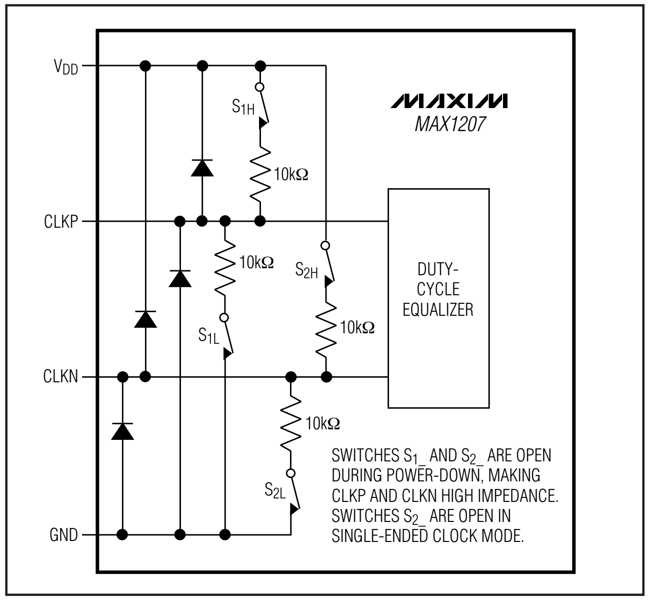


Figure 4. Simplified Clock Input Circuit

DAV is high impedance when the MAX1207 is in power-down (PD = high). DAV is capable of sinking and sourcing 600µA and has three times the drive strength of D0–D11 and DOR. DAV is typically used to latch the MAX1207 output data into an external back-end digital circuit.

Keep the capacitive load on DAV as low as possible (<25pF) to avoid large digital currents feeding back into the analog portion of the MAX1207 and degrading its dynamic performance. An external buffer on DAV isolates it from heavy capacitive loads. Refer to the MAX1211 evaluation kit schematic for an example of DAV driving back-end digital circuitry through an external buffer.

Data Out-of-Range Indicator (DOR)

The DOR digital output indicates when the analog input voltage is out of range. When DOR is high, the analog input is out of range. When DOR is low, the analog input is within range. The valid differential input range is from (V_{REFP} - V_{REFN}) to (V_{REFN} - V_{REFP}). Signals outside this valid differential range cause DOR to assert high as shown in Table 2.

DOR is synchronized with DAV and transitions along with output data D0–D11. There is an 8.5 clock-cycle latency in the DOR function just as with the output data (Figure 5).

Table 2. Output Codes vs. Input Voltage

GRAY CODE OUTPUT CODE ($G/\overline{T}$ = 1)				TWO'S COMPLEMENT OUTPUT CODE ($G/\overline{T}$ = 0)				$V_{INP} - V_{INN}$ (V_{REFP} = 2.162V, V_{REFN} = 1.138V)
BINARY D11 → D0	**DOR**	**HEXADECIMAL EQUIVALENT OF D11 → D0**	**DECIMAL EQUIVALENT OF D11 → D0 ($CODE_{10}$)**	**BINARY D11 → D0**	**DOR**	**HEXADECIMAL EQUIVALENT OF D11 → D0**	**DECIMAL EQUIVALENT OF D11 → D0 ($CODE_{10}$)**	
1000 0000 0000	**1**	0x800	+4095	0111 1111 1111	**1**	0x7FF	+2047	>+1.0235V (DATA OUT OF RANGE)
1000 0000 0000	0	0x800	+4095	0111 1111 1111	0	0x7FF	+2047	+1.0235V
1000 0000 0001	0	0x801	+4094	0111 1111 1110	0	0x7FE	+2046	+1.0230V
1100 0000 0011	0	0xC03	+2050	0000 0000 0010	0	0x002	+2	+0.0010V
1100 0000 0001	0	0xC01	+2049	0000 0000 0001	0	0x001	+1	+0.0005V
1100 0000 0000	0	0xC00	+2048	0000 0000 0000	0	0x000	0	+0.0000V
0100 0000 0000	0	0x400	+2047	1111 1111 1111	0	0xFFF	-1	-0.0005V
0100 0000 0001	0	0x401	+2046	1111 1111 1110	0	0xFFE	-2	-0.0010V
0000 0000 0001	0	0x001	+1	1000 0000 0001	0	0x801	-2047	-1.0235V
0000 0000 0000	0	0x000	0	1000 0000 0000	0	0x800	-2048	-1.0240V
0000 0000 0000	**1**	0x000	0	1000 0000 0000	**1**	0x800	-2048	<-1.0240V (DATA OUT OF RANGE)

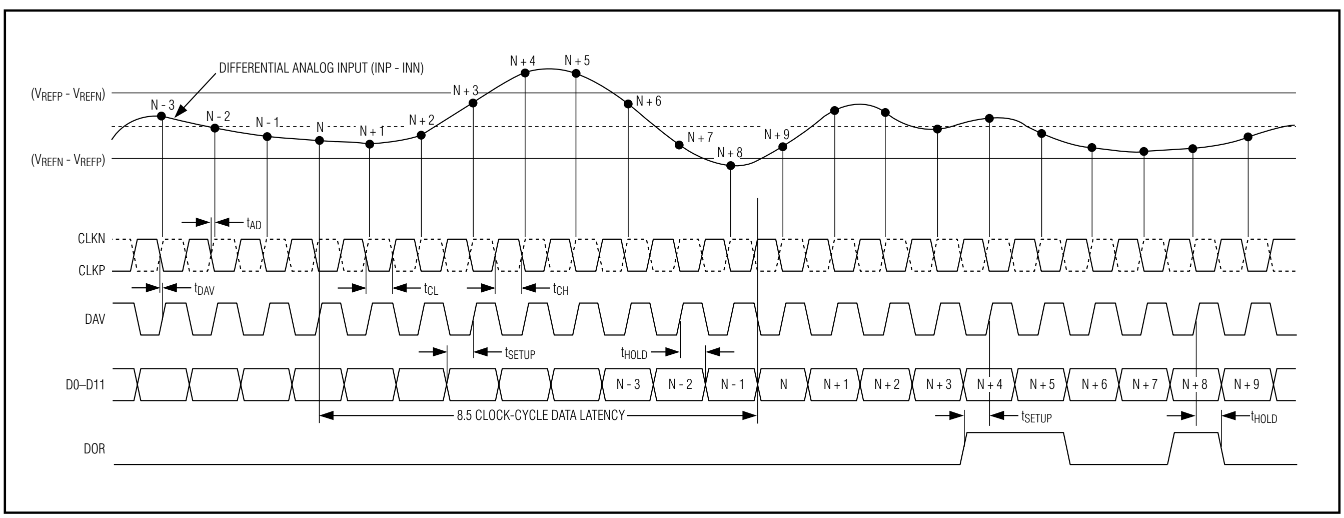


Figure 5. System Timing Diagram

DOR is high impedance when the MAX1207 is in power-down (PD = high). DOR enters a high-impedance state within 10ns of the rising edge of PD and becomes active within 10ns of PD's falling edge.

Digital Output Data (D0–D11), Output Format ($G/\overline{T}$)

The MAX1207 provides a 12-bit, parallel, tri-state output bus. D0–D11 and DOR update on the falling edge of DAV and are valid on the rising edge of DAV.

The MAX1207 output data format is either Gray code or two's complement, depending on the logic input $G/\overline{T}$. With $G/\overline{T}$ high, the output data format is Gray code. With $G/\overline{T}$ low, the output data format is two's complement. See Figure 8 for a binary-to-Gray and Gray-to-binary code-conversion example.

The following equations, Table 2, Figure 6, and Figure 8 define the relationship between the digital output and the analog input:

$$V_{INP} - V_{INN} = (V_{REFP} - V_{REFN}) \times 2 \times \frac{CODE_{10} - 2048}{4096}$$

for Gray code ($G/\overline{T}$ = 1).

$$V_{INP} - V_{INN} = (V_{REFP} - V_{REFN}) \times 2 \times \frac{CODE_{10}}{4096}$$

for two's complement ($G/\overline{T}$ = 0).

where $CODE_{10}$ is the decimal equivalent of the digital output code as shown in Table 2.

The digital outputs D0–D11 are high impedance when the MAX1207 is in power-down (PD = high). D0–D11 go high impedance within 10ns of the rising edge of PD and become active within 10ns of PD's falling edge.

Keep the capacitive load on the MAX1207 digital outputs D0–D11 as low as possible (<15pF) to avoid large digital currents feeding back into the analog portion of the MAX1207 and degrading its dynamic performance. The addition of external digital buffers on the digital outputs isolate the MAX1207 from heavy capacitive loads. To improve the dynamic performance of the MAX1207, add 220Ω resistors in series with the digital outputs close to the MAX1207. Refer to the MAX1211 evaluation kit schematic for an example of the digital outputs driving a digital buffer through 220Ω series resistors.

Power-Down Input (PD)

The MAX1207 has two power modes that are controlled with the power-down digital input (PD). With PD low, the MAX1207 is in its normal operating mode. With PD high, the MAX1207 is in power-down mode.

The power-down mode allows the MAX1207 to efficiently use power by transitioning to a low-power state when conversions are not required. Additionally, the MAX1207 parallel output bus goes high impedance in power-down mode, allowing other devices on the bus to be accessed.

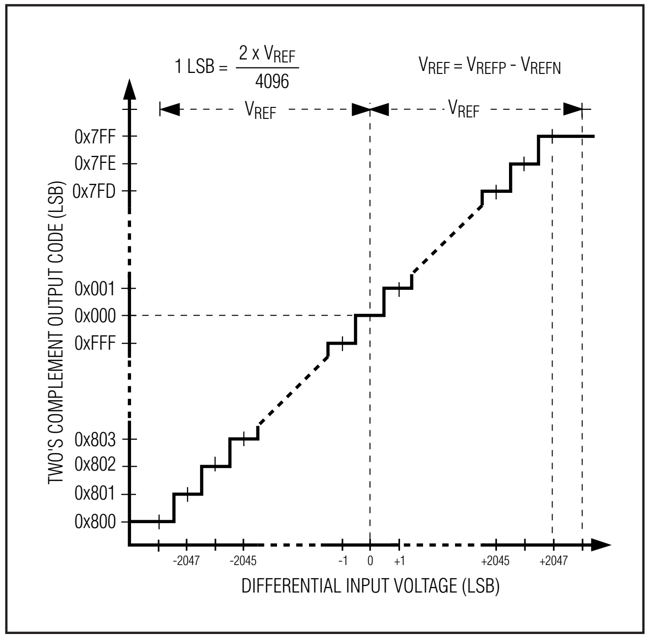


Figure 6. Two's Complement Transfer Function ($G/\overline{T}$ = 0)

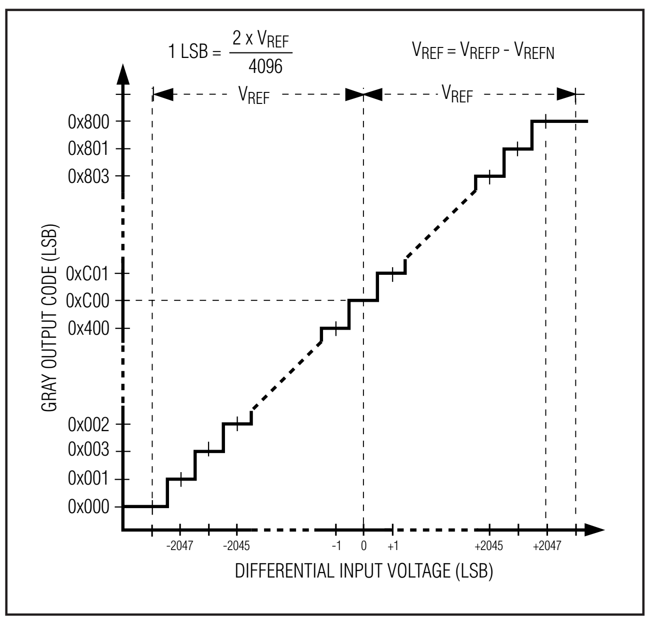
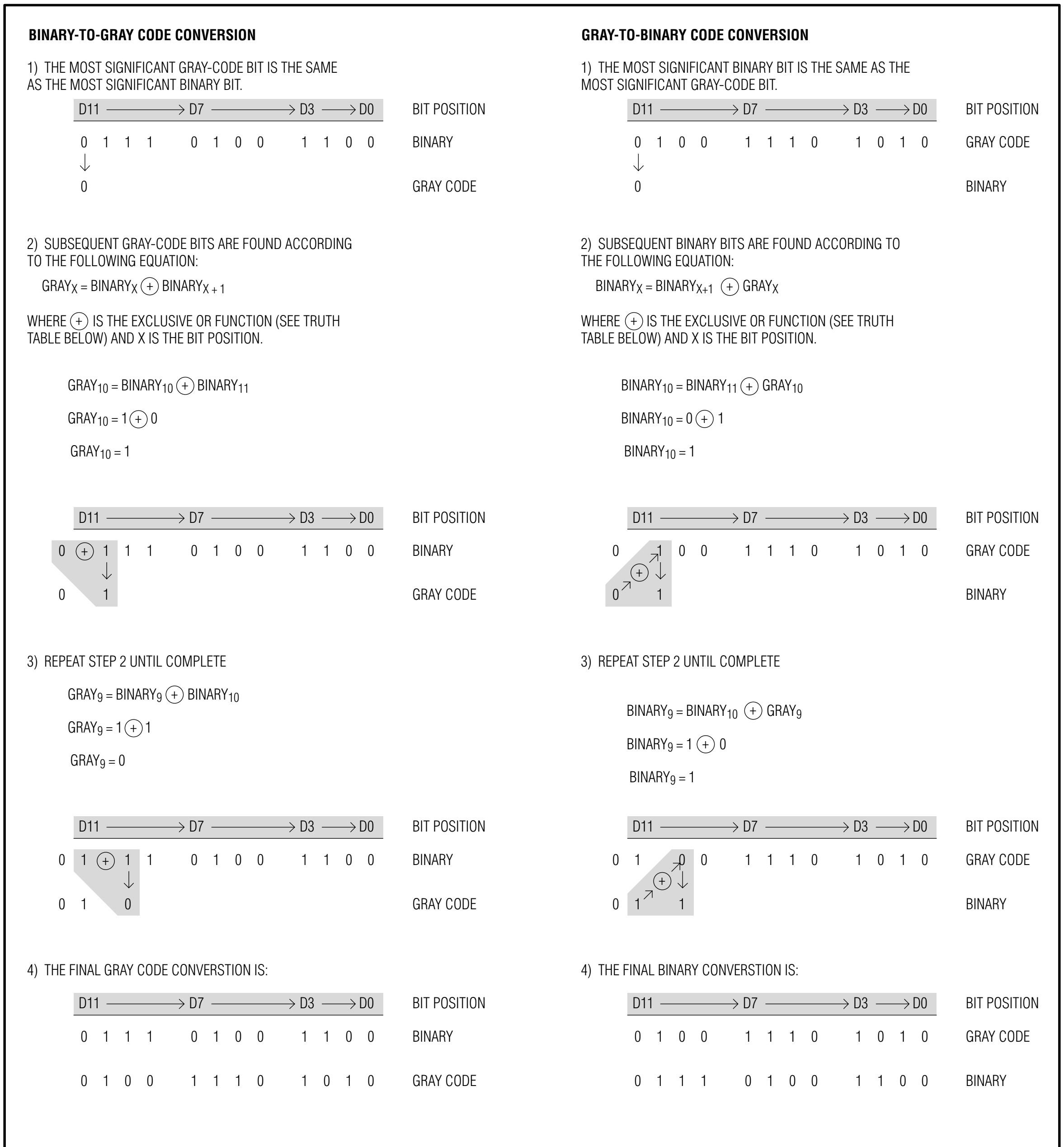


Figure 7. Gray Code Transfer Function ($G/\overline{T}$ = 1)



A	B	Y = A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

Figure 8. Binary-to-Gray and Gray-to-Binary Code Conversion

In power-down mode, all internal circuits are off, the analog supply current reduces to 0.045A, and the digital supply current reduces to 6µA. The following list shows the state of the analog inputs and digital outputs in power-down mode:

- INP, INN analog inputs are disconnected from the internal input amplifier (Figure 3).
- REFOUT has approximately 17kΩ to GND.
- REFP, COM, REFN go high impedance with respect to V_{DD} and GND, but there is an internal 4kΩ resistor between REFP and COM, as well as an internal 4kΩ resistor between REFN and COM.
- D0–D11, DOR, and DAV go high impedance.
- CLKP, CLKN clock inputs go high impedance (Figure 4).

The wake-up time from power-down mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 10ms. When operating in the unbuffered external reference mode, the wake-up time is dependent on the external reference drivers.

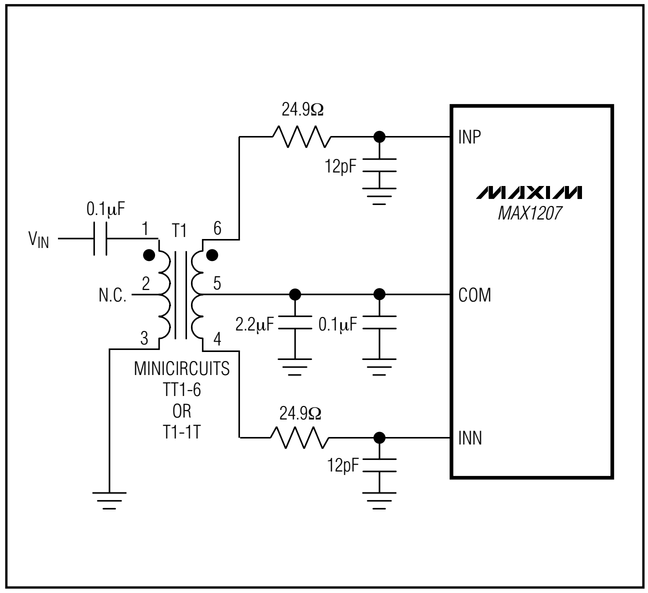


Figure 9. Transformer-Coupled Input Drive for Input Frequencies Up to Nyquist

Applications Information

Using Transformer Coupling

In general, the MAX1207 provides better SFDR and THD with fully differential input signals than single-ended input drive. In differential input mode, even-order harmonics are lower as both inputs are balanced, and each of the ADC inputs only requires half the signal swing compared to single-ended input mode.

An RF transformer (Figure 9) provides an excellent solution to convert a single-ended input source signal to a fully differential signal, required by the MAX1207 for optimum performance. Connecting the center tap of the transformer to COM provides a V_{DD} / 2 DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion. The configuration of Figure 9 is good for input frequencies up to Nyquist (f_{CLK} / 2).

The circuit of Figure 10 converts a single-ended input signal to fully differential just as in Figure 9. However, Figure 10 utilizes an additional transformer to improve the common-mode rejection, allowing high-frequency signals beyond the Nyquist frequency. The two sets of 49.9Ω termination resistors provide an equivalent 50Ω termination to the signal source. The second set of termination resistors connects to COM, providing the correct input common-mode voltage. Two 0Ω resistors in series with the analog inputs allow high IF input frequencies. These 0Ω resistors can be replaced with low-value resistors to limit the input bandwidth.

Single-Ended AC-Coupled Input Signal

Figure 11 shows an AC-coupled, single-ended input application. The MAX4108 provides high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity.

Buffered External Reference Drives Multiple ADCs

The buffered external reference mode allows for more control over the MAX1207 reference voltage and allows multiple converters to use a common reference. The REFIN input impedance is >50MΩ.

Figure 12 shows the MAX6062 precision bandgap reference used as a common reference for multiple converters. The 2.048V output of the MAX6062 passes through a one-pole 10Hz lowpass filter to the MAX4250. The MAX4250 buffers the 2.048V reference before its output is applied to the REFIN input of the MAX1207. The MAX4250 provides a low offset voltage (for high gain accuracy) and a low noise level.

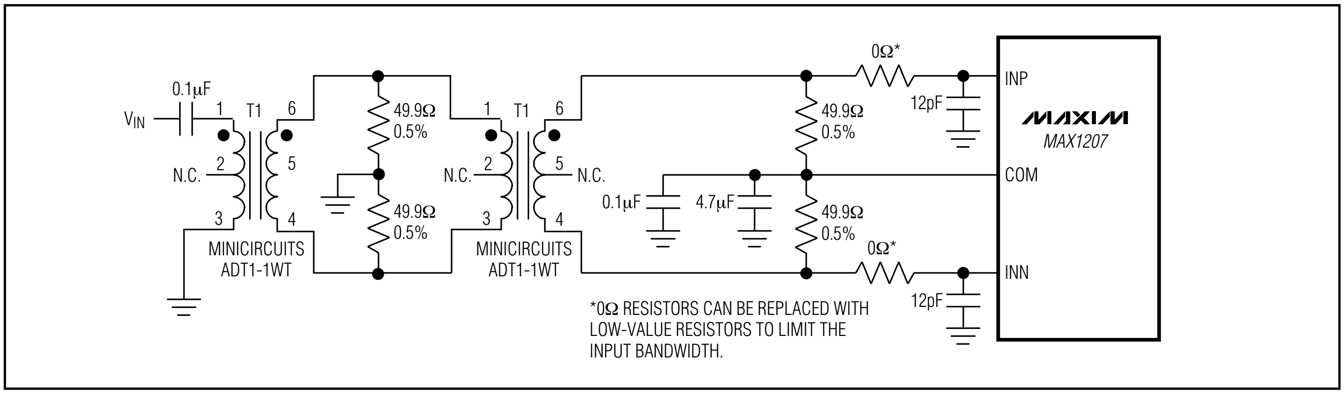


Figure 10. Transformer-Coupled Input Drive for Input Frequencies Beyond Nyquist

Unbuffered External Reference Drives Multiple ADCs

The unbuffered external reference mode allows for precise control over the MAX1207 reference and allows multiple converters to use a common reference. Connecting REFIN to GND disables the internal reference, allowing REFP, REFN, and COM to be driven directly by a set of external reference sources.

Figure 13 shows the MAX6066 precision bandgap reference used as a common reference for multiple converters. The 2.500V output of the MAX6066 is followed by a 10Hz lowpass filter and precision voltage-divider. The MAX4254 buffers the taps of this divider to provide the +2.000V, +1.500V, and +1.000V sources to drive REFP, REFN, and COM. The MAX4254 provides a low offset voltage and low noise level. The individual voltage followers are connected to 10Hz lowpass filters, which filter both the reference voltage and amplifier noise to a level of $3nV/\sqrt{Hz}$. The 2.000V and 1.000V reference voltages set the differential full-scale range of the associated ADCs at ±1.000V.

The common power supply for all active components removes any concern regarding power-supply sequencing when powering up or down.

With the outputs of the MAX4254 matching better than 0.1%, the buffers and subsequent lowpass support as many as 8 ADCs.

Grounding, Bypassing, and Board Layout

The MAX1207 requires high-speed board layout design techniques. Refer to the MAX1211 evaluation kit data sheet for a board layout reference. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a 2.2µF ceramic capacitor. Bypass OV_{DD} to GND with a

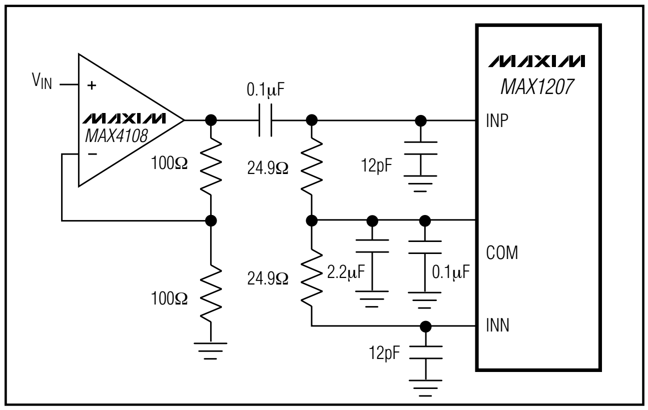


Figure 11. Single-Ended, AC-Coupled Input Drive

0.1µF ceramic capacitor in parallel with a 2.2µF ceramic capacitor.

Multilayer boards with ample ground and power planes produce the highest level of signal integrity. All MAX1207 GNDs and the exposed backside paddle must be connected to the same ground plane. The MAX1207 relies on the exposed backside paddle connection for a low-inductance ground connection. Use multiple vias to connect the top-side ground to the bottom-side ground. Isolate the ground plane from any noisy digital system ground planes such as a DSP or output buffer ground.

Route high-speed digital signal traces away from the sensitive analog traces. Keep all signal lines short and free of 90° turns.

Ensure that the differential analog input network layout is symmetric and that all parasitics are balanced equally. Refer to the MAX1211 evaluation kit data sheet for an example of symmetric input layout.

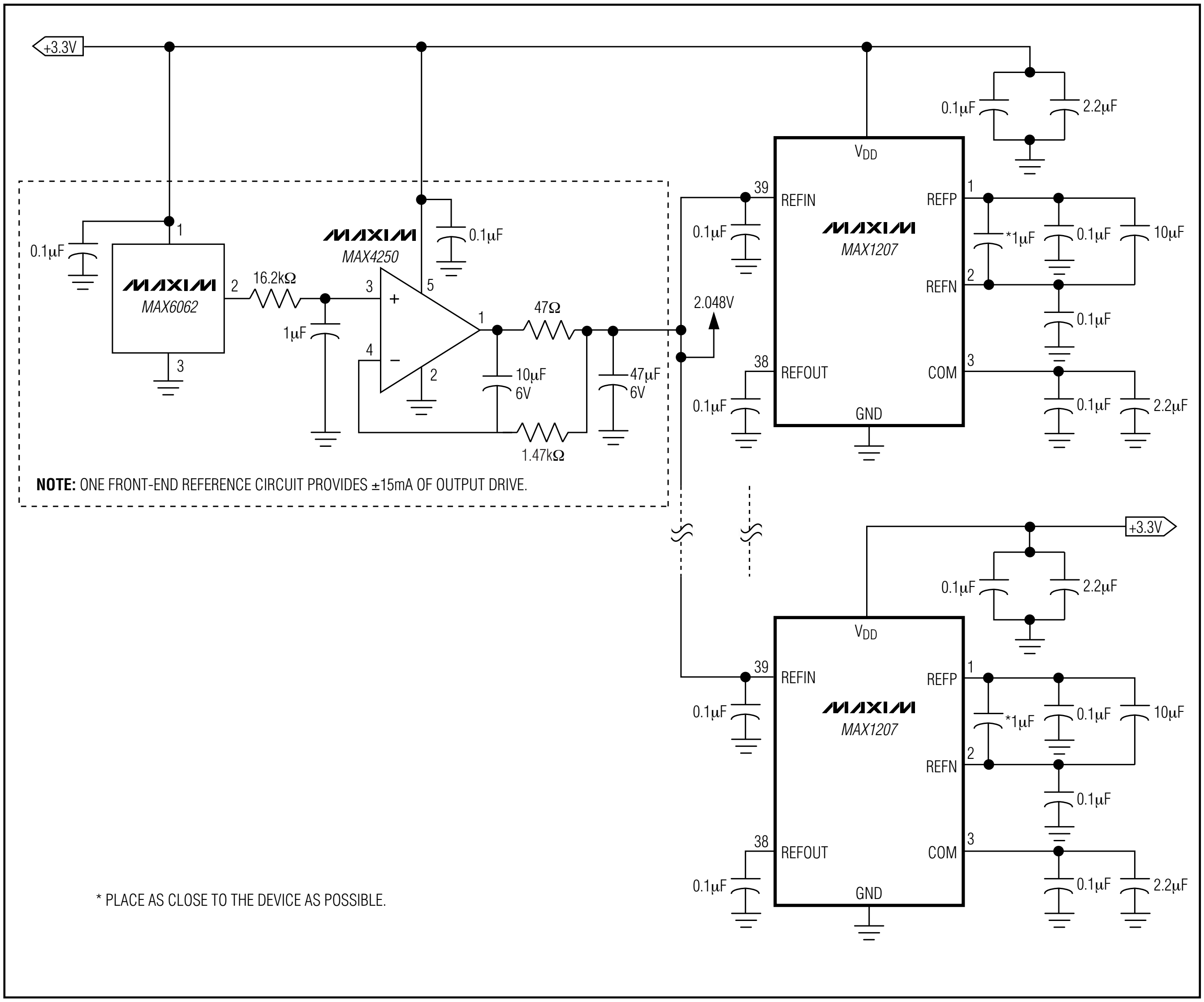


Figure 12. External Buffered (MAX4250) Reference Drive Using a MAX6062 Bandgap Reference

Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1207 are guaranteed by design using the best-straight-line fit method.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Ideally, the midscale MAX1207 transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured transition point and the ideal transition point.

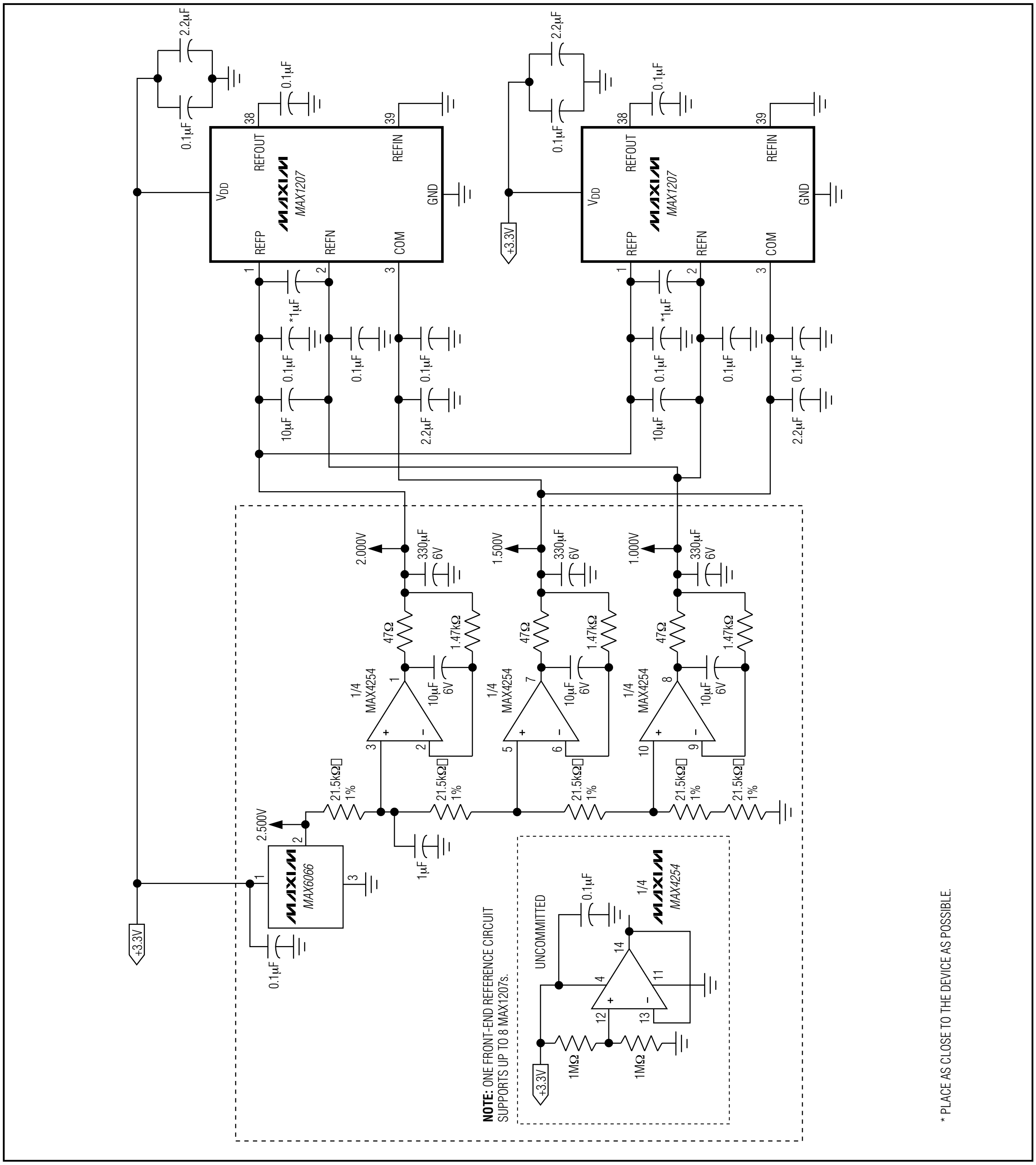


Figure 13. External Unbuffered Reference Driving 8 ADCs with MAX4254 and MAX6066

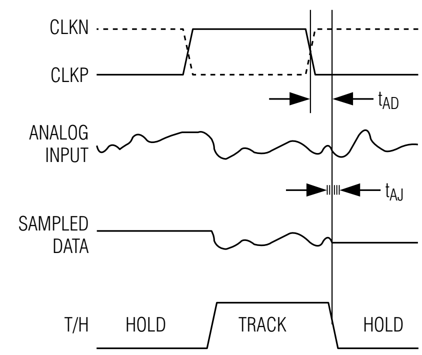


Figure 14. T/H Aperture Timing

Gain Error

Ideally, the positive full-scale MAX1207 transition occurs at 1.5 LSB below positive full scale, and the negative full-scale transition occurs at 0.5 LSB above negative full scale. The gain error is the difference of the measured transition points minus the difference of the ideal transition points.

Aperture Jitter

Figure 14 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 14).

Overdrive Recovery Time

Overdrive recovery time is the time required for the ADC to recover from an input transient that exceeds the full-scale limits. The MAX1207 specifies overdrive recovery time using an input transient that exceeds the full-scale limits by ±10%.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency, excluding the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02}\right)$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_7 are the amplitudes of the 2nd- through 7th-order harmonics (HD2–HD7).

Single-Tone Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS amplitude of the next-largest spurious component, excluding DC offset.

Two-Tone Spurious-Free Dynamic Range ($SFDR_{TT}$)

$SFDR_{TT}$ represents the ratio, expressed in decibels, of the RMS amplitude of either input tone to the RMS amplitude of the next-largest spurious component in the spectrum, excluding DC offset. This spurious component can occur anywhere in the spectrum up to Nyquist and is usually an intermodulation product or a harmonic.

Intermodulation Distortion (IMD)

IMD is the ratio of the RMS sum of the intermodulation products to the RMS sum of the two fundamental input tones. This is expressed as:

$$IMD = 20 \times \log\left(\frac{\sqrt{V_{IMP1}^2 + V_{IMP2}^2 + \cdots + V_{IMPn}^2}}{\sqrt{V_1^2 + V_2^2}}\right)$$

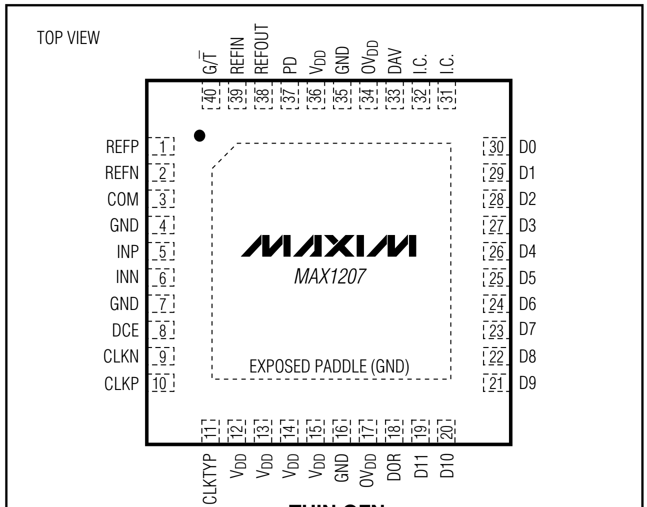
The fundamental input tone amplitudes (V_1 and V_2) are at -7dBFS. Fourteen intermodulation products ($V_{IMP\_}$) are used in the MAX1207 calculation. The intermodulation products are the amplitudes of the output spectrum at the following frequencies:

- 2nd-order intermodulation products: f1 + f2, f2 - f1
- 3rd-order intermodulation products: 2 x f1 - f2, 2 x f2 - f1, 2 x f1 + f2, 2 x f2 + f1
- 4th-order intermodulation products: 3 x f1 - f2, 3 x f2 - f1, 3 x f1 + f2, 3 x f2 + f1
- 5th-order intermodulation products: 3 x f1 - 2 x f2, 3 x f2 - 2 x f1, 3 x f1 + 2 x f2, 3 x f2 + 2 x f1

3rd-Order Intermodulation (IM3)

IM3 is the total power of the 3rd-order intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f1 and f2. The individual input tone levels are at -7dBFS. The 3rd-order intermodulation products are 2 x f1 - f2, 2 x f2 - f1, 2 x f1 + f2, 2 x f2 + f1.

Pin Configuration



THIN QFN
6mm × 6mm × 0.8mm

Chip Information

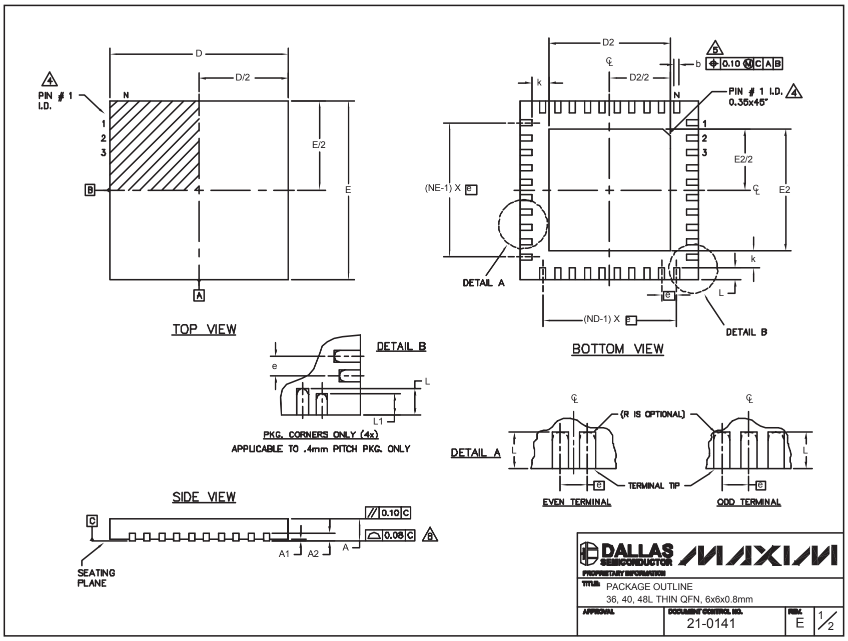
TRANSISTOR COUNT: 18,700

PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

Note: For the MAX1207 exposed pad variations, the package code is T4066-3.



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR / MAXIM

TITLE: PACKAGE OUTLINE 36, 40, 48L THIN QFN, 6x6x0.8mm

DOCUMENT CONTROL NO.: 21-0141 REV.: E 2/2

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