ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +36V
GND to PGND .....-0.3V to +0.3V
VL to GND .....-0.3V to +6V
BST to GND .....-0.3V to +36V
DH to LX .....-0.3V to (BST + 0.3V)
LX to BST .....-6V to +0.3V
$\overline{SHDN}$ to GND .....-0.3V to (V+ + 0.3V)
SYNC, SS, REF, SECFB, $\overline{SKIP}$, FB to GND ...-0.3V to (VL + 0.3V)
DL to PGND .....-0.3V to (VL + 0.3V)
CSH, CSL to GND .....-0.3V to +6V
VL Short Circuit to GND .....Momentary
REF Short Circuit to GND .....Continuous
VL Output Current .....+50mA to -1mA
REF Output Current .....+5mA to -1mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.70mW/°C above +70°C) 696mW
QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range
MAX165_E_E .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +15V, GND = PGND = 0V, SYNC = REF, I_{VL} = I_{REF} = 0A, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
3.3V AND 5V STEP-DOWN CONTROLLERS						
Input Supply Range			4.5		30	V
5V Output Voltage (CSL)	0 < (CSH - CSL) < 80mV, FB = VL, 6V < V+ < 30V, includes line and load regulation		4.85	5.06	5.25	V
3.3V Output Voltage (CSL)	0 < (CSH - CSL) < 80mV, FB = 0V, 4.5V < V+ < 30V, includes line and load regulation		3.20	3.34	3.46	V
Nominal Adjustable Output Voltage Range	External resistor divider	MAX1655	1		5.5	V
		MAX1652/MAX1653/MAX1654	2.5		5.5	
Feedback Voltage	$\overline{CSH}$ - CSL = 0V, CSL = FB, $\overline{SKIP}$ = 0V, 4.5V < V+ < 30V	MAX1655	0.97	1.00	1.03	V
		MAX1652/MAX1653/MAX1654	2.43	2.50	2.57	
Load Regulation	0 < (CSH - CSL) < 80mV			2		%
	25mV < (CSH - CSL) < 80mV			1.2		
Line Regulation	6V < V+ < 30V			0.03	0.06	%/V
Current-Limit Voltage	CSH - CSL, positive		80	100	120	mV
	CSH - CSL, negative		-50	-100	-160	
SS Source Current	V_{SS} = 0V		2.5	4.0	6.5	µA
SS Fault Sink Current	V_{SS} = 4V		2.0			mA
FLYBACK/PWM CONTROLLER						
SECFB Regulation Setpoint	Falling edge, rising edge, hysteresis = 22mV (MAX1652)		2.45	2.50	2.55	V
	Rising edge, falling edge, hysteresis = 22mV (MAX1654)		-0.05	0	0.05	
INTERNAL REGULATOR AND REFERENCE						
VL Output Voltage	$\overline{SHDN}$ = 2V, 0 < I_{VL} < 25mA, 5.5V < V+ < 30V		4.7	5.0	5.3	V
VL Fault Lockout Voltage	Rising edge, falling edge hysteresis = 50mV		3.8	3.9	4.0	V
VL/CSL Switchover Voltage	Rising edge, falling edge hysteresis = 60mV		4.2	4.5	4.7	V

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +15V, GND = PGND = 0V, SYNC = REF, I_{VL} = I_{REF} = 0A, **T_A = 0°C to +85°C,** unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Output Voltage	No external load (Note 1)	2.46	2.50	2.54	V
Reference Fault Lockout Voltage	Falling edge	2.0		2.4	V
Reference Load Regulation	0 < I_{REF} < 100µA			15	mV
CSL, CSH Shutdown Leakage Current	$\overline{SHDN}$ = 0V, CSL = 5.5V, CSH = 5.5V, V+ = 0 or 30V, VL = 0V		0.1	1	µA
V+ Shutdown Current	$\overline{SHDN}$ = 0V, V+ = 30V, CSL = 0 or 5.5V		3	7	µA
V+ Off-State Leakage Current	FB = CSH = CSL = 5.5V, VL switched over to CSL		5	15	µA
Dropout Power Consumption	V+ = 4.5V, CSH = CSL = 4.0V (Note 2)		1	8	mW
Quiescent Power Consumption	CSH = CSL = 5.5V		1	2	mW
OSCILLATOR AND INPUTS/OUTPUTS					
Oscillator Frequency	SYNC = REF	270	300	330	kHz
	SYNC = 0 or 5V	125	150	175	
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			ns
SYNC Rise/Fall Time	Guaranteed by design, not tested			200	ns
Oscillator Sync Range		190		340	kHz
Dropout-Mode Maximum Duty Cycle	SYNC = REF	97	98		%
	SYNC = 0 or 5V	98	99		
Input High Voltage	SYNC	VL - 0.5			V
	$\overline{SHDN}$, $\overline{SKIP}$	2.0			
Input Low Voltage	SYNC			0.8	V
	$\overline{SHDN}$, $\overline{SKIP}$			0.5	
Input Current	$\overline{SHDN}$, 0 or 30V			3.0	µA
	SECFB, 0 or 4V			0.1	
	SYNC, $\overline{SKIP}$			1.0	
	CSH, CSL, CSH = CSL ≤ 4V			70	
	FB, FB = REF			±0.1	
DL Sink/Source Current	DL forced to 2V		1		A
DH Sink/Source Current	DH forced to 2V, BST - LX = 4.5V		1		A
DL On-Resistance	High or low		1.5	5	Ω
DH On-Resistance	High or low, BST - LX = 4.5V		1.5	5	Ω

Note 1: Since the reference uses VL as its supply, V+ line-regulation error is insignificant.

Note 2: At very low input voltages, quiescent supply current may increase due to excessive PNP base current in the VL linear regulator. This occurs if V+ falls below the preset VL regulation point (5V nominal).

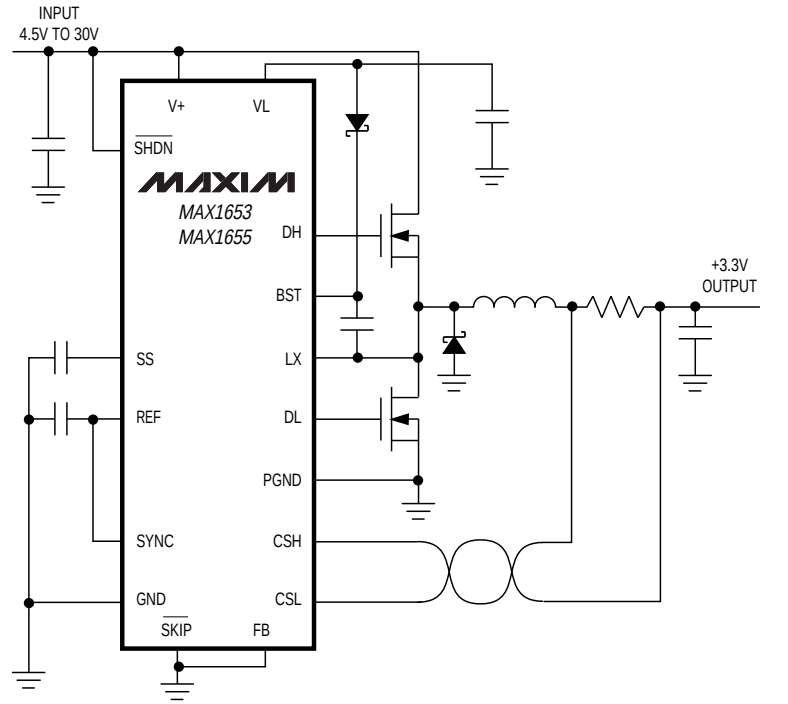
ELECTRICAL CHARACTERISTICS (continued)

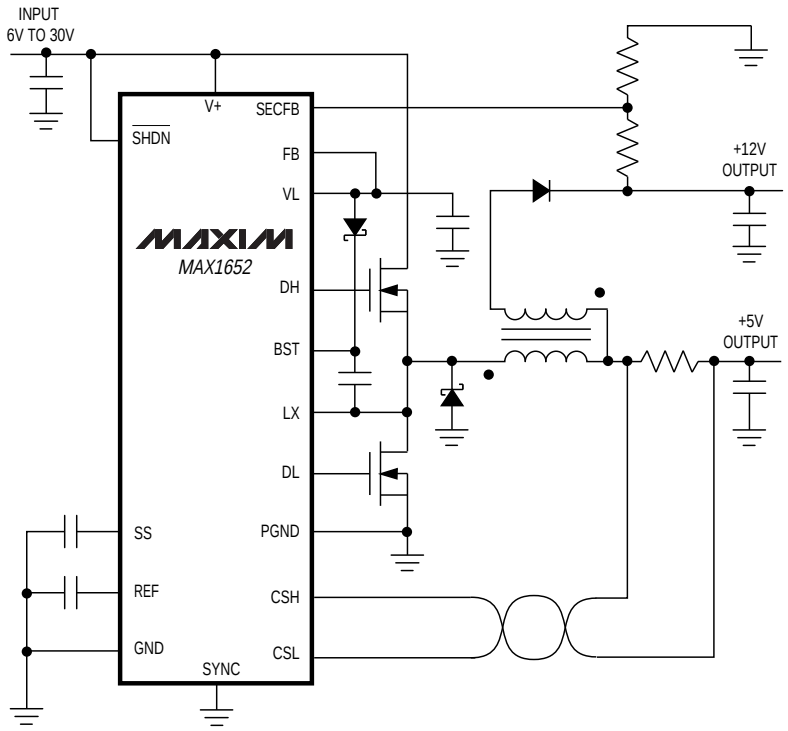
(V+ = +15V, GND = PGND = 0V, SYNC = REF, I_{VL} = I_{REF} = 0A, **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
3.3V and 5V STEP-DOWN CONTROLLERS						
Input Supply Range			4.5		30	V
5V Output Voltage (CSL)	0 < (CSH - CSL) < 70mV, FB = VL, 6V < V+ < 30V, includes line and load regulation		4.80		5.30	V
3.3V Output Voltage (CSL)	0 < (CSH - CSL) < 70mV, FB = VL, 4.5V < V+ < 30V, includes line and load regulation		3.16		3.50	V
Feedback Voltage	CSH - CSL = 0V, 5V < V+ < 30V, CSL = FB, $\overline{SKIP}$ = 0V	MAX1655	0.96		1.04	V
		MAX1652/MAX1653/ MAX1654	2.40		2.60	
Line Regulation	6V < V+ < 30V				0.06	%/V
Current-Limit Voltage	CSH - CSL, positive		70		130	mV
	CSH - CSL, negative		-40		-160	
FLYBACK/PWM CONTROLLER						
SECFB Regulation Setpoint	Falling edge, hysteresis = 22mV (MAX1652)		2.40		2.60	V
	Falling edge, hysteresis = 22mV (MAX1654)		-0.08		0.08	
INTERNAL REGULATOR AND REFERENCE						
VL Output Voltage	$\overline{SHDN}$ = 2V, 0 < I_{VL} < 25mA, 5.5V < V+ < 30V		4.7		5.3	V
VL Fault Lockout Voltage	Rising edge, hysteresis = 50mV		3.75		4.05	V
VL/CSL Switchover Voltage	Rising edge, hysteresis = 60mV		4.2		4.7	V
Reference Output Voltage	No external load (Note 1)		2.43		2.57	V
Reference Load Regulation	0 < I_{REF} < 100µA				15	mV
V+ Shutdown Current	$\overline{SHDN}$ = 0V, V+ = 30V, CSL = 0 or 5.5V				10	µA
V+ Off-State Leakage Current	FB = CSH = CSL = 5.5V, VL switched over to CSL				15	µA
Quiescent Power Consumption					2	mW
OSCILLATOR AND INPUTS/OUTPUTS						
Oscillator Frequency	SYNC = REF		250		350	kHz
	SYNC = 0 or 5V		120		180	
SYNC High Pulse Width			250			ns
SYNC Low Pulse Width			250			ns
Oscillator Sync Range			210		320	kHz
Maximum Duty Cycle	SYNC = REF		97			%
	SYNC = 0 or 5V		98			
DL On-Resistance	High or low				5	Ω
DH On-Resistance	High or low, BST - LX = 4.5V				5	Ω

Note 3: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

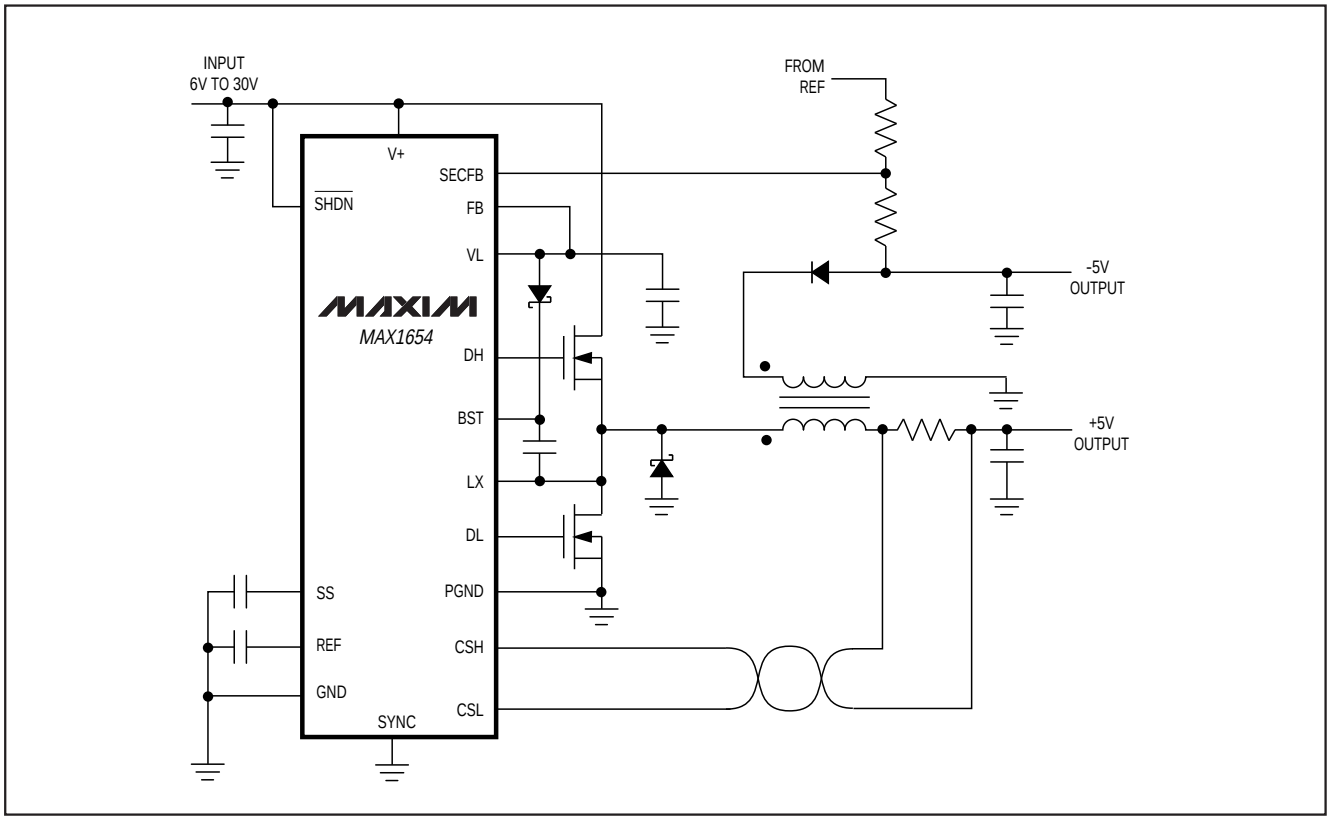
Typical Operating Circuits





High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

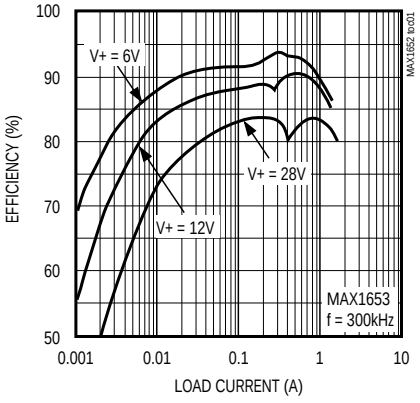
Typical Operating Circuits (continued)



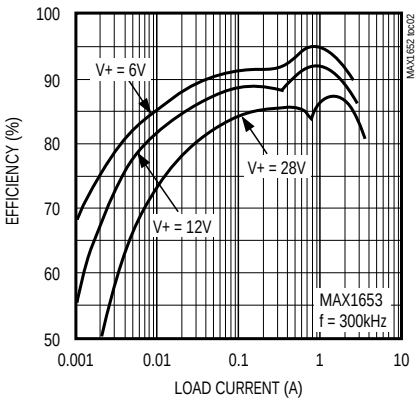
Typical Operating Characteristics

(Circuit of Figure 1, $\overline{SKIP}$ = GND, T_A = +25°C, unless otherwise noted.)

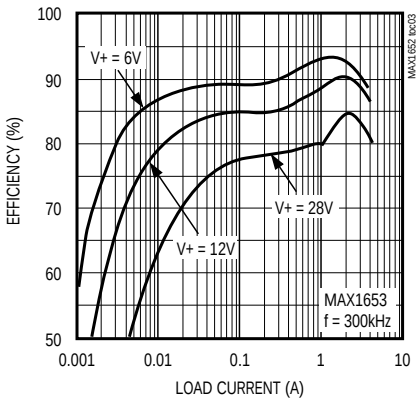
EFFICIENCY vs. LOAD CURRENT (3.3V/1A CIRCUIT)



EFFICIENCY vs. LOAD CURRENT (3.3V/2A CIRCUIT)



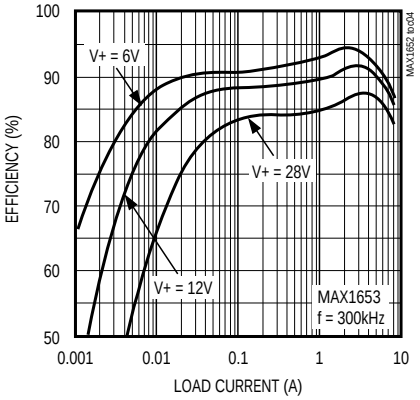
EFFICIENCY vs. LOAD CURRENT (3.3V/3A CIRCUIT)



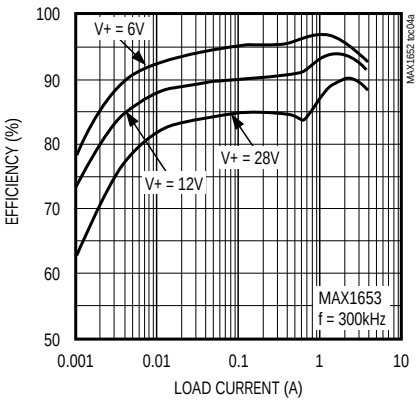
Typical Operating Characteristics (continued)

(Circuit of Figure 1, $\overline{SKIP}$ = GND, T_A = +25°C, unless otherwise noted.)

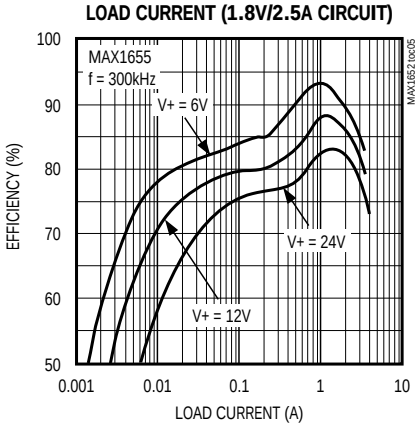
EFFICIENCY vs. LOAD CURRENT (3.3V/5A CIRCUIT)



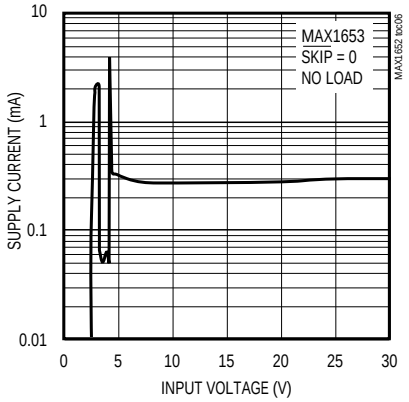
EFFICIENCY vs. LOAD CURRENT (5V/3A CIRCUIT)



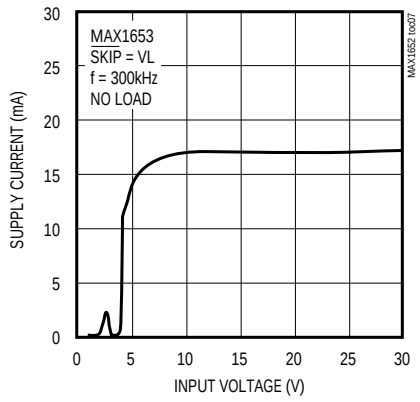
EFFICIENCY vs. LOAD CURRENT (1.8V/2.5A CIRCUIT)



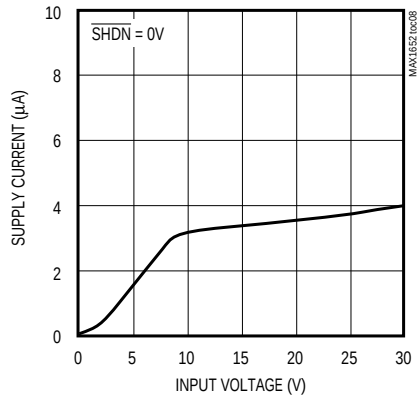
IDLE-MODE SUPPLY CURRENT vs. INPUT VOLTAGE (3.3V/3A CIRCUIT)



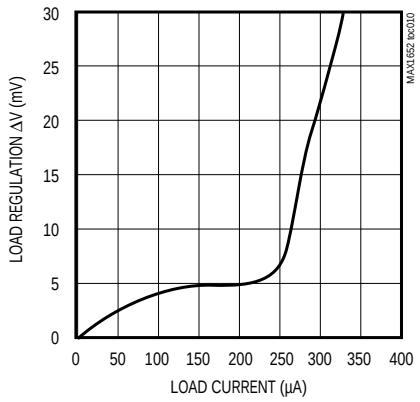
PWM-MODE SUPPLY CURRENT vs. INPUT VOLTAGE (3.3V/3A CIRCUIT)



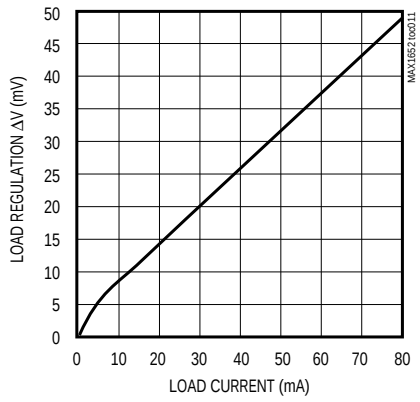
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



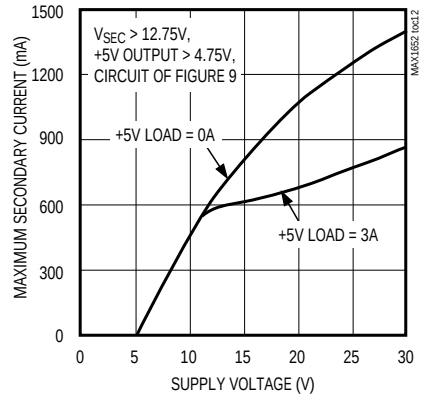
REF LOAD-REGULATION ERROR vs. REF LOAD CURRENT



VL LOAD-REGULATION ERROR vs. VL LOAD CURRENT



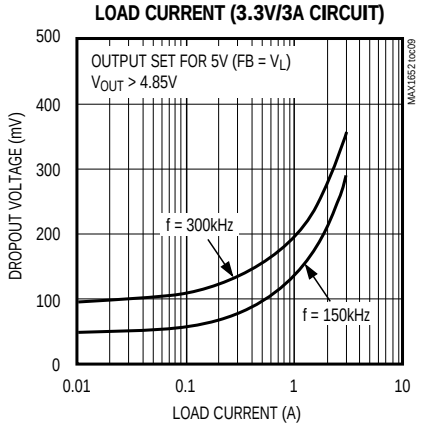
MAX1652 MAXIMUM SECONDARY OUTPUT CURRENT vs. SUPPLY VOLTAGE



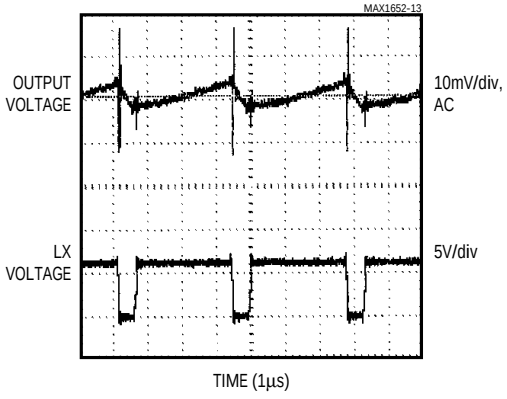
Typical Operating Characteristics (continued)

(Circuit of Figure 1, $\overline{SKIP}$ = GND, T_A = +25°C, unless otherwise noted.)

DROPOUT VOLTAGE vs. LOAD CURRENT (3.3V/3A CIRCUIT)

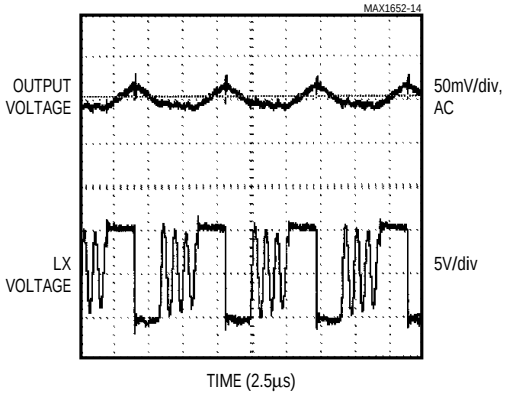


PULSE-WIDTH-MODULATION MODE WAVEFORMS



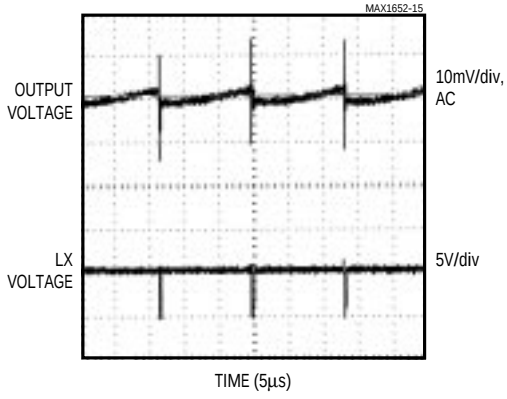
V_{IN} = 6V, 3.3V/3A CIRCUIT

IDLE-MODE WAVEFORMS



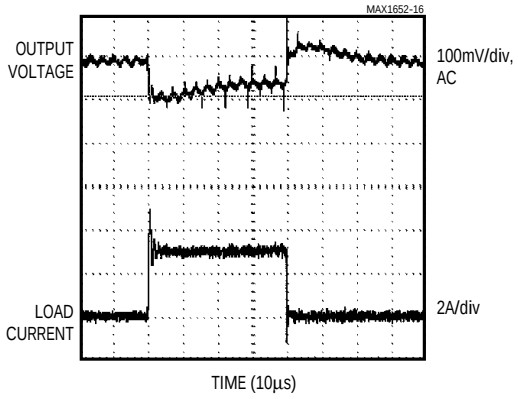
I_{LOAD} = 300mA, V_{IN} = 10V, 3.3V/3A CIRCUIT

DROPOUT WAVEFORMS



V_{IN} = 5.1V, NO LOAD, 3.3V/3A CIRCUIT, SET TO 5V OUTPUT (FB = VL)

LOAD-TRANSIENT RESPONSE



V_{IN} = 15V, 3.3V/3A CIRCUIT

Pin Description

PIN	NAME	FUNCTION
1	SS	Soft-Start Timing Capacitor Connection. Ramp time to full current limit is approximately 1ms/nF.
2	SECFB (MAX1652/ MAX1654)	Secondary Winding Feedback Input. Normally connected to a resistor divider from an auxiliary output. **Don't leave SECFB unconnected.** • MAX1652: SECFB regulates at VSECFB = 2.50V. Tie to VL if not used. • MAX1654: SECFB regulates at VSECFB = 0V. Tie to a negative voltage through a high-value current-limiting resistor (I_{MAX} = 100µA) if not used.
	$\overline{SKIP}$ (MAX1653/ MAX1655)	Disables pulse-skipping mode when high. Connect to GND for normal use. **Don't leave $\overline{SKIP}$ unconnected.** With $\overline{SKIP}$ grounded, the device will *automatically* change from pulse-skipping operation to full PWM operation when the load current exceeds approximately 30% of maximum (Table 3).
3	REF	Reference Voltage Output. Bypass to GND with 0.33µF minimum.
4	GND	Low-Noise Analog Ground and Feedback Reference Point
5	SYNC	Oscillator Synchronization and Frequency Select. Tie to GND or VL for 150kHz operation; tie to REF for 300kHz operation. A high-to-low transition begins a new cycle. Drive SYNC with 0 to 5V logic levels (see the *Electrical Characteristics* table for V_{IH} and V_{IL} specifications). SYNC capture range is 190kHz to 340kHz.
6	$\overline{SHDN}$	Shutdown Control Input, active low. Logic threshold is set at approximately 1V (V_{TH} of an internal N-channel MOSFET). Tie $\overline{SHDN}$ to V+ for automatic start-up.
7	FB	Feedback Input. Regulates at the feedback voltage in adjustable mode. FB is a Dual Mode™ input that also selects the fixed output voltage settings as follows: • Connect to GND for 3.3V operation. • Connect to VL for 5V operation. • Connect FB to a resistor divider for adjustable mode. FB can be driven with +5V CMOS logic in order to change the output voltage under system control.
8	CSH	Current-Sense Input, high side. Current-limit level is 100mV referred to CSL.
9	CSL	Current-Sense Input, low side. Also serves as the feedback input in fixed-output modes.
10	V+	Battery Voltage Input (4.5V to 30V). Bypass V+ to PGND close to the IC with a 0.1µF capacitor. Connects to a linear regulator that powers VL.
11	VL	5V Internal Linear-Regulator Output. VL is also the supply voltage rail for the chip. VL is switched to the output voltage via CSL (V_{CSL} > 4.5V) for automatic bootstrapping. Bypass to GND with 4.7µF. VL can supply up to 5mA for external loads.
12	PGND	Power Ground
13	DL	Low-Side Gate-Drive Output. Normally drives the synchronous-rectifier MOSFET. Swings from 0V to VL.
14	BST	Boost Capacitor Connection for High-Side Gate Drive (0.1µF)
15	LX	Switching Node (inductor) Connection. Can swing 2V below ground without hazard.
16	DH	High-Side Gate-Drive Output. Normally drives the main buck switch. DH is a floating driver output that swings from LX to BST, riding on the LX switching-node voltage.

Dual Mode is a trademark of Maxim Integrated Products.

High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

Standard Application Circuits

It's easy to adapt the basic MAX1653 single-output 3.3V buck converter (Figure 1) to meet a wide range of applications with inputs up to 30V (limited by choice of external MOSFET). Simply substitute the appropriate components from Table 1 (candidate suppliers are provided in Table 2). These circuits represent a good set of trade-offs among cost, size, and efficiency while staying within the worst-case specification limits for stress-related parameters such as capacitor ripple current.

Don't change the frequency of these circuits without first recalculating component values (particularly inductance value at maximum battery voltage).

For a discussion of dual-output circuits using the MAX1652 and MAX1654, see Figure 9 and the *Secondary Feedback-Regulation Loop* section.

Detailed Description

The MAX1652 family are BiCMOS, switch-mode power-supply controllers designed primarily for buck-topology regulators in battery-powered applications where high efficiency and low quiescent supply current are critical. The parts also work well in other topologies such as boost, inverting, and Cuk due to the flexibility of their floating high-speed gate driver. Light-load efficiency is enhanced by automatic idle-mode operation—a variable-frequency pulse-skipping mode that reduces losses due to MOSFET gate charge. The step-down power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average of the AC voltage at the switching node, which is adjusted and regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the N-channel high-side MOSFET must exceed the battery voltage and is provided by a flying capacitor boost circuit that uses a 100nF capacitor connected to BST.

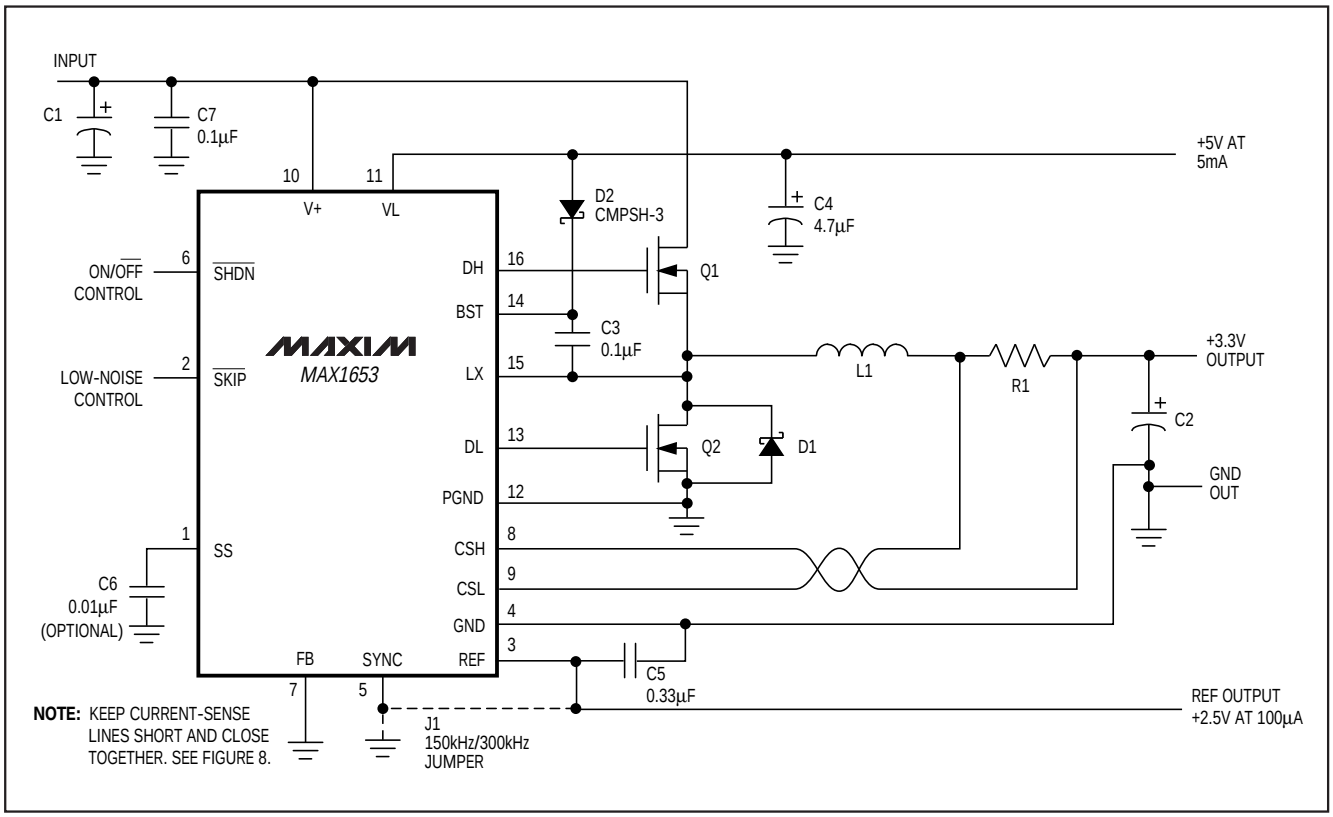


Figure 1. Standard 3.3V Application Circuit (see Table 1 for Component Values)

Table 1. Component Selection for Standard Applications

COMPONENT	3.3V at 1A	3.3V at 2A	5V/3.3V at 3A	3.3V at 5A	1.8V at 2.5A
Input Range	4.75V to 28V	4.75V to 28V	4.75V to 28V	4.75V to 28V	4.75V to 22V
Frequency	300kHz	300kHz	300kHz	300kHz	150kHz
Q1 High-Side MOSFET	International Rectifier 1/2 IRF7101	International Rectifier 1/2 IRF7303 or Fairchild Semiconductor 1/2 NDS8936	International Rectifier IRF7403 or Fairchild Semiconductor NDS 8410A	Fairchild Semiconductor FDS6680	International Rectifier 1/2 IRF7303 or Fairchild Semiconductor 1/2 NDS8936
Q2 Low-Side MOSFET	International Rectifier 1/2 IRF7101	International Rectifier 1/2 IRF7303 or Fairchild Semiconductor 1/2 NDS8936	International Rectifier IRF7403 or Fairchild Semiconductor NDS 8410A	Fairchild Semiconductor FDS6680	International Rectifier 1/2 IRF7303 or Fairchild Semiconductor 1/2 NDS8936
C1 Input Capacitor	10µF, 35V AVX TPSD106M035R0300	22µF, 35V AVX TPSE226M035R0300	(2) 22µF, 35V AVX TPSE226M035R0300	(3) 22µF, 35V AVX TPSE226M035R0300	10µF, 25V ceramic Taiyo Yuden TMK325F106Z
C2 Output Capacitor	100µF, 6.3V AVX TPSC107M006R	220µF, 10V AVX TPSE227M010R0100 or Sprague 594D227X001002T	470µF, 6V (for 3.3V) Kemet T510X477M006AS **or** (2) 220µF, 10V (for 5V) AVX TPSE227M010R011	(3) 330µF, 10V Sprague 594D337X0010R2T **or** (2) 470µF, 6V Kemet T510X477M006AS	470µF, 4V Sprague 594D477X0004R2T **or** 470µF, 6V Kemet T510X477M006AS
D1 Rectifier	1N5819 or Motorola MBR0520L	1N5819 or Motorola MBRS130LT3	1N5819 or Motorola MBRS130LT3	1N5821 or Motorola MBRS340T3	1N5817 or Motorola MBRS130LT3
R1 Sense Resistor	70mΩ Dale WSL-1206-R070F or IRC LR2010-01-R070	33mΩ Dale WSL-2010-R033F or IRC LR2010-01-R033	25mΩ Dale WSL-2010-R025F or IRC LR2010-01-R025	12mΩ Dale WSL-2512-R012F	30mΩ Dale WSL-2010-R030F or IRC LR2010-01-R030
L1 Inductor	33µH Sumida CDR74B-330	15µH Sumida CDR105B-150	10µH Sumida CDRH125-100	4.7µH Sumida CDRH127-4R7	15µH Sumida CDRH125-150

Table 2. Component Suppliers

MANUFACTURER	USA PHONE	FACTORY FAX [Country Code]
AVX	803-946-0690	[1] 803-626-3123
Central Semiconductor	516-435-1110	[1] 516-435-1824
Coilcraft	847-639-6400	[1] 847-639-1469
Coiltronics	561-241-7876	[1] 561-241-9339
Dale	605-668-4131	[1] 605-665-1627
Fairchild	408-822-2181	[1] 408-721-1635
International Rectifier	310-322-3331	[1] 310-322-3332
IRC	512-992-7900	[1] 512-992-3377
Kemet	408-986-0424	[1] 408-986-1442
Matsuo	714-969-2491	[1] 714-960-6492
Motorola	602-303-5454	[1] 602-994-6430

MANUFACTURER	USA PHONE	FACTORY FAX [Country Code]
Murata	814-237-1431 800-831-9172	[1] 814-238-0490
NIEC	805-867-2555*	[81] 3-3494-7414
Sanyo	619-661-6835	[81] 7-2070-1174
Siliconix	408-988-8000 800-554-5565	[1] 408-970-3950
Sprague	603-224-1961	[1] 603-224-1430
Sumida	847-956-0666	[81] 3-3607-5144
Taiyo Yuden	408-573-4150	[1] 408-573-4159
TDK	847-390-4461	[1] 847-390-4405
Transpower Technologies	702-831-0140	[1] 702-831-3521

** Distributor*

The MAX1652–MAX1655 contain nine major circuit blocks, which are shown in Figure 2:

PWM Controller Blocks:

- Multi-Input PWM Comparator
- Current-Sense Circuit
- PWM Logic Block
- Dual-Mode Internal Feedback Mux
- Gate-Driver Outputs
- Secondary Feedback Comparator

Bias Generator Blocks:

- +5V Linear Regulator
- Automatic Bootstrap Switchover Circuit
- +2.50V Reference

These internal IC blocks aren't powered directly from the battery. Instead, a +5V linear regulator steps down the battery voltage to supply both the IC internal rail (VL pin) as well as the gate drivers. The synchronous-switch gate driver is directly powered from +5V VL, while the high-side-switch gate driver is indirectly powered from VL via an external diode-capacitor boost circuit. An automatic bootstrap circuit turns off the +5V linear regulator and powers the IC from its output voltage if the output is above 4.5V.

PWM Controller Block

The heart of the current-mode PWM controller is a multi-input open-loop comparator that sums three signals: output voltage error signal with respect to the reference voltage, current-sense signal, and slope compensation ramp (Figure 3). The PWM controller is a direct summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches the ideal of cycle-by-cycle control over the output voltage.

Under heavy loads, the controller operates in full PWM mode. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT}/V_{IN}). As the high-side switch turns off, the synchronous rectifier latch is set. 60ns later the low-side switch turns on, and stays on until the beginning of the next clock cycle (in continuous mode) or until the inductor current crosses zero (in discontinuous mode). Under fault conditions where the inductor current exceeds the 100mV current-limit threshold, the high-side latch resets and the high-side switch turns off.

If the load is light in Idle Mode ($\overline{SKIP}$ = low), the inductor current does not exceed the 25mV threshold set by the Idle Mode comparator. When this occurs, the controller skips most of the oscillator pulses in order to reduce the switching frequency and cut back gate-charge losses. The oscillator is effectively gated off at light loads because the Idle Mode comparator immediately resets the high-side latch at the beginning of each cycle, unless the feedback signal falls below the reference voltage level.

When in PWM mode, the controller operates as a fixed-frequency current-mode controller where the duty ratio is set by the input/output voltage ratio. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak current, the circuit acts as a switch-mode transconductance amplifier and pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current "staircasing," a slope-compensation ramp is summed into the main PWM comparator to reduce the apparent duty factor to less than 50%.

The relative gains of the voltage- and current-sense inputs are weighted by the values of current sources that bias three differential input stages in the main PWM comparator (Figure 4). The relative gain of the voltage comparator to the current comparator is internally fixed at K = 2:1. The resulting loop gain (which is relatively low) determines the 2% typical load regulation error. The low loop-gain value helps reduce output filter capacitor size and cost by shifting the unity-gain crossover to a lower frequency.

The output filter capacitor C2 sets a dominant pole in the feedback loop. This pole must roll off the loop gain to unity before the zero introduced by the output capacitor's parasitic resistance (ESR) is encountered (see *Design Procedure* section). A 12kHz pole-zero cancellation filter provides additional rolloff above the unity-gain crossover. This internal 12kHz lowpass compensation filter cancels the zero due to the filter capacitor's ESR. The 12kHz filter is included in the loop in both fixed- and adjustable-output modes.

Synchronous-Rectifier Driver (DL Pin)

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode with a low-resistance MOSFET switch. The synchronous rectifier also ensures proper start-up of the boost-gate driver circuit. If you must omit the synchronous power MOSFET for cost or other reasons, replace it with a small-signal MOSFET such as a 2N7002.

If the circuit is operating in continuous-conduction mode, the DL drive waveform is simply the complement of the DH high-side drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through").

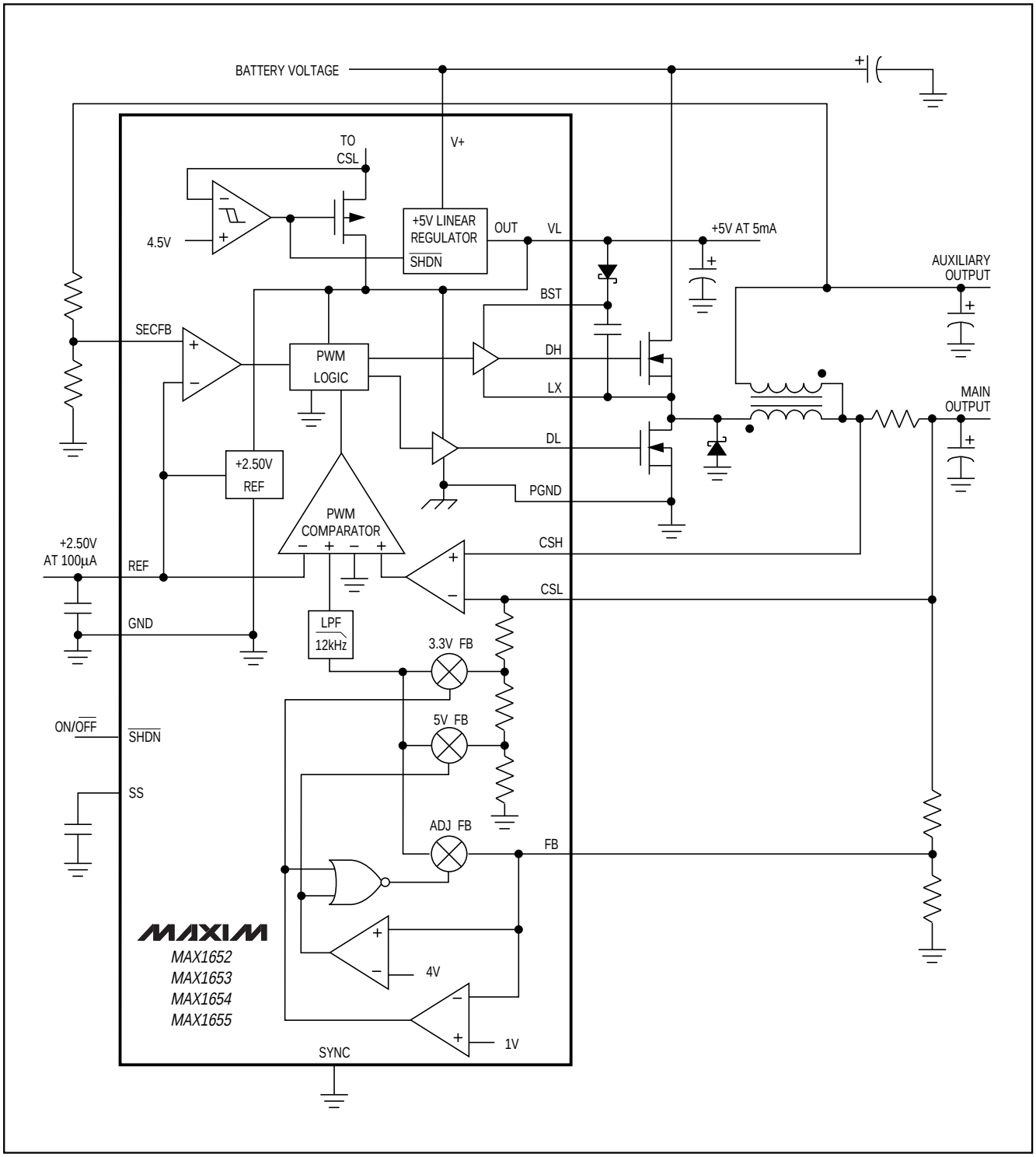


Figure 2. MAX1652–MAX1655 Functional Diagram

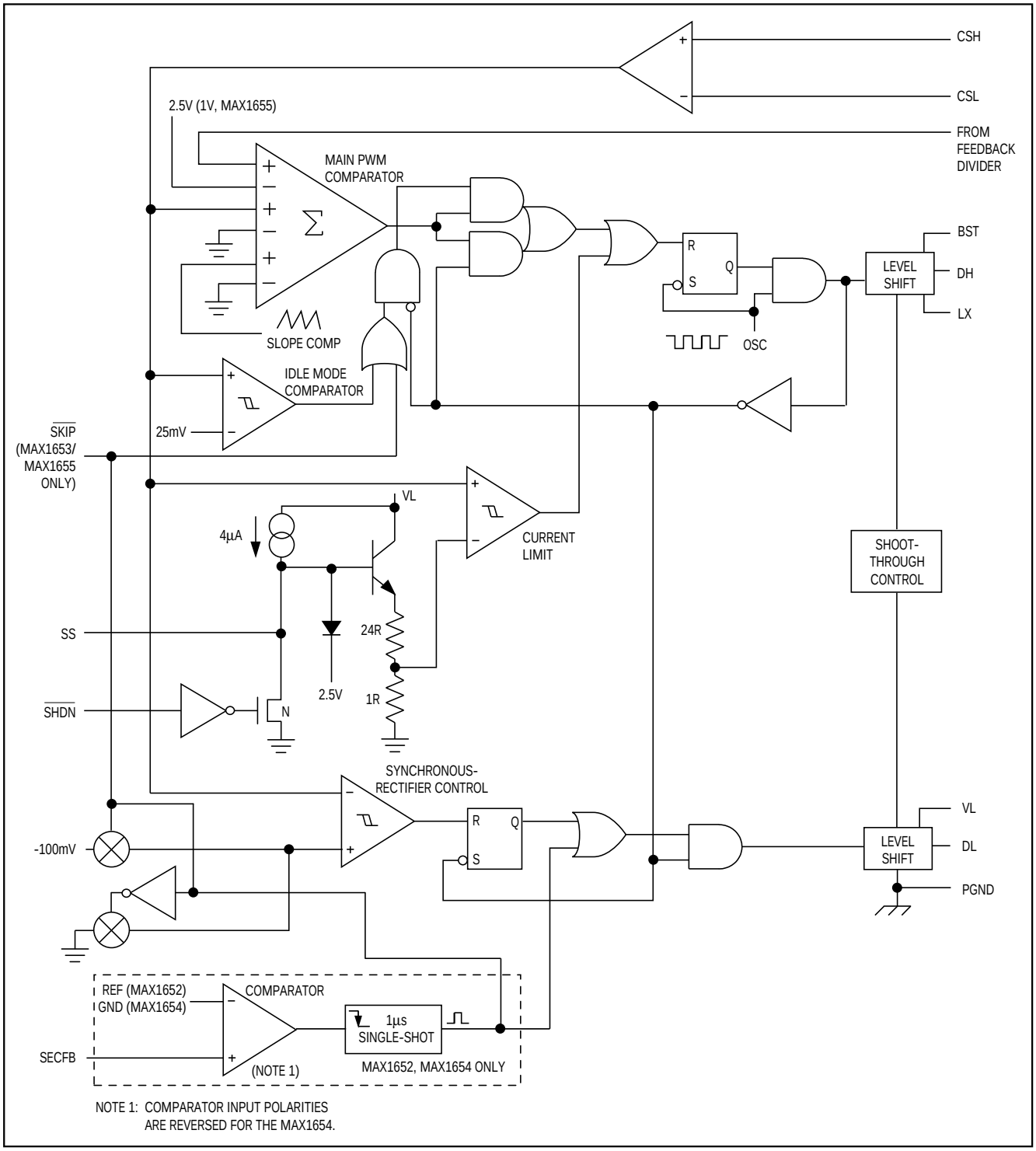


Figure 3. PWM Controller Detailed Block Diagram

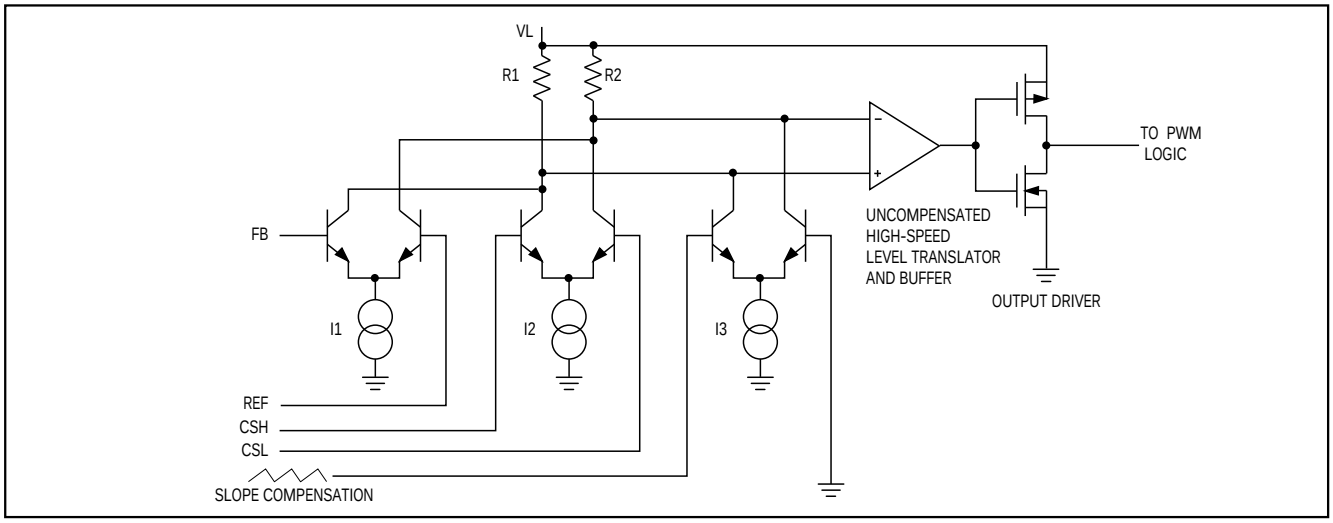


Figure 4. Main PWM Comparator Block Diagram

In discontinuous (light-load) mode, the synchronous switch is turned off as the inductor current falls through zero. The synchronous rectifier works under all operating conditions, including idle mode. The synchronous-switch timing is further controlled by the secondary feedback (SECFB) signal in order to improve multiple-output cross-regulation (see *Secondary Feedback-Regulation Loop* section).

Internal VL and REF Supplies

An internal regulator produces the 5V supply (VL) that powers the PWM controller, logic, reference, and other blocks. This +5V low-dropout linear regulator can supply up to 5mA for external loads, with a reserve of 20mA for gate-drive power. Bypass VL to GND with 4.7µF. **Important**: VL must not be allowed to exceed 5.5V. Measure VL with the main output fully loaded. If VL is being pumped up above 5.5V, the probable cause is either excessive boost-diode capacitance or excessive ripple at V+. Use only small-signal diodes for D2 (10mA to 100mA Schottky or 1N4148 are preferred) and bypass V+ to PGND with 0.1µF directly at the package pins.

The 2.5V reference (REF) is accurate to ±1.6% over temperature, making REF useful as a precision system reference. Bypass REF to GND with 0.33µF minimum. REF can supply up to 1mA for external loads. However, if tight-accuracy specs for either V_{OUT} or REF are essential, avoid loading REF with more than 100µA. Loading REF reduces the main output voltage slightly, according to the reference-voltage load regulation error. In MAX1654 applications, ensure that the SECFB divider doesn't load REF heavily.

When the main output voltage is above 4.5V, an internal P-channel MOSFET switch connects CSL to VL while simultaneously shutting down the VL linear regulator. This action bootstraps the IC, powering the internal circuitry from the output voltage, rather than through a linear regulator from the battery. Bootstrapping reduces power dissipation caused by gate-charge and quiescent losses by providing that power from a 90%-efficient switch-mode source, rather than from a less efficient linear regulator.

It's often possible to achieve a bootstrap-like effect, even for circuits that are set to V_{OUT} < 4.5V, by powering VL from an external-system +5V supply. To achieve this pseudo-bootstrap, add a Schottky diode between the external +5V source and VL, with the cathode to the VL side. This circuit provides a 1% to 2% efficiency boost and also extends the minimum battery input to less than 4V. The external source must be in the range of 4.8V to 5.5V.

Boost High-Side Gate-Driver Supply (BST Pin)

Gate-drive voltage for the high-side N-channel switch is generated by a flying-capacitor boost circuit as shown in Figure 5. The capacitor is alternately charged from the VL supply and placed in parallel with the high-side MOSFET's gate-source terminals.

On start-up, the synchronous rectifier (low-side MOSFET) forces LX to 0V and charges the BST capacitor to 5V. On the second half-cycle, the PWM turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary enhancement voltage to turn on the high-side switch,

High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

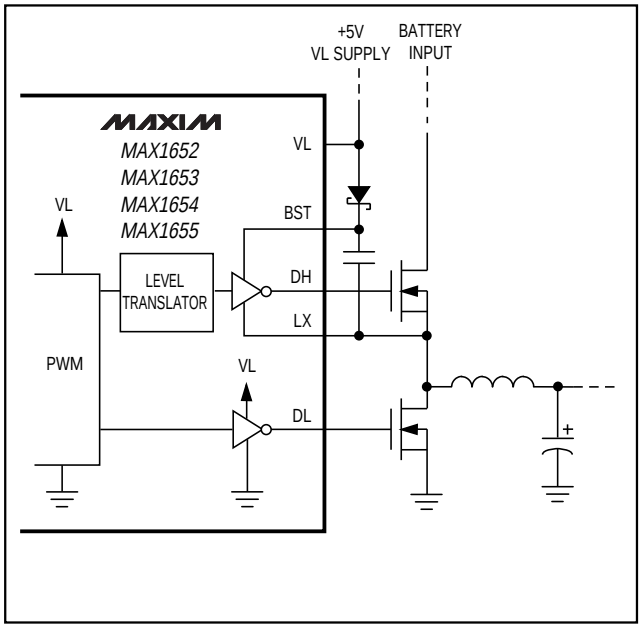


Figure 5. Boost Supply for Gate Drivers

an action that "boosts" the 5V gate-drive signal above the battery voltage.

Ringing seen at the high-side MOSFET gate (DH) in discontinuous-conduction mode (light loads) is a natural operating condition caused by the residual energy in the tank circuit formed by the inductor and stray capacitance at the switching node LX. The gate-driver negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive output.

Current-Limiting and Current-Sense Inputs (CSH and CSL)

The current-limit circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL exceeds 100mV. This limiting is effective for both current flow directions, putting the threshold limit at ±100mV. The tolerance on the positive current limit is ±20%, so the external low-value sense resistor must be sized for 80mV/R1 to guarantee enough load capability, while components must be designed to withstand continuous current stresses of 120mV/R1.

For breadboarding purposes or very-high-current applications, it may be useful to wire the current-sense inputs with a twisted pair rather than PC traces.

Oscillator Frequency and Synchronization (SYNC Pin)

The SYNC input controls the oscillator frequency. Connecting SYNC to GND or to VL selects 150kHz operation; connecting SYNC to REF selects 300kHz. SYNC can also be used to synchronize with an external 5V CMOS clock generator. SYNC has a guaranteed 190kHz to 340kHz capture range.

300kHz operation optimizes the application circuit for component size and cost. 150kHz operation provides increased efficiency and improved low-duty factor operation (see *Dropout Operation* section).

Dropout Operation

Dropout (low input-output differential operation) is enhanced by stretching the clock pulse width to increase the maximum duty factor. The algorithm follows: if the output voltage (V_{OUT}) drops out of regulation without the current limit having been reached, the controller skips an off-time period (extending the on-time). At the end of the cycle, if the output is still out of regulation, another off-time period is skipped. This action can continue until three off-time periods are skipped, effectively dividing the clock frequency by as much as four.

The typical PWM minimum off-time is 300ns, regardless of the operating frequency. Lowering the operating frequency raises the maximum duty factor above 98%.

Low-Noise Mode ($\overline{SKIP}$ Pin)

The low-noise mode ($\overline{SKIP}$ = high) is useful for minimizing RF and audio interference in noise-sensitive applications such as audio-equipped systems, cellular phones, RF communicating computers, and electromagnetic pen-entry systems. See the summary of operating modes in Table 3. $\overline{SKIP}$ can be driven from an external logic signal.

The MAX1653 and MAX1655 can reduce interference due to switching noise by ensuring a constant switching frequency regardless of load and line conditions, thus concentrating the emissions at a known frequency outside the system audio or IF bands. Choose an oscillator frequency where harmonics of the switching frequency don't overlap a sensitive frequency band. If necessary, synchronize the oscillator to a tight-tolerance external clock generator.

The low-noise mode ($\overline{SKIP}$ = high) forces two changes upon the PWM controller. First, it ensures fixed-frequency operation by disabling the minimum-current comparator and ensuring that the PWM latch is set at the beginning of each cycle, even if the output is in regulation. Second, it ensures continuous inductor current

Table 3. Operating-Mode Truth Table

$\overline{SHDN}$	$\overline{SKIP}$	LOAD CURRENT	MODE NAME	DESCRIPTION
Low	X	X	Shutdown	All circuit blocks turned off; supply current = 3µA typ
High	Low	Low, <10%	Idle	Pulse-skipping; supply current = 300µA typ at V_{IN} = 10V; discontinuous inductor current
High	Low	Medium, <30%	Idle	Pulse-skipping; continuous inductor current
High	Low	High, >30%	PWM	Constant-frequency PWM; continuous inductor current
High	High	X	Low Noise* (PWM)	Constant-frequency PWM regardless of load; continuous inductor current even at no load

** MAX1652/MAX1654 have no $\overline{SKIP}$ pin and therefore can't go into low-noise mode.*

X = Don't care

flow, and thereby suppresses discontinuous-mode inductor ringing by changing the reverse current-limit detection threshold from 0 to -100mV, allowing the inductor current to reverse at very light loads.

In most applications, $\overline{SKIP}$ should be tied to GND in order to minimize quiescent supply current. Supply current with $\overline{SKIP}$ high is typically 10mA to 20mA, depending on external MOSFET gate capacitance and switching losses.

Forced continuous conduction via $\overline{SKIP}$ can improve cross regulation of transformer-coupled multiple-output supplies. This second function of the $\overline{SKIP}$ pin produces a result that is similar to the method of adding secondary regulation via the SECFB feedback pin, but with much higher quiescent supply current. Still, improving cross regulation by enabling $\overline{SKIP}$ instead of building in SECFB feedback can be useful in noise-sensitive applications, since SECFB and $\overline{SKIP}$ are mutually exclusive pins/functions in the MAX1652 family.

Adjustable-Output Feedback (Dual-Mode FB Pin)

The MAX1652–MAX1655 family has both fixed and adjustable output voltage modes. For fixed mode, connect FB to GND for a 3.3V output and to V_L for a 5V output. Adjusting the main output voltage with external resistors is easy for any of the devices in this family, via the circuit of Figure 6. The feedback voltage is nominally 2.5 for all family members except the MAX1655, which has a nominal FB voltage of 1V. The output voltage (given by the formula in Figure 6) should be set approximately 2% high in order to make up for the MAX1652's load-regulation error. For example, if designing for a 3.0V output, use a resistor ratio that results in a nominal output voltage of 3.06V. This slight offsetting gives the best possible accuracy. Recommended normal values for R5 range from 5kΩ to 100kΩ.

Remote sensing of the output voltage, while not possible in fixed-output mode due to the combined nature of the voltage- and current-sense input (CSL), is easy to achieve in adjustable mode by using the top of the external resistor divider as the remote sense point.

Duty-Factor Limitations for Low V_{OUT}/V_{IN} Ratios

The MAX1652/MAX1653/MAX1654's output voltage is adjustable down to 2.5V and the MAX1655's output is adjustable as low as 1V. However, the minimum duty factor may limit the choice of operating frequency, high input voltage, and low output voltage.

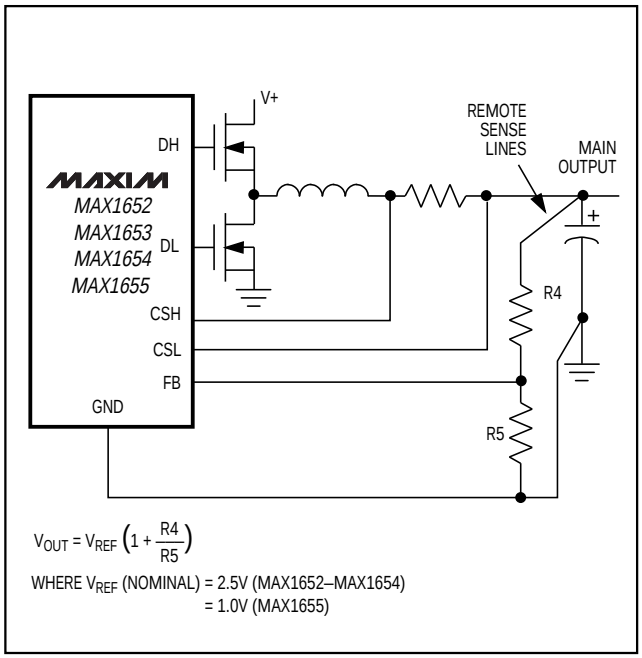


Figure 6. Adjusting the Main Output Voltage

High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

With high input voltages, the required duty factor is approximately (V_{OUT} + V_{Q2})/ V_{IN}, where V_{Q2} is the voltage drop across the synchronous rectifier. The MAX1652's minimum duty factor is determined by delays through the feedback network, error comparator, internal logic gate drivers, and the external MOSFETs, which typically total 400ns. This delay is about 12% of the switching period at 300kHz and 6% at 150kHz, limiting the typical minimum duty factor to these values.

Even if the circuit can not attain the required duty factor dictated by the input and output voltages, the output voltage will remain in regulation. However, there may be intermittent or continuous half-frequency operation. This can cause a factor-of-two increase in output voltage ripple and current ripple, which will increase noise and reduce efficiency. Choose 150kHz operation for high-input-voltage/low-output-voltage circuits.

Secondary Feedback-Regulation Loop (SECFB Pin)

A flyback winding control loop regulates a secondary winding output (MAX1652/MAX1654 only), improving cross-regulation when the primary is lightly loaded or when there is a low input-output differential voltage. If SECFB crosses its regulation threshold, a 1µs one-shot is triggered that extends the low-side switch's on-time beyond the point where the inductor current crosses zero (in discontinuous mode). This causes the inductor (primary) current to reverse, which in turn pulls current out of the output filter capacitor and causes the flyback transformer to operate in the forward mode. The low impedance presented by the transformer secondary in the forward mode dumps current into the secondary output, charging up the secondary capacitor and bringing SECFB back into regulation. The SECFB feedback loop does not improve secondary output accuracy in normal flyback mode, where the main (primary) output is heavily loaded. In this mode, secondary output accuracy is determined (as usual) by the secondary rectifier drop, turns ratio, and accuracy of the main output voltage. Hence, a linear post-regulator may still be needed in order to meet tight output accuracy specifications.

The secondary output voltage-regulation point is determined by an external resistor-divider at SECFB. For negative output voltages, the SECFB comparator is referenced to GND (MAX1654); for positive output voltages, SECFB regulates at the 2.50V reference (MAX1652). As a result, output resistor-divider connections and design equations for the two device types differ slightly (Figure 7). Ordinarily, the secondary regulation point is set 5% to 10% below the voltage normally produced by the flyback effect. For example, if the

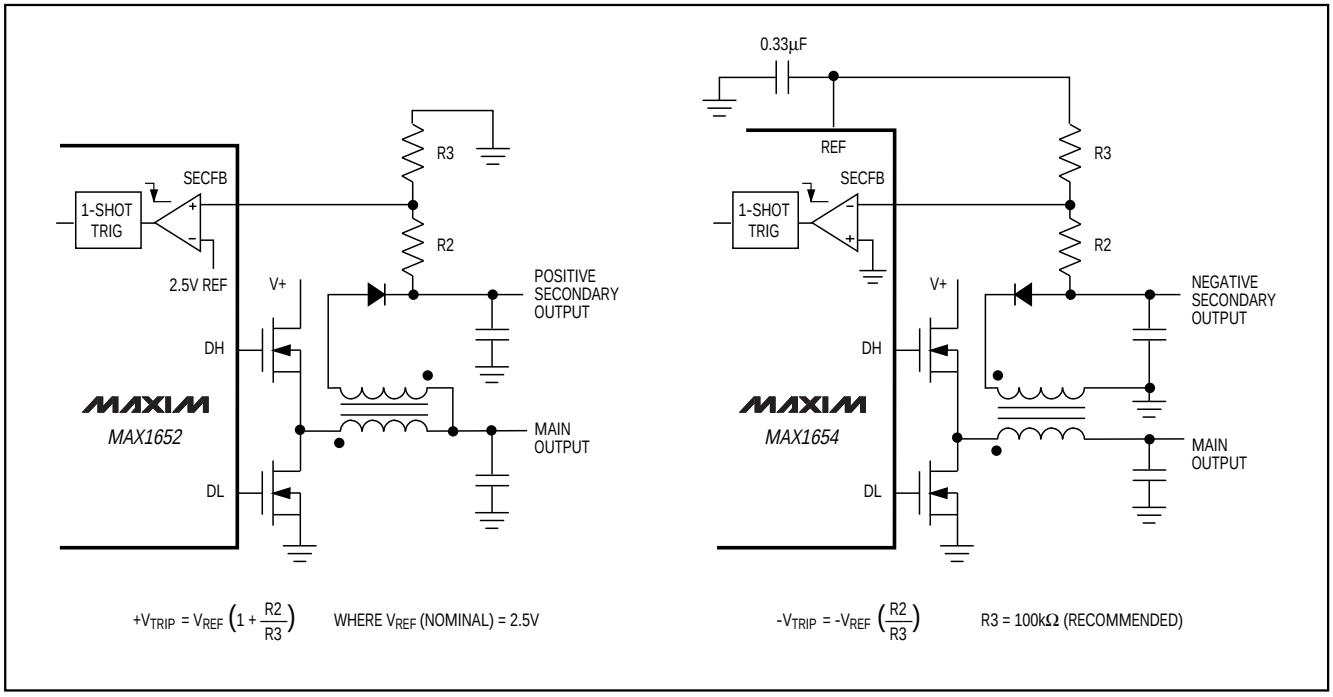


Figure 7. Secondary-Output Feedback Dividers

output voltage as determined by the turns ratio is +15V, the feedback resistor ratio should be set to produce about +13.5V; otherwise, the SECFB one-shot might be triggered unintentionally, causing an unnecessary increase in supply current and output noise. In negative-output (MAX1654) applications, the resistor-divider acts as a load on the internal reference, which in turn can cause errors at the main output. Avoid overloading REF (see the Reference Load-Regulation Error vs. Load Current graph in the *Typical Operating Characteristics*). 100kΩ is a good value for R3 in MAX1654 circuits.

Output current on secondary winding applications is limited at low input voltages. See the MAX1652 Maximum Secondary Output Current vs. Supply Voltage graph in the Typical Operating Characteristics for data from the application circuit of Figure 8.

Soft-Start Circuit (SS)

Soft-start allows a gradual increase of the internal current-limit level at start-up for the purpose of reducing input surge currents, and perhaps for power-supply sequencing. In shutdown mode, the soft-start circuit holds the SS capacitor discharged to ground. When $\overline{SHDN}$ goes high, a 4µA current source charges the SS capacitor up to 3.2V. The resulting linear ramp waveform causes the internal current-limit level to increase proportionally from 0 to 100mV. The main output capacitor thus charges up relatively slowly, depending on the SS capacitor value. The exact time of the output rise depends on output capacitance and load current and is typically 1ms per nanofarad of soft-start capacitance. With no SS capacitor connected, maximum current limit is reached within 10µs.

Shutdown

Shutdown mode ($\overline{SHDN}$ = 0V) reduces the V+ supply current to typically 3µA. In this mode, the reference and VL are inactive. $\overline{SHDN}$ is a logic-level input, but it can be safely driven to the full V+ range. Connect $\overline{SHDN}$ to V+ for automatic start-up. Do not allow slow transitions (slower than 0.02V/µs) on $\overline{SHDN}$.

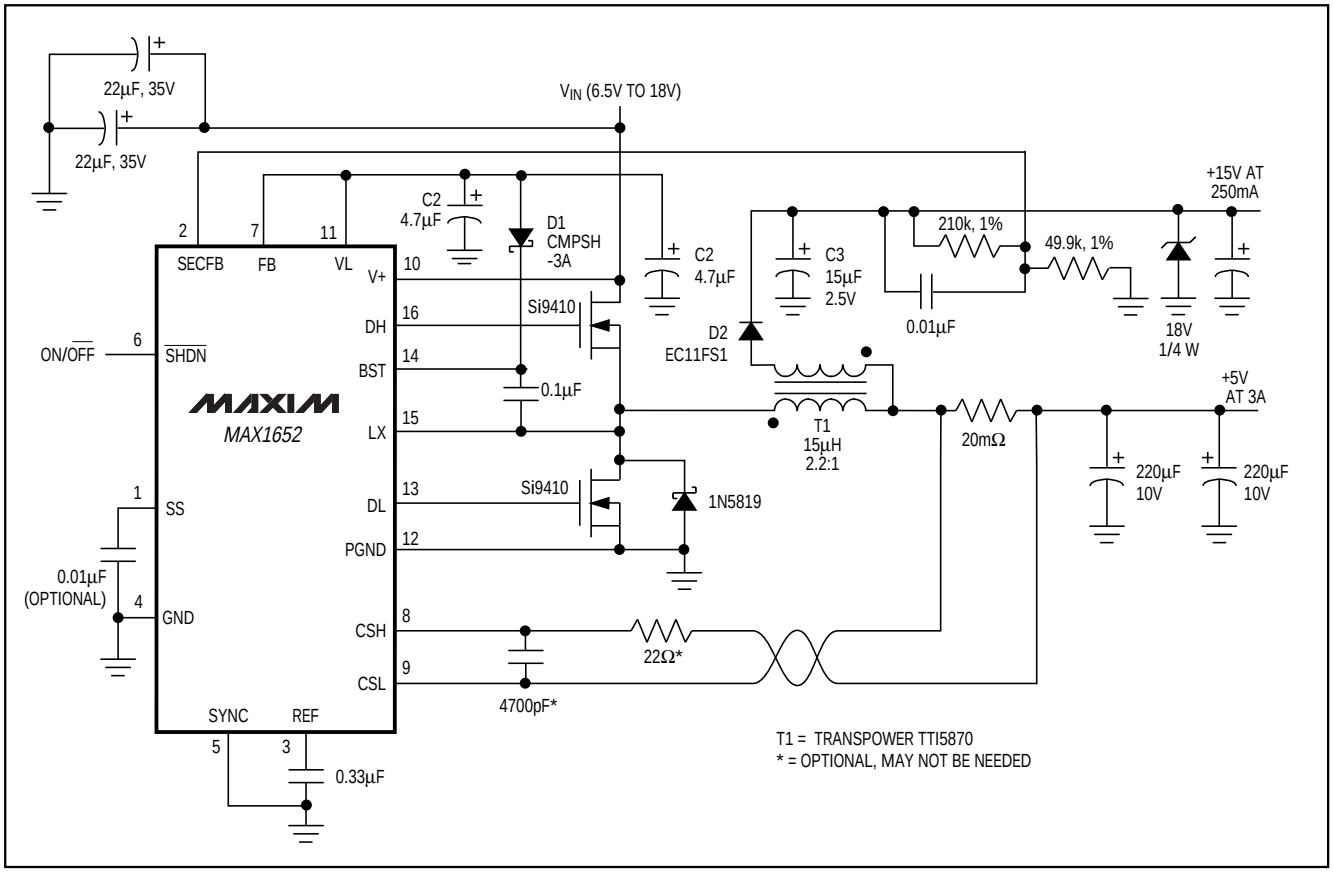


Figure 8. 5V/15V Dual-Output Application Circuit (MAX1652)

Design Procedure

The predesigned standard application circuits (Figure 1 and Table 1) contain ready-to-use solutions for common applications. Use the following design procedure to optimize the basic schematic for different voltage or current requirements. Before beginning a design, firmly establish the following:

$V_{IN(MAX)}$, the maximum input (battery) voltage. This value should include the worst-case conditions, such as no-load operation when a battery charger or AC adapter is connected but no battery is installed. $V_{IN(MAX)}$ must not exceed 30V. This 30V upper limit is determined by the breakdown voltage of the BST floating gate driver to GND (36V absolute maximum).

$V_{IN(MIN)}$, the minimum input (battery) voltage. This should be at full-load under the lowest battery conditions. If $V_{IN(MIN)}$ is less than 4.5V, a special circuit must be used to externally hold up VL above 4.8V. If the minimum input-output difference is less than 1V, the filter capacitance required to maintain good AC load regulation increases.

Inductor Value

The exact inductor value isn't critical and can be adjusted freely in order to make trade-offs among size, cost, and efficiency. Although lower inductor values will minimize size and cost, they will also reduce efficiency due to higher peak currents. To permit use of the physically smallest inductor, lower the inductance until the circuit is operating at the border between continuous and discontinuous modes. Reducing the inductor value even further, below this crossover point, results in discontinuous-conduction operation even at full load. This helps reduce output filter capacitance requirements but causes the core energy storage requirements to increase again. On the other hand, higher inductor values will increase efficiency, but at some point resistive losses due to extra turns of wire will exceed the benefit gained from lower AC current levels. Also, high inductor values affect load-transient response; see the V_{SAG} equation in the *Low-Voltage Operation* section.

The following equations are given for continuous-conduction operation since the MAX1652 family is mainly intended for high-efficiency, battery-powered applications. See Appendix A in Maxim's *Battery Management and DC-DC Converter Circuit Collection* for crossover point and discontinuous-mode equations. Discontinuous conduction doesn't affect normal Idle Mode operation.

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher value of LIR allows smaller inductance, but results in higher losses and ripple. A good compromise between size and losses is found at a 30% ripple current to load current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times higher than the DC load current.

$$L = \frac{V_{OUT}\,(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{OUT} \times LIR}$$

where: f = switching frequency, normally 150kHz or 300kHz
I_{OUT} = maximum DC load current
LIR = ratio of AC to DC inductor current, typically 0.3

The peak inductor current at full load is 1.15 x I_{OUT} if the above equation is used; otherwise, the peak current can be calculated by:

$$I_{PEAK} = I_{LOAD} + \frac{V_{OUT}\,(V_{IN(MAX)} - V_{OUT})}{2 \times f \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance is a key parameter for efficiency performance and must be ruthlessly minimized, preferably to less than 25mΩ at I_{OUT} = 3A. If a standard off-the-shelf inductor is not available, choose a core with an LI^2 rating greater than L x I_{PEAK}^2 and wind it with the largest diameter wire that fits the winding area. For 300kHz applications, ferrite core material is strongly preferred; for 150kHz applications, Kool-mu (aluminum alloy) and even powdered iron can be acceptable. If light-load efficiency is unimportant (in desktop 5V-to-3V applications, for example) then low-permeability iron-powder cores may be acceptable, even at 300kHz. For high-current applications, shielded core geometries (such as toroidal or pot core) help keep noise, EMI, and switching-waveform jitter low.

Current-Sense Resistor Value

The current-sense resistor value is calculated according to the worst-case, low-current-limit threshold voltage (from the *Electrical Characteristics* table) and the peak inductor current. The continuous-mode peak inductor-current calculations that follow are also useful for sizing the switches and specifying the inductor-current saturation ratings. In order to simplify the calculation, I_{LOAD} may be used in place of I_{PEAK} if the inductor value has been set for LIR = 0.3 or less (high inductor values) and 300kHz operation is selected. Low-inductance resistors, such as surface-mount metal-film resistors, are preferred.

$$R_{SENSE} = \frac{80mV}{I_{PEAK}}$$

Input Capacitor Value

Place a small ceramic capacitor (0.1µF) between V+ and GND, close to the device. Also, connect a low-ESR bulk capacitor directly to the drain of the high-side MOSFET. Select the bulk input filter capacitor according to input ripple-current requirements and voltage rating, rather than capacitor value. Electrolytic capacitors that have low enough effective series resistance (ESR) to meet the ripple-current requirement invariably have more than adequate capacitance values. Ceramic capacitors or low-ESR aluminum-electrolytic capacitors such as Sanyo OS-CON or Nichicon PL are preferred. Tantalum types are also acceptable but may be less tolerant of high input surge currents. RMS input ripple current is determined by the input voltage and load current, with the worst possible case occurring at $V_{IN} = 2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT\ (VIN\ -\ VOUT)}}}{V_{IN}}$$

$$I_{RMS} = I_{LOAD} / 2 \text{ when } V_{IN} \text{ is } 2 \times V_{OUT}$$

Output Filter Capacitor Value

The output filter capacitor values are determined by the ESR, capacitance, and voltage rating requirements. Electrolytic and tantalum capacitors are generally chosen by voltage rating and ESR specifications, as they will generally have more output capacitance than is required for AC stability. Use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. To ensure stability, the capacitor must meet *both* minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > \frac{V_{REF}\ (1 + V_{OUT} / V_{IN(MIN)})}{V_{OUT} \times R_{SENSE} \times f}$$

$$R_{ESR} < \frac{R_{SENSE} \times V_{OUT}}{V_{REF}}$$

(can be multiplied by 1.5, see note below)

These equations are “worst-case” with 45 degrees of phase margin to ensure jitter-free fixed-frequency operation and provide a nicely damped output response for zero to full-load step changes. Some cost-conscious designers may wish to bend these rules by using less expensive (lower quality) capacitors, particularly if the load lacks large step changes. This practice is tolerable if some bench testing over temperature is done to verify acceptable noise and transient response.

There is no well-defined boundary between stable and unstable operation. As phase margin is reduced, the first symptom is a bit of timing jitter, which shows up as blurred edges in the switching waveforms where the scope won’t quite sync up. Technically speaking, this (usually) harmless jitter is unstable operation, since the switching frequency is now nonconstant. As the capacitor quality is reduced, the jitter becomes more pronounced and the load-transient output voltage waveform starts looking ragged at the edges. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the allowable output voltage tolerance. Note that even with zero phase margin and gross instability present, the output voltage noise never gets much worse than $I_{PEAK} \times R_{ESR}$ (under constant loads, at least).

Note: Designers of RF communicators or other noise-sensitive analog equipment should be conservative and stick to the ESR guidelines. Designers of notebook computers and similar commercial-temperature-range digital systems can multiply the R_{ESR} value by a factor of 1.5 without hurting stability or transient response.

The output voltage ripple is usually dominated by the ESR of the filter capacitor and can be approximated as $I_{RIPPLE} \times R_{ESR}$. There is also a capacitive term, so the full equation for ripple in the continuous mode is $V_{NOISE(p-p)} = I_{RIPPLE} \times [R_{ESR} + 1 / (8 \times f \times C_{OUT})]$. In Idle Mode, the inductor current becomes discontinuous with high peaks and widely spaced pulses, so the noise can actually be higher at light load compared to full load. In Idle Mode, the output ripple can be calculated as:

$$V_{NOISE(p-p)} = \frac{0.025 \times R_{ESR}}{R_{SENSE}} + \frac{(0.025)^2 \times L \times [1 / V_{OUT} + 1 / (V_{IN} - V_{OUT})]}{(R_{SENSE})^2 \times C_{OUT}}$$

Transformer Design (MAX1652/MAX1654 Only)

Buck-plus-flyback applications, sometimes called “coupled-inductor” topologies, use a transformer to generate multiple output voltages. The basic electrical design is a simple task of calculating turns ratios and adding the power delivered to the secondary in order to calculate the current-sense resistor and primary inductance. However, extremes of low input-output differentials, widely different output loading levels, and high turns ratios can complicate the design due to parasitic transformer parameters such as interwinding capacitance, secondary resistance, and leakage inductance. For examples of what is possible with real-world transformers, see the graphs of Maximum Secondary Current vs. Input Voltage in the *Typical Operating Characteristics.*

Power from the main and secondary outputs is lumped together to obtain an equivalent current referred to the main output voltage (see *Inductor Value* section for definitions of parameters). Set the value of the current-sense resistor at 80mV / I_{TOTAL}.

P_{TOTAL} = the sum of the output power from all outputs

$I_{TOTAL} = P_{TOTAL} / V_{OUT}$ = the equivalent output current referred to V_{OUT}

$$L(primary) = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{TOTAL} \times LIR}$$

$$Turns\ Ratio\ N = \frac{V_{SEC} + V_{FWD}}{V_{OUT(MIN)} + V_{RECT} + V_{SENSE}}$$

where: V_{SEC} is the minimum required rectified secondary-output voltage

V_{FWD} is the forward drop across the secondary rectifier

$V_{OUT(MIN)}$ is the *minimum* value of the main output voltage (from the *Electrical Characteristics*)

V_{RECT} is the on-state voltage drop across the synchronous-rectifier MOSFET

V_{SENSE} is the voltage drop across the sense resistor

In positive-output (MAX1652) applications, the transformer secondary return is often referred to the main output voltage rather than to ground in order to reduce the needed turns ratio. In this case, the main output voltage must first be subtracted from the secondary voltage to obtain V_{SEC}.

Selecting Other Components

MOSFET Switches

The two high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. Lower gate threshold specs are better (i.e., 2V max rather than 3V max). Drain-source breakdown voltage ratings must at least equal the maximum input voltage, preferably with a 20% derating factor. The best MOSFETs will have the lowest on-resistance per nanocoulomb of gate charge. Multiplying $R_{DS(ON)} \times Q_G$ provides a meaningful figure by which to compare various MOSFETs. Newer MOSFET process technologies with dense cell structures generally give the best performance. The internal gate drivers can tolerate more than 100nC total gate charge, but 70nC is a more practical upper limit to maintain best switching times.

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R losses are distributed between Q1 and Q2 according to duty factor (see the equations below). Switching losses affect the upper MOSFET only, since the Schottky rectifier clamps the switching node before the synchronous rectifier turns on. Gate-charge losses are dissipated by the driver and don't heat the MOSFET. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. The worst-case dissipation for the high-side MOSFET occurs at the minimum battery voltage, and the worst-case for the low-side MOSFET occurs at the maximum battery voltage.

$$PD\ (upper\ FET) = I_{LOAD}^2 \times R_{DS(ON)} \times DUTY + V_{IN} \times I_{LOAD} \times f \times \left(\frac{V_{IN} \times C_{RSS}}{I_{GATE}} + 20ns\right)$$

$$PD\ (lower\ FET) = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - DUTY)$$

$$DUTY = (V_{OUT} + V_{Q2}) / (V_{IN} - V_{Q1} + V_{Q2})$$

where the on-state voltage drop $V_{Q\_} = I_{LOAD} \times R_{DS(ON)}$

C_{RSS} = MOSFET reverse transfer capacitance

I_{GATE} = DH driver peak output current capability (1A typically)

20ns = DH driver inherent rise/fall time

Under output short circuit, the synchronous-rectifier MOSFET suffers extra stress and may need to be oversized if a continuous DC short circuit must be tolerated. During short circuit, Q2's duty factor can increase to greater than 0.9 according to:

$$Q2\ DUTY\ (short\ circuit) = 1 - [V_{Q2} / (V_{IN(MAX)} - V_{Q1} + V_{Q2})]$$

where the on-state voltage drop $V_Q = (120mV / R_{SENSE}) \times R_{DS(ON)}$.

Rectifier Diode D1

Rectifier D1 is a clamp that catches the negative inductor swing during the 60ns dead time between turning off the high-side MOSFET and turning on the low-side. D1 must be a Schottky type in order to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit D1 and let the body diode clamp the negative inductor swing, but efficiency will drop one or two percent as a result. Use an MBR0530 (500mA rated) type for loads up to 1.5A, a 1N5819 type for loads up to 3A, or a 1N5822 type for loads up to 10A. D1's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor.

Boost-Supply Diode D2

A 10mA to 100mA Schottky diode or signal diode such as a 1N4148 works well for D2 in most applications. If the input voltage can go below 6V, use a Schottky diode for slightly improved efficiency and dropout characteristics. Don't use large power diodes such as 1N5817 or 1N4001, since high junction capacitance can cause VL to be pumped up to excessive voltages.

Rectifier Diode D3 (Transformer Secondary Diode)

The secondary diode in coupled-inductor applications must withstand high flyback voltages greater than 60V, which usually rules out most Schottky rectifiers. Common silicon rectifiers such as the 1N4001 are also prohibited, as they are far too slow. This often makes fast silicon rectifiers such as the MURS120 the only choice. The flyback voltage across the rectifier is related to the V_{IN}-V_{OUT} difference according to the transformer turns ratio:

$$V_{FLYBACK} = V_{SEC} + (V_{IN} - V_{OUT}) \times N$$

where: N is the transformer turns ratio SEC/PRI
V_{SEC} is the maximum secondary DC output voltage
V_{OUT} is the primary (main) output voltage

Subtract the main output voltage (V_{OUT}) from $V_{FLYBACK}$ in this equation if the secondary winding is returned to V_{OUT} and not to ground. The diode reverse breakdown rating must also accommodate any ringing due to leakage inductance. D3's current rating should be at least twice the DC load current on the secondary output.

Low-Voltage Operation

Low input voltages and low input-output differential voltages each require some extra care in the design. Low absolute input voltages can cause the VL linear regulator to enter dropout, and eventually shut itself off. Low input voltages relative to the output (low V_{IN}-V_{OUT} differential) can cause bad load regulation in multi-output flyback applications. See *Transformer Design* section. Finally, low V_{IN}-V_{OUT} differentials can also cause the output voltage to sag when the load current changes abruptly. The amplitude of the sag is a function of inductor value and maximum duty factor (D_{MAX} an *Electrical Characteristics* parameter, 98% guaranteed over temperature at f = 150kHz) as follows:

$$V_{SAG} = \frac{(I_{STEP})^2 \times L}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The cure for low-voltage sag is to increase the value of the output capacitor. For example, at V_{IN} = 5.5V, V_{OUT} = 5V, L = 10µH, f = 150kHz, a total capacitance of 660µF will prevent excessive sag. Note that only the capacitance requirement is increased and the ESR requirements don't change. Therefore, the added capacitance can be supplied by a low-cost bulk capacitor in parallel with the normal low-ESR capacitor. Table 4 summarizes low-voltage operational issues.

Table 4. Low-Voltage Troubleshooting

SYMPTOM	CONDITION	ROOT CAUSE	SOLUTION
Sag or droop in V_{OUT} under step load change	Low V_{IN}-V_{OUT} differential, <1V	Limited inductor-current slew rate per cycle.	Increase bulk output capacitance per formula above. Reduce inductor value.
Dropout voltage is too high (V_{OUT} follows V_{IN} as V_{IN} decreases)	Low V_{IN}-V_{OUT} differential, <0.5V	Maximum duty-cycle limits exceeded.	Reduce f to 150kHz. Reduce MOSFET on-resistance and coil DCR.
Unstable—jitters between two distinct duty factors	Low V_{IN}-V_{OUT} differential, <0.5V	Normal function of internal low-dropout circuitry.	Increase the minimum input voltage or ignore.
Secondary output won't support a load	Low V_{IN}-V_{OUT} differential, V_{IN} < 1.3 x V_{OUT}(main)	Not enough duty cycle left to initiate forward-mode operation. Small AC current in primary can't store energy for flyback operation.	Reduce f to 150kHz. Reduce secondary impedances—use Schottky if possible. Stack secondary winding on main output.
High supply current, poor efficiency	Low input voltage, <5V	VL linear regulator is going into dropout and isn't providing good gate-drive levels.	Use a small 20mA Schottky diode for boost diode D2. Supply VL from an external source.
Won't start under load or quits before battery is completely dead	Low input voltage, <4.5V	VL output is so low that it hits the VL UVLO threshold at 4.2V max.	Supply VL from an external source other than V_{BATT}, such as the system 5V supply.

High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

Applications Information

Heavy-Load Efficiency Considerations

The major efficiency loss mechanisms under loads (in the usual order of importance) are:

- P(I^2R), I^2R losses
- P(gate), gate-charge losses
- P(diode), diode-conduction losses
- P(tran), transition losses
- P(cap), capacitor ESR losses
- P(IC), losses due to the operating supply current of the IC

Inductor-core losses are fairly low at heavy loads because the inductor's AC current component is small. Therefore, they aren't accounted for in this analysis. Ferrite cores are preferred, especially at 300kHz, but powdered cores such as Kool-mu can work well.

$$\text{Efficiency} = P_{OUT} / P_{IN} \times 100\%$$
$$= P_{OUT} / (P_{OUT} + P_{TOTAL}) \times 100\%$$

$$P_{TOTAL} = P(I^2R) + P(\text{gate}) + P(\text{diode}) + P(\text{tran}) + P(\text{cap}) + P(\text{IC})$$

$$P(I^2R) = (I_{LOAD})^2 \times (R_{DC} + R_{DS(ON)} + R_{SENSE})$$

where R_{DC} is the DC resistance of the coil, $R_{DS(ON)}$ is the MOSFET on-resistance, and R_{SENSE} is the current-sense resistor value. The $R_{DS(ON)}$ term assumes identical MOSFETs for the high- and low-side switches because they time-share the inductor current. If the MOSFETs aren't identical, their losses can be estimated by averaging the losses according to duty factor.

$$P(\text{gate}) = \text{gate-driver loss} = qG \times f \times VL$$

where VL is the MAX1652 internal logic supply voltage (5V), and qG is the sum of the gate-charge values for low- and high-side switches. For matched MOSFETs, qG is twice the data sheet value of an individual MOSFET. If V_{OUT} is set to less than 4.5V, replace VL in this equation with V_{BATT}. In this case, efficiency can be improved by connecting VL to an efficient 5V source, such as the system +5V supply.

$$P(\text{diode}) = \text{diode conduction losses} = I_{LOAD} \times V_{FWD} \times t_D \times f$$

where t_D is the diode conduction time (120ns typ) and V_{FWD} is the forward voltage of the Schottky.

PD(tran) = transition loss =

$$V_{BATT} \times I_{LOAD} \times f \times \left(\frac{V_{BATT} \times C_{RSS}}{I_{GATE}} + 20ns\right)$$

where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data sheet parameter), I_{GATE} is the DH gate-driver peak output current (1A typ), and 20ns is the rise/fall time of the DH driver.

$$P(\text{cap}) = \text{input capacitor ESR loss} = (I_{RMS})^2 \times R_{ESR}$$

where I_{RMS} is the input ripple current as calculated in the *Input Capacitor Value* section of the *Design Procedure.*

Light-Load Efficiency Considerations

Under light loads, the PWM operates in discontinuous mode, where the inductor current discharges to zero at some point during the switching cycle. This causes the AC component of the inductor current to be high compared to the load current, which increases core losses and I^2R losses in the output filter capacitors. Obtain best light-load efficiency by using MOSFETs with moderate gate-charge levels and by using ferrite, MPP, or other low-loss core material. Avoid powdered iron cores; even Kool-mu (aluminum alloy) is not as good as ferrite.

PC Board Layout Considerations

Good PC board layout is *required* to achieve specified noise, efficiency, and stability performance. The PC board layout artist must be provided with explicit instructions, preferably a pencil sketch of the placement of power switching components and high-current routing. See the evaluation kit PC board layouts in the MAX1653, MAX796, and MAX797 EV kit manuals for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections (REF, SS, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide.

1) Place the high-power components (C1, C2, Q1, Q2, D1, L1, and R1) first, with their grounds adjacent.

   Priority 1: **Minimize current-sense resistor trace lengths** (see Figure 9).

   Priority 2: **Minimize ground trace lengths** in the high-current paths (discussed below).

   Priority 3: **Minimize other trace lengths** in the high-current paths. Use >5mm wide traces. C1 to Q1: 10mm max length. D1 anode to Q2: 5mm max length LX node (Q1 source, Q2 drain, D1 cathode, inductor): 15mm max length

   Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds (C1-, C2-, source of Q2, anode of D1, and PGND) are then connected to each other with a wide filled zone

of top-layer copper, so that they don't go through vias. The resulting top-layer "sub-ground-plane" is connected to the normal inner-layer ground plane at the output ground terminals. This ensures that the analog GND of the IC is sensing at the output terminals of the supply, without interference from IR drops and ground noise. Other high-current paths should also be minimized, **but focusing ruthlessly on short ground and current-sense connections eliminates about 90% of all PC board layout difficulties.** See the evaluation kit PC board layouts for examples.

2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and REF and SS capacitors). Placing the IC and analog components on the opposite side of the board from the power-switching node is desirable. Important: the IC must be no farther than 10mm from the current-sense resistor. Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm and route them away from CSH, CSL, REF, and SS.

3) Employ a single-point star ground where the input ground trace, power ground (subground plane), and normal ground plane all meet at the output ground terminal of the supply.

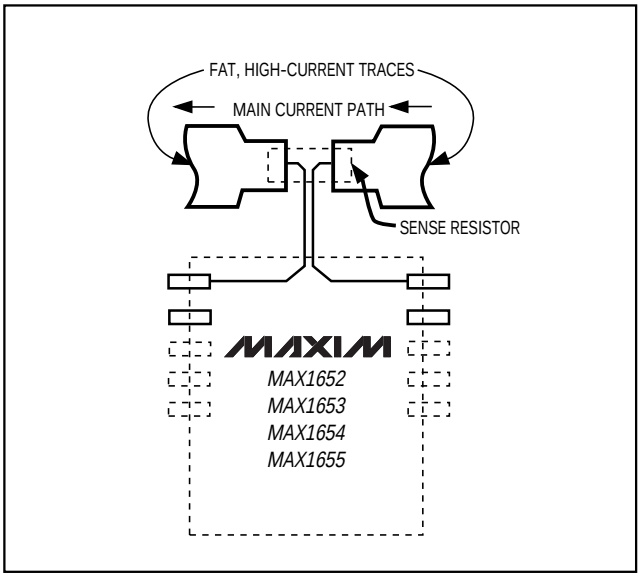
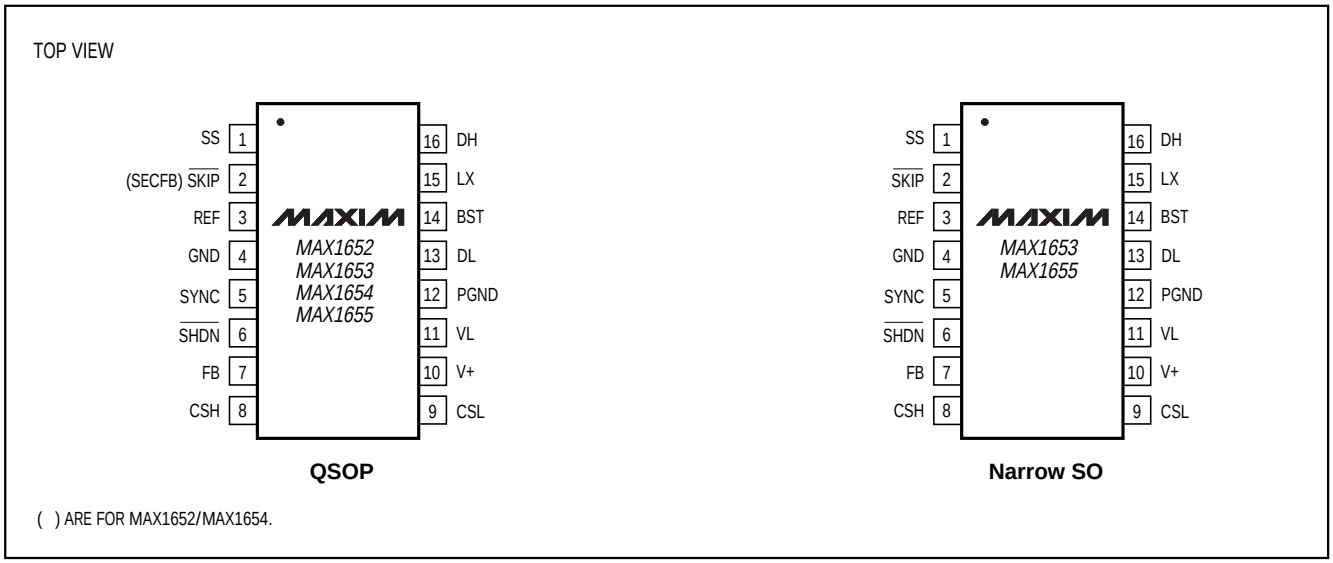


Figure 9. Kelvin Connections for the Current-Sense Resistor

Pin Configurations



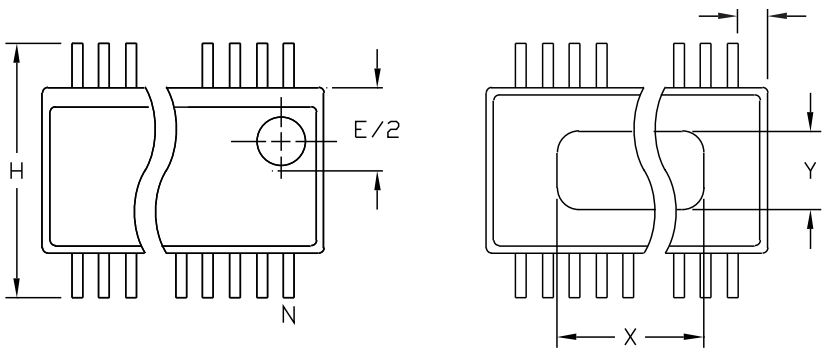
High-Efficiency, PWM, Step-Down DC-DC Controllers in 16-Pin QSOP

Chip Information

TRANSISTOR COUNT: 1990

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

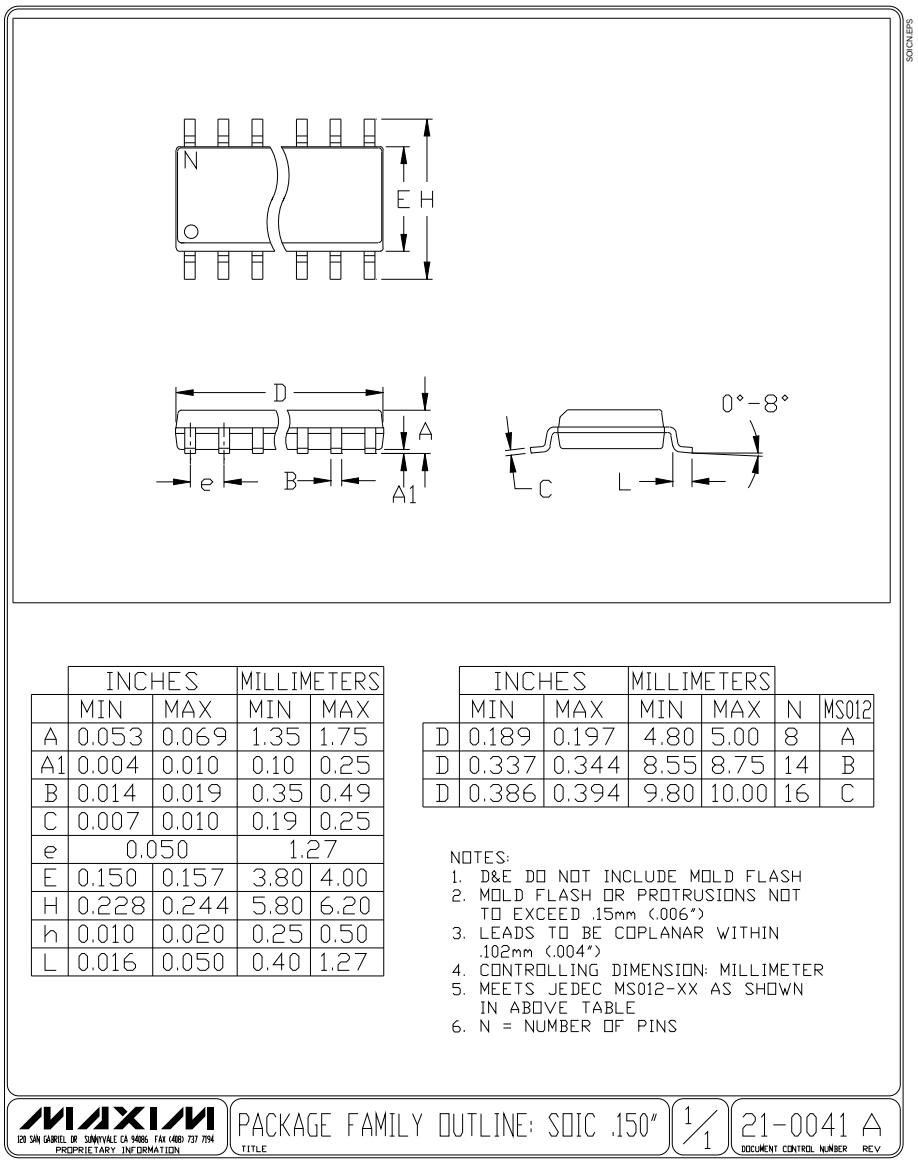
NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150" (TITLE) | 1/1 | 21-0041 A (DOCUMENT CONTROL NUMBER REV)

NOTES

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX1653EEE+ MAX1653ESE+ MAX1655EEE+ MAX1655ESE+ MAX1652EEE+ MAX1652EEE+T MAX1653EEE+T MAX1653ESE+T MAX1654EEE+ MAX1654EEE+T MAX1655EEE+T MAX1655ESE+T MAX1653ESE-T MAX1654EEE-T MAX1655ESE-T MAX1653ESE MAX1654EEE MAX1655EEE MAX1655ESE MAX1653EEE MAX1653EEE-T MAX1655EEE-T