

2N6107, 2N6109, 2N6111 (PNP), 2N6288, 2N6292 (NPN)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (Note 3) ($I_C = 100\text{ mA}$, $I_B = 0$) 2N6111, 2N6288 2N6109 2N6107, 2N6292	$V_{CE(sus)}$	30 50 70	– – –	Vdc
Collector Cutoff Current ($V_{CE} = 20\text{ Vdc}$, $I_B = 0$) 2N6111, 2N6288 ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) 2N6109 ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$) 2N6107, 2N6292	I_{CEO}	– – –	1.0 1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 40\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$) 2N6111, 2N6288 ($V_{CE} = 60\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$) 2N6109 ($V_{CE} = 80\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$) 2N6107, 2N6292 ($V_{CE} = 30\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) 2N6111, 2N6288 ($V_{CE} = 50\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) 2N6109 ($V_{CE} = 70\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) 2N6107, 2N6292	I_{CEX}	– – – – – –	100 100 100 2.0 2.0 2.0	μAdc mAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	1.0	mAdc

ON CHARACTERISTICS (Note 3)

DC Current Gain ($I_C = 2.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) 2N6107, 2N6292 ($I_C = 2.5\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) 2N6109 ($I_C = 3.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) 2N6111, 2N6288 ($I_C = 7.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$) All Devices	h_{FE}	30 30 30 2.3	150 150 150 –	–
Collector–Emitter Saturation Voltage ($I_C = 7.0\text{ Adc}$, $I_B = 3.0\text{ Adc}$)	$V_{CE(sat)}$	–	3.5	Vdc
Base–Emitter On Voltage ($I_C = 7.0\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	–	3.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product (Note 4) ($I_C = 500\text{ mA}$, $V_{CE} = 4.0\text{ Vdc}$, $f_{test} = 1.0\text{ MHz}$) 2N6288, 2N6292 2N6107, 2N6109, 2N6111	f_T	4.0 10	– –	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{ob}	–	250	pF
Small–Signal Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$, $f = 50\text{ kHz}$)	h_{fe}	20	–	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates JEDEC Registered Data.

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

4. $f_T = |h_{fe}| \cdot f_{test}$

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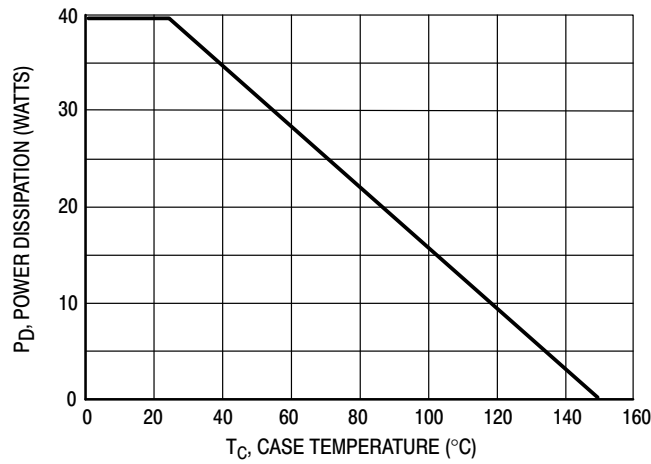


Figure 1. Power Derating

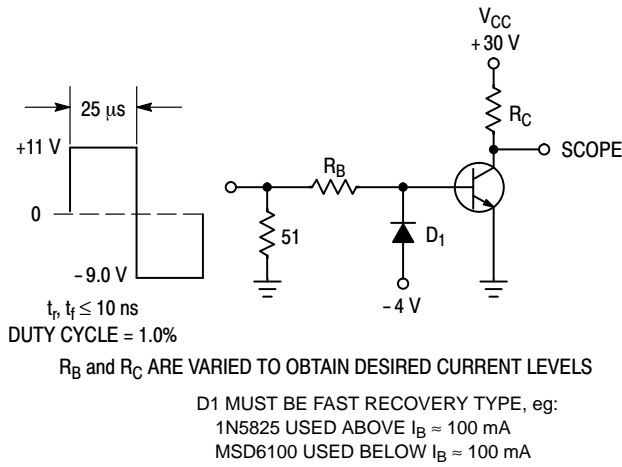


Figure 2. Switching Time Test Circuit

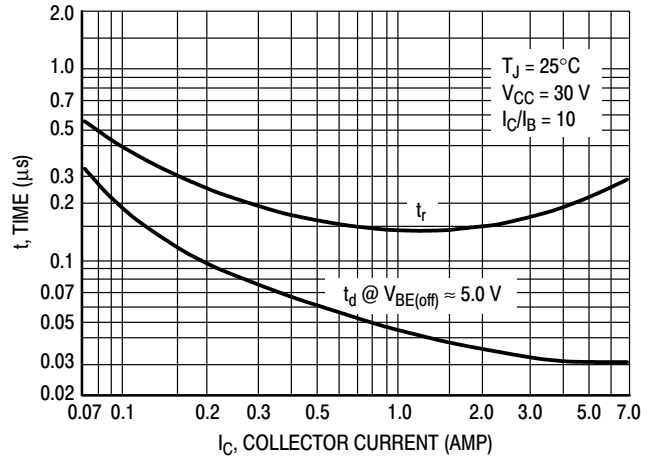


Figure 3. Turn-On Time

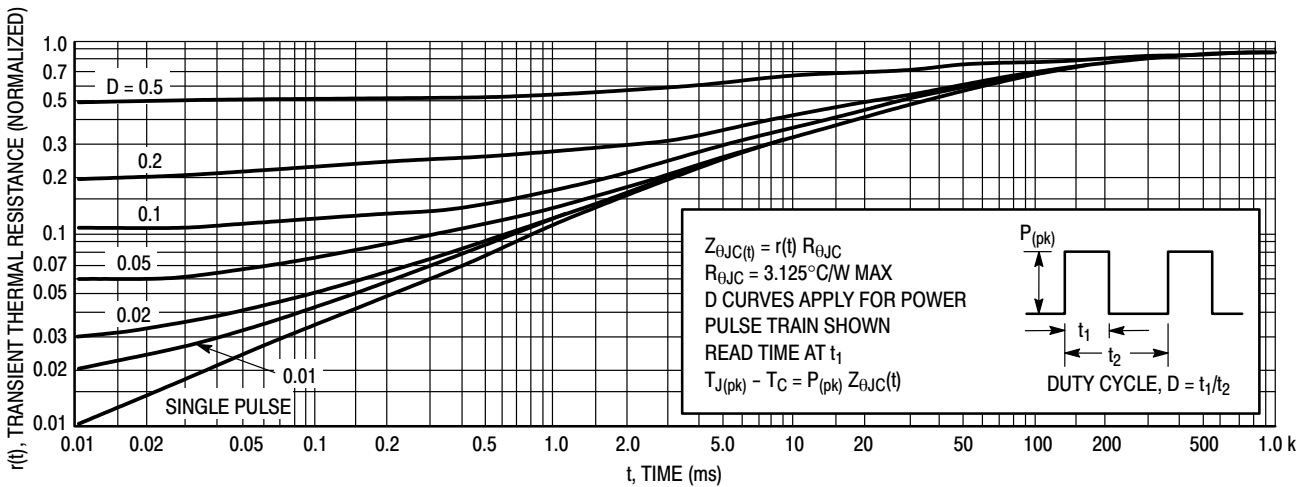


Figure 4. Thermal Response

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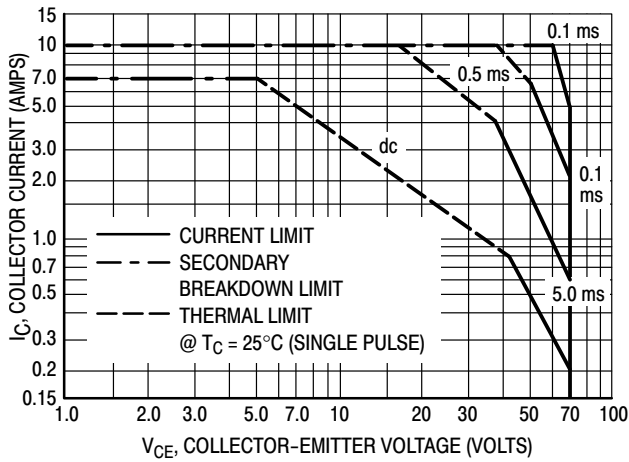


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

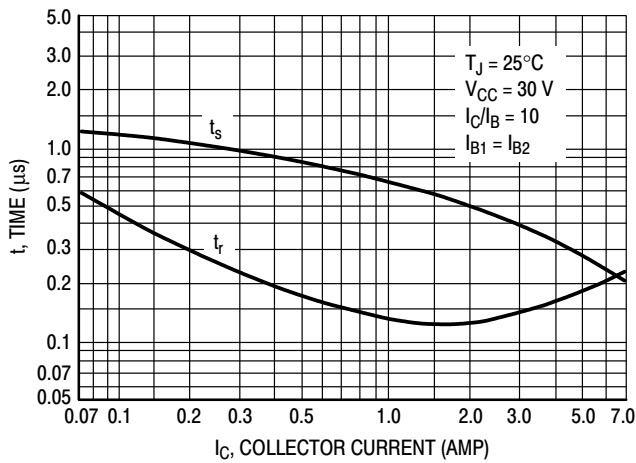


Figure 6. Turn-Off Time

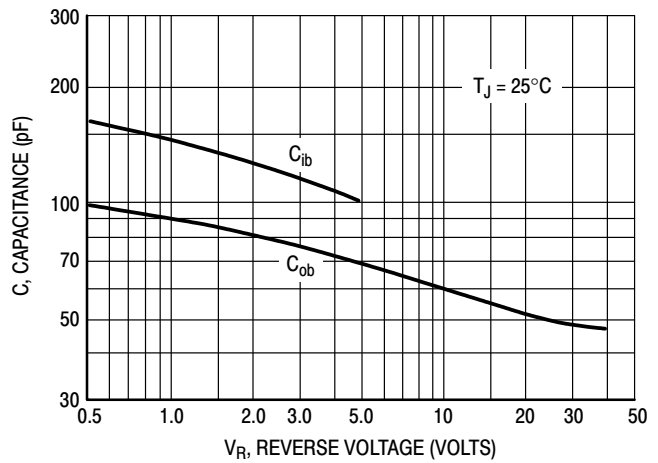


Figure 7. Capacitance

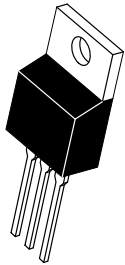
ORDERING INFORMATION

Device	Device Marking	Package	Shipping
2N6107G	2N6107	TO-220 (Pb-Free)	50 Units / Rail
2N6109G	2N6109	TO-220 (Pb-Free)	50 Units / Rail
2N6111G	2N6111	TO-220 (Pb-Free)	50 Units / Rail
2N6288G	2N6288	TO-220 (Pb-Free)	50 Units / Rail
2N6292G	2N6292	TO-220 (Pb-Free)	50 Units / Rail

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

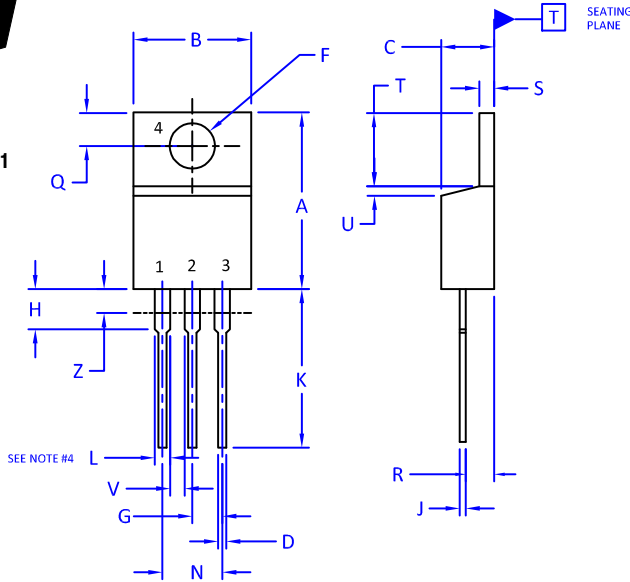
ON Semiconductor®



SCALE 1:1

TO-220 CASE 221A-09 ISSUE AJ

DATE 05 NOV 2019



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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