

**Absolute Maximum Ratings**

RS+, RS- to GND .....-0.3V to +30V  
 OUT to GND .....-0.3V to +6V  
 RS+ to RS- .....±30V  
 Short-Circuit Duration: OUT to GND ..... Continuous  
 Continuous Input Current (Any Pin) ..... ±20mA  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
     4-Bump UCSP (derate 3.0mW/°C above +70°C).....238mW  
     5-Pin SOT23 (derate 3.9mW/°C above +70°C) .....312mW  
     6-Pin µDFN (derate 4.5mW/°C above +70°C) .....358mW

Operating Temperature Range ..... -40°C to +85°C  
 Junction Temperature ..... +150°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (excluding UCSP, soldering, 10s) ..... +300°C  
 Soldering Temperature (reflow) ..... +260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Electrical Characteristics**

(V<sub>RS+</sub> = V<sub>RS-</sub> = 3.6V, V<sub>SENSE</sub> = (V<sub>RS+</sub> - V<sub>RS-</sub>) = 0V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Current (Note 2)	I <sub>CC</sub>	V <sub>RS+</sub> = 5V, T <sub>A</sub> = +25°C		0.5	0.85	µA	
		V <sub>RS+</sub> = 5V, -40°C < T <sub>A</sub> < +85°C			1.1		
		V <sub>RS+</sub> = 28V, T <sub>A</sub> = +25°C		1.1	1.8		
		V <sub>RS+</sub> = 28V, -40°C < T <sub>A</sub> < +85°C			2.5		
Common-Mode Input Range	V <sub>CM</sub>	Guaranteed by CMRR, -40°C < T <sub>A</sub> < +85°C	1.6		28	V	
Common-Mode Rejection Ratio	CMRR	1.6V < V <sub>RS+</sub> < 28V, -40°C < T <sub>A</sub> < +85°C	94	130		dB	
Input Offset Voltage (Note 3)	V <sub>OS</sub>	T <sub>A</sub> = +25°C		±100	±500	µV	
		-40°C < T <sub>A</sub> < +85°C			±600		
Gain	G	MAX9938T		25		V/V	
		MAX9938F		50			
		MAX9938H		100			
		MAX9938W		200			
Gain Error (Note 4)	GE	MAX9938T/MAX9938F/ MAX9938H	T <sub>A</sub> = +25°C	±0.1	±0.5	%	
			-40°C < T <sub>A</sub> < +85°C				±0.6
		MAX9938W	T <sub>A</sub> = +25°C	±0.1	±0.7		
			-40°C < T <sub>A</sub> < +85°C				±0.8
Output Resistance	R <sub>OUT</sub>	(Note 5)	MAX9938T/F/H	7.0	10	13.2	kΩ
			MAX9938W	14.0	20	26.4	
OUT Low Voltage	V <sub>OL</sub>	Gain = 25		1.5	15	mV	
		Gain = 50		3	30		
		Gain = 100		6	60		
		Gain = 200		12	120		
OUT High Voltage	V <sub>OH</sub>	V <sub>OH</sub> = V <sub>RS-</sub> - V <sub>OUT</sub> (Note 6)		0.1	0.2	V	
Small-Signal Bandwidth (Note 5)	BW	V <sub>SENSE</sub> = 50mV, gain = 25		125		V	
		V <sub>SENSE</sub> = 50mV, gain = 50		60		kHz	
		V <sub>SENSE</sub> = 50mV, gain = 100		30			
		V <sub>SENSE</sub> = 50mV, gain = 200		15			
Output Settling Time	t <sub>S</sub>	1% final value, V <sub>SENSE</sub> = 50mV		100		µs	

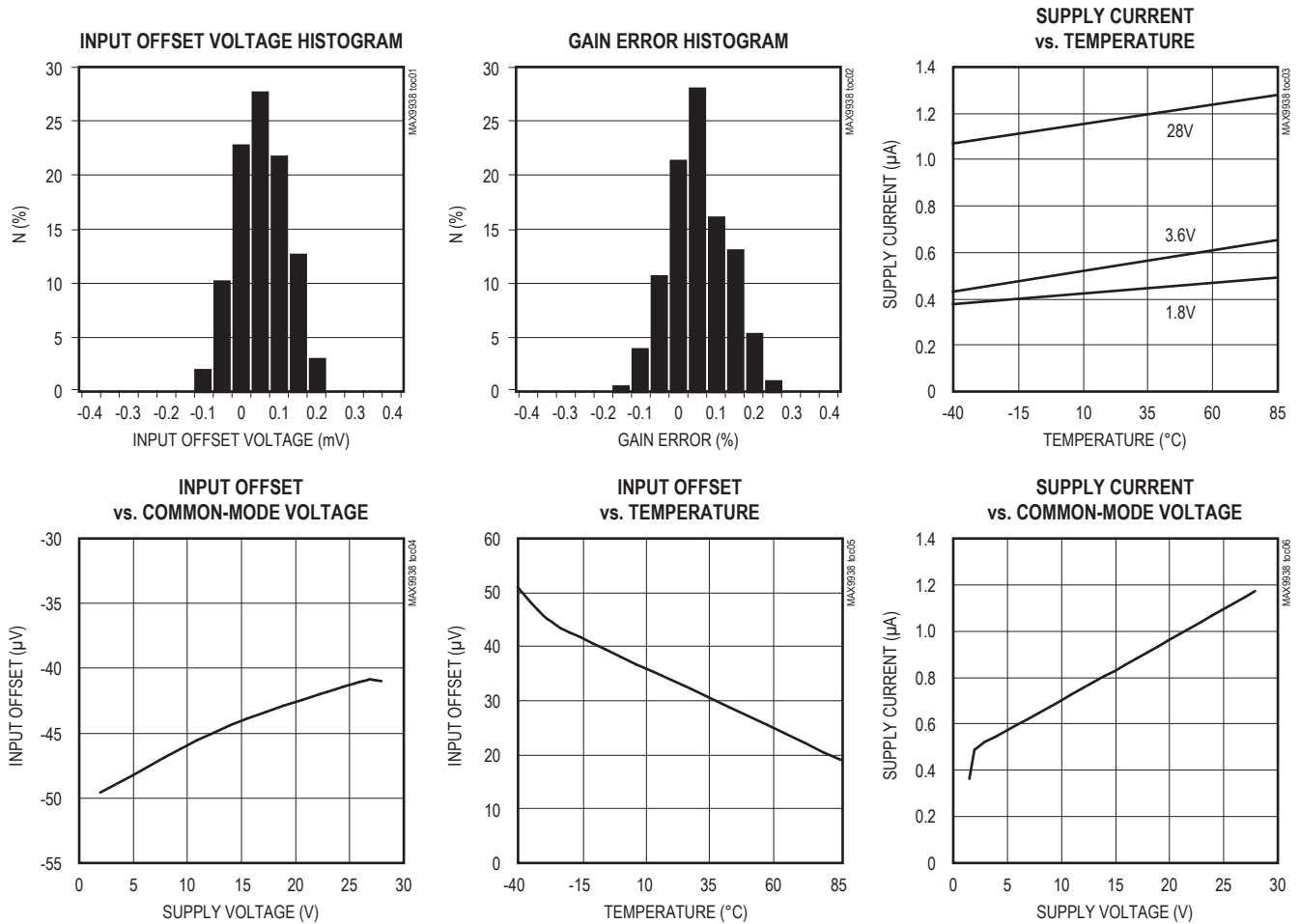
**Electrical Characteristics (continued)**

( $V_{RS+} = V_{RS-} = 3.6V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

- Note 1:** All devices are 100% production tested at  $T_A = +25^{\circ}C$ . All temperature limits are guaranteed by design.
- Note 2:**  $V_{OUT} = 0$ .  $I_{CC}$  is the total current into  $RS+$  plus  $RS-$  pins.
- Note 3:**  $V_{OS}$  is extrapolated from measurements for the gain-error test.
- Note 4:** Gain error is calculated by applying two values of  $V_{SENSE}$  and calculating the error of the slope vs. the ideal:  
 Gain = 25,  $V_{SENSE}$  is 20mV and 120mV.  
 Gain = 50,  $V_{SENSE}$  is 10mV and 60mV.  
 Gain = 100,  $V_{SENSE}$  is 5mV and 30mV.  
 Gain = 200,  $V_{SENSE}$  is 2.5mV and 15mV.
- Note 5:** The device is stable for any external capacitance value.
- Note 6:**  $V_{OH}$  is the voltage from  $V_{RS-}$  to  $V_{OUT}$  with  $V_{SENSE} = 3.6V/gain$ .

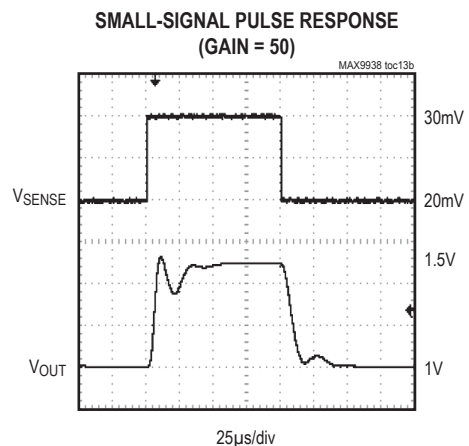
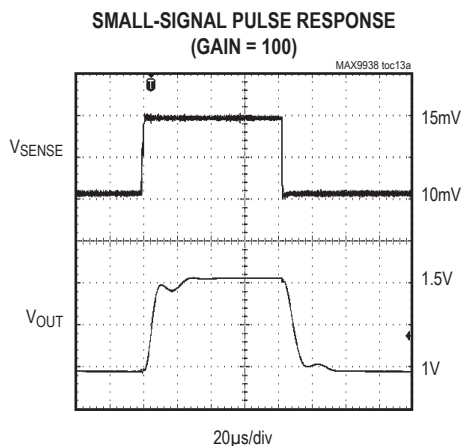
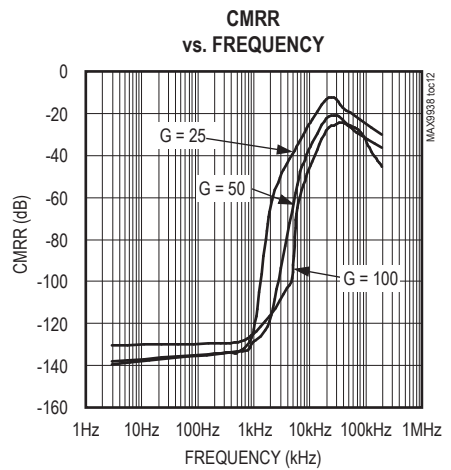
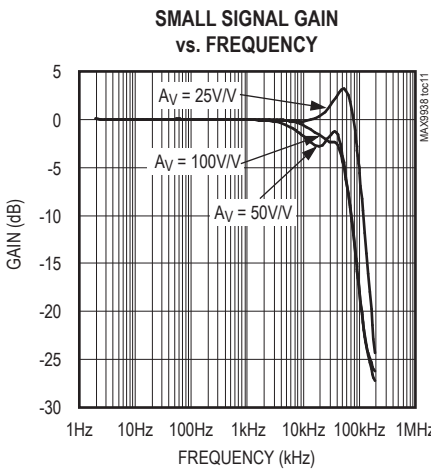
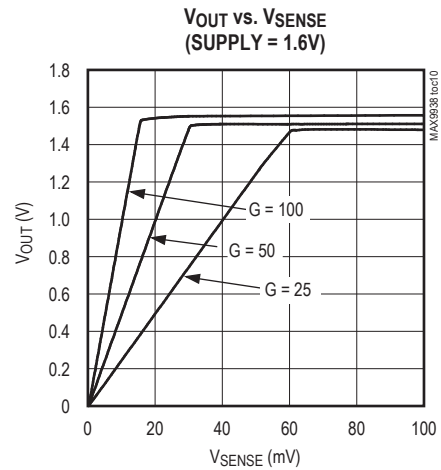
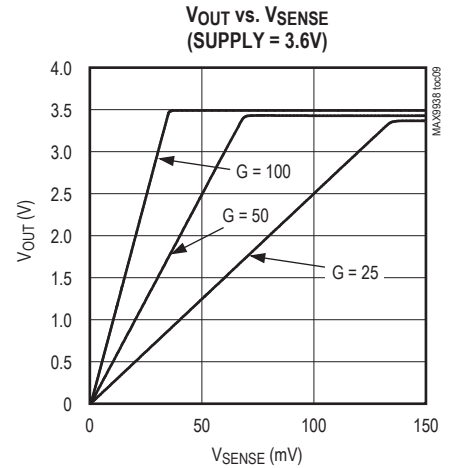
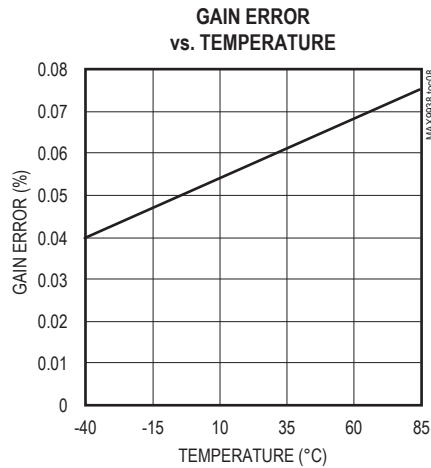
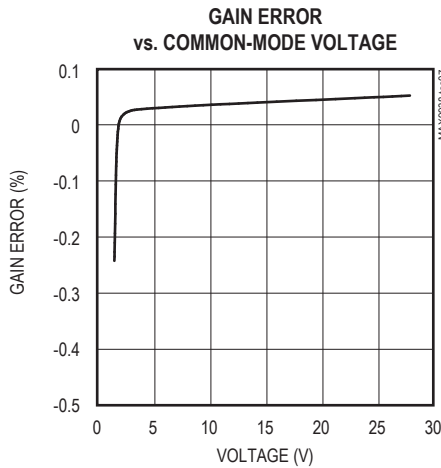
**Typical Operating Characteristics**

( $V_{RS+} = V_{RS-} = 3.6V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



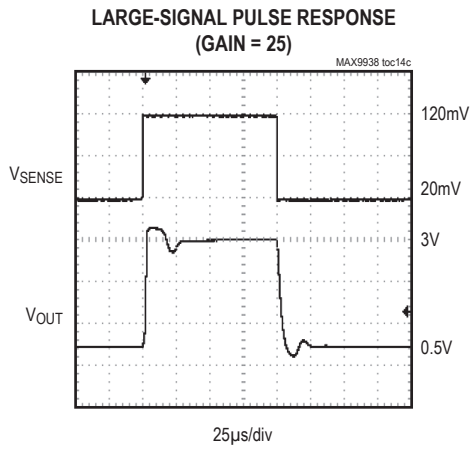
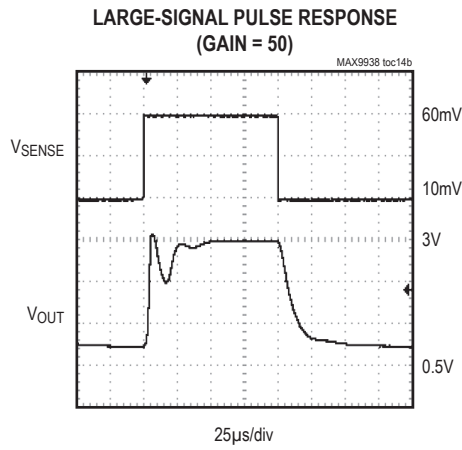
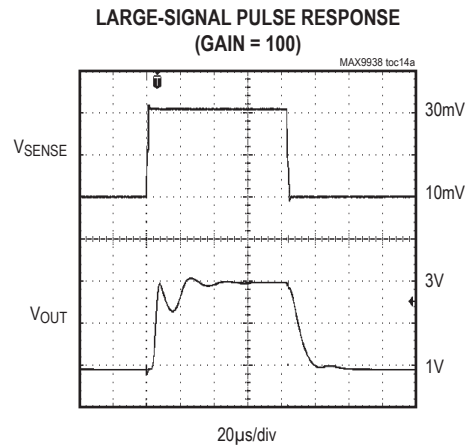
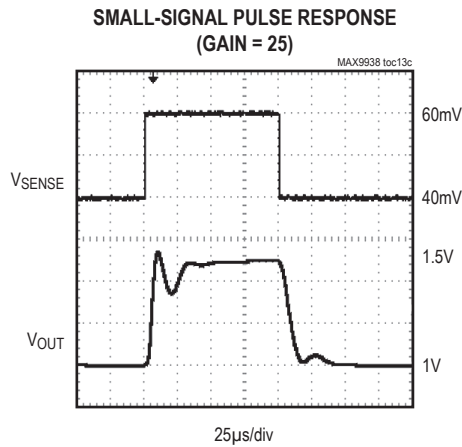
Typical Operating Characteristics (continued)

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**Typical Operating Characteristics (continued)**

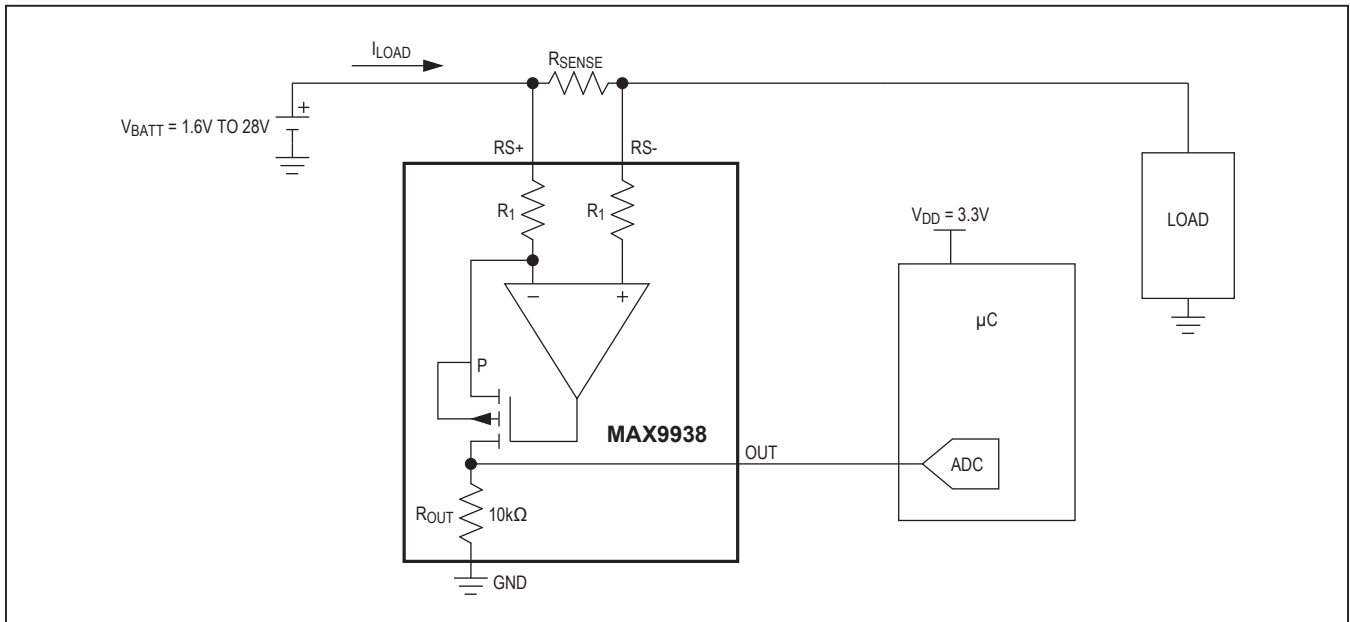
( $V_{RS+} = V_{RS-} = 3.6V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



**Pin Description**

PIN			NAME	FUNCTION
UCSP	SOT23	µDFN		
A1	5	4	RS+	External Sense Resistor Power-Side Connection
A2	4	6	RS-	External Sense Resistor Load-Side Connection
B1	1, 2	3	GND	Ground
B2	3	1	OUT	Output Voltage. $V_{OUT}$ is proportional to $V_{SENSE} = V_{RS+} - V_{RS-}$ .
—	—	2, 5	N.C.	No Connection. Not internally connected.

Typical Operating Circuit



Detailed Description

The MAX9938 unidirectional high-side, current-sense amplifier features a 1.6V to 28V input common-mode range. This feature allows the monitoring of current out of a battery with a voltage as low as 1.6V. The MAX9938 monitors current through a current-sense resistor and amplifies the voltage across that resistor.

The MAX9938 is a unidirectional current-sense amplifier that has a well-established history. An op amp is used to force the current through an internal gain resistor at RS+, which has a value of R<sub>1</sub>, such that its voltage drop equals the voltage drop across an external sense resistor, R<sub>SENSE</sub>. There is an internal resistor at RS-

with the same value as R<sub>1</sub> to minimize offset voltage. The current through R<sub>1</sub> is sourced by a high-voltage p-channel FET. Its source current is the same as its drain current, which flows through a second gain resistor, R<sub>OUT</sub>. This produces an output voltage, V<sub>OUT</sub>, whose magnitude is I<sub>LOAD</sub> × R<sub>SENSE</sub> × R<sub>OUT</sub>/R<sub>1</sub>. The gain accuracy is based on the matching of the two gain resistors R<sub>1</sub> and R<sub>OUT</sub> (see Table 1). Total gain = 25V/V for the MAX9938T, 50V/V for the MAX9938F, 100V/V for the MAX9938H, and 200V/V for the MAX9938W. The output is protected from input overdrive by use of an output current limiting circuit of 7mA (typical) and a 6V clamp protection circuit.

Table 1. Internal Gain Setting Resistors (Typical Values)

GAIN (V/V)	R <sub>1</sub> (Ω)	R <sub>OUT</sub> (kΩ)
200	100	20
100	100	10
50	200	10
25	400	10

## Applications Information

### Choosing the Sense Resistor

Choose  $R_{SENSE}$  based on the following criteria:

#### Voltage Loss

A high  $R_{SENSE}$  value causes the power-source voltage to drop due to IR loss. For minimal voltage loss, use the lowest  $R_{SENSE}$  value.

#### OUT Swing vs. $V_{RS+}$ and $V_{SENSE}$

The MAX9938 is unique since the supply voltage is the input common-mode voltage (the average voltage at  $RS+$  and  $RS-$ ). There is no separate  $V_{CC}$  supply voltage pin. Therefore, the OUT voltage swing is limited by the minimum voltage at  $RS+$ .

$V_{OUT}(\max) = V_{RS+}(\min) - V_{SENSE}(\max) - V_{OH}$   
and

$$R_{SENSE} = \frac{V_{OUT}(\max)}{G \times I_{LOAD}(\max)}$$

$V_{SENSE}$  full scale should be less than  $V_{OUT}/\text{gain}$  at the minimum  $RS+$  voltage. For best performance with a 3.6V supply voltage, select  $R_{SENSE}$  to provide approximately 120mV (gain of 25V/V), 60mV (gain of 50V/V), 30mV (gain of 100V/V), or 15mV (gain of 200V/V) of sense voltage for the full-scale current in each application. These can be increased by use of a higher minimum input voltage.

#### Accuracy

In the linear region ( $V_{OUT} < V_{OUT}(\max)$ ), there are two components to accuracy: input offset voltage ( $V_{OS}$ ) and gain error (GE). For the MAX9938,  $V_{OS} = 500\mu\text{V}(\max)$  and gain error is 0.5% (max). Use the linear equation:

$$V_{OUT} = (\text{gain} \pm \text{GE}) \times V_{SENSE} \pm (\text{gain} \times V_{OS})$$

to calculate total error. A high  $R_{SENSE}$  value allows lower currents to be measured more accurately because offsets are less significant when the sense voltage is larger.

### Efficiency and Power Dissipation

At high current levels, the  $I^2R$  losses in  $R_{SENSE}$  can be significant. Take this into consideration when choosing the resistor value and its power dissipation (wattage) rating. Also, the sense resistor's value might drift if it is allowed to heat up excessively. The precision  $V_{OS}$  of the MAX9938 allows the use of small sense resistors to reduce power dissipation and reduce hot spots.

### Kelvin Connections

Because of the high currents that flow through  $R_{SENSE}$ , take care to eliminate parasitic trace resistance from causing errors in the sense voltage. Either use a four-terminal current-sense resistor or use Kelvin (force and sense) PCB layout techniques.

### Optional Output Filter Capacitor

When designing a system that uses a sample-and-hold stage in the ADC, the sampling capacitor momentarily loads OUT and causes a drop in the output voltage. If sampling time is very short (less than a microsecond), consider using a ceramic capacitor across OUT and GND to hold  $V_{OUT}$  constant during sampling. This also decreases the small-signal bandwidth of the current-sense amplifier and reduces noise at OUT.

### Input Filters

Some applications of current-sense amplifiers need to measure currents accurately even in the presence of both differential and common-mode ripple, as well as a wide variety of input transient conditions. For example, high-frequency ripple at the output of a switching buck or boost regulator results in a common-mode voltage at the inputs of the MAX9938. Alternatively, fast load-current transients, when measuring at the input of a switching buck or boost regulator, can cause high-frequency differential sense voltages to occur at the inputs of the MAX9938, although the signal of interest is the average DC value. Such high-frequency differential sense voltages may result in a voltage offset at the MAX9938 output.

# MAX9938

# nanoPower, 4-Bump UCSP/SOT23, Precision Current-Sense Amplifier

The MAX9938 allows two methods of filtering to help improve performance in the presence of input common-mode voltage and input differential voltage transients. [Figure 1](#) shows a differential input filter.

The capacitor  $C_{IN}$  between  $RS+$  and  $RS-$  along with the resistor  $R_{IN}$  between the sense resistor and  $RS-$  helps filter against input differential voltages and prevents them from reaching the MAX9938.

The corner frequency of this filter is determined by the choice of  $R_{IN}$ ,  $C_{IN}$ , and the value of the input resistance at  $RS-$  ( $R_1$ ). See Table 1 for  $R_1$  values at the different gain options.

The value of  $R_{IN}$  should be chosen to minimize its effect on the input offset voltage due to the bias current at  $RS-$ .  $R_{IN} \times I_{BIAS}$  contributes to the input voltage offset.  $I_{BIAS}$  is typically  $0.2\mu A$ .

Placing  $R_{IN}$  at the  $RS-$  input does not affect the gain error of the device because the gain is given by the ratio between  $R_{OUT}$  and  $R_1$  at  $RS+$ .

[Figure 2](#) shows the input common-mode filter.

Again, the corner frequency of the filter is determined by the choice of  $R_{IN}$ ,  $C_{IN}$  and is affected by  $R_1$ .

In this case  $R_{IN}$  affects both gain error and input offset voltage.  $R_{IN}$  should be smaller than  $R_1$  so that it has negligible effect on the device gain. If, for example, a filter with  $R_{IN} = 10\Omega$  and  $C_{IN} = 1\mu F$  is built, then depending upon the gain selection, the gain error is affected by either 2.5% ( $G = 25V/V$ ,  $R_1 = 400\Omega$ ) or 5% ( $G = 50V/V$ ,  $R_1 = 200\Omega$ ) or 10% ( $G = 100V/V$ ,  $R_1 = 100\Omega$ ) or 10% ( $G = 200V/V$ ,  $R_1 = 100\Omega$ ).

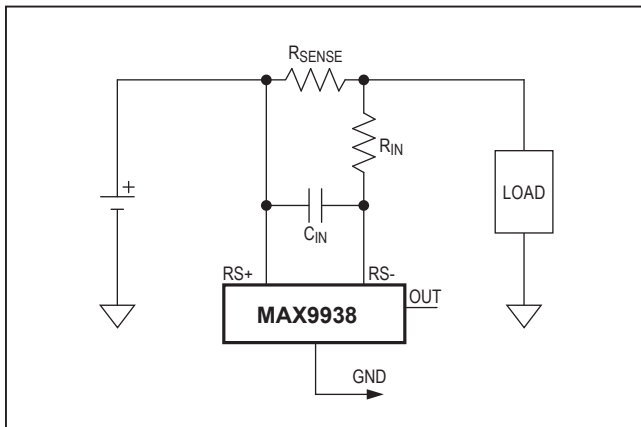


Figure 1. Differential Input Filter

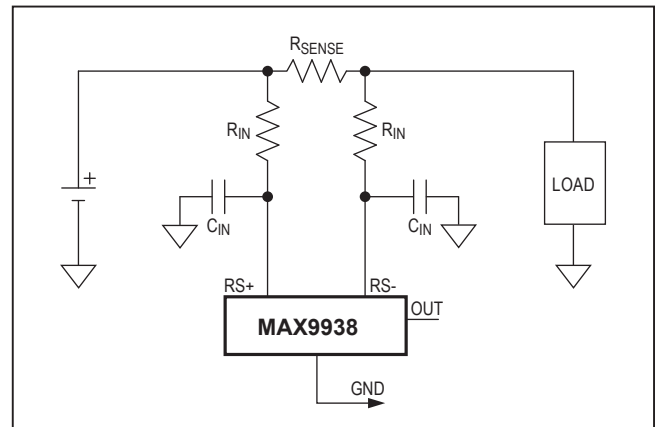


Figure 2. Input Common-Mode Filter

**Bidirectional Application**

Battery-powered systems may require a precise bidirectional current-sense amplifier to accurately monitor the battery's charge and discharge currents. Measurements of the two separate outputs with respect to GND yields an accurate measure of the charge and discharge currents respectively (Figure 3).

**UCSP Applications Information**

For the latest application details on UCSP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications* available on Maxim's website at [www.maximintegrated.com/ucsp](http://www.maximintegrated.com/ucsp).

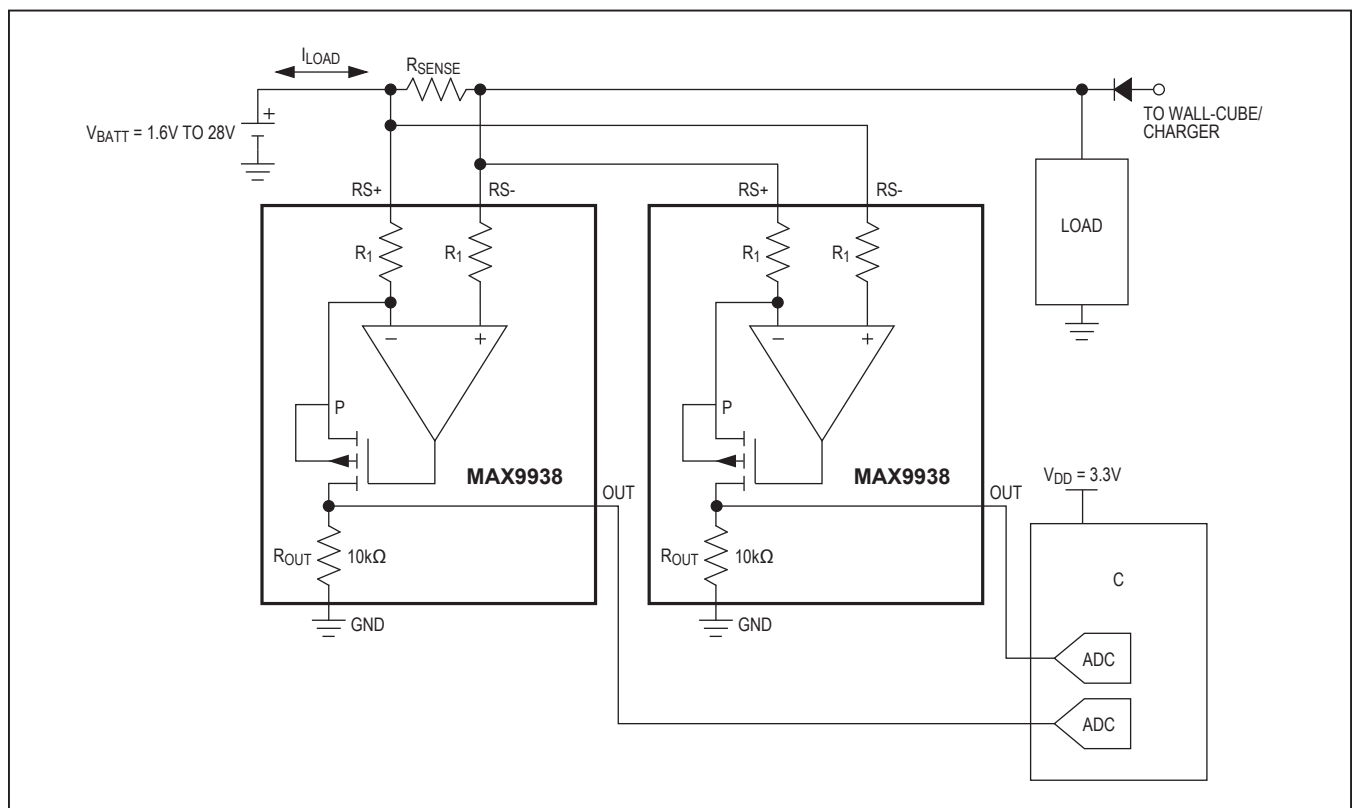


Figure 3. Bidirectional Application

**Chip Information**

PROCESS: BiCMOS



**Package Information**

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
2 x 2 UCSP	B4+1	<a href="#">21-0117</a>	—
5 SOT23	U5-2	<a href="#">21-0057</a>	<a href="#">90-0174</a>
6 µDFN	L622+1	<a href="#">21-0164</a>	<a href="#">90-0004</a>

TOP VIEW

BOTTOM VIEW

SIDE VIEW

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	0.50 BASIC
E1	0.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B4-1	1.00±0.05	1.00±0.05	NONE
B4-2	1.05±0.05	1.05±0.05	NONE
B4-3	1.10±0.05	1.10±0.05	NONE

**NOTES:**

- ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
- MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC #10-0131.
- OUTER DIMENSION (D & E) IS DEFINES BY CENTER LINES BETWEEN SCRIBE LINES.
- MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY. NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.
- ALL DIMENSIONS APPLY BOTH TO LEAD FREE (+) & LEADED (-) PKG. CODES.
- PACKAGE CODE: B4-1, B4-2, B4-3

-DRAWING NOT TO SCALE-

TITLE:  
PACKAGE OUTLINE, 4 BUMPS UCSP (B),  
2X2 ARRAY

APPROVAL	DOCUMENT CONTROL NO. 21-0117	REV. I	1/1
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Package Information (continued)

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**TOP VIEW**

**SIDE VIEW**

**FRONT VIEW**

SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
α	0°	2.5°	8°
PKG CODES: U5-1, U5-2			

**NOTES:**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
- PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
- PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
- MEETS JEDEC MO178, VARIATION AA.
- LEADS TO BE COPLANAR WITHIN 0.10 mm.
- SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.

**maxim integrated.**

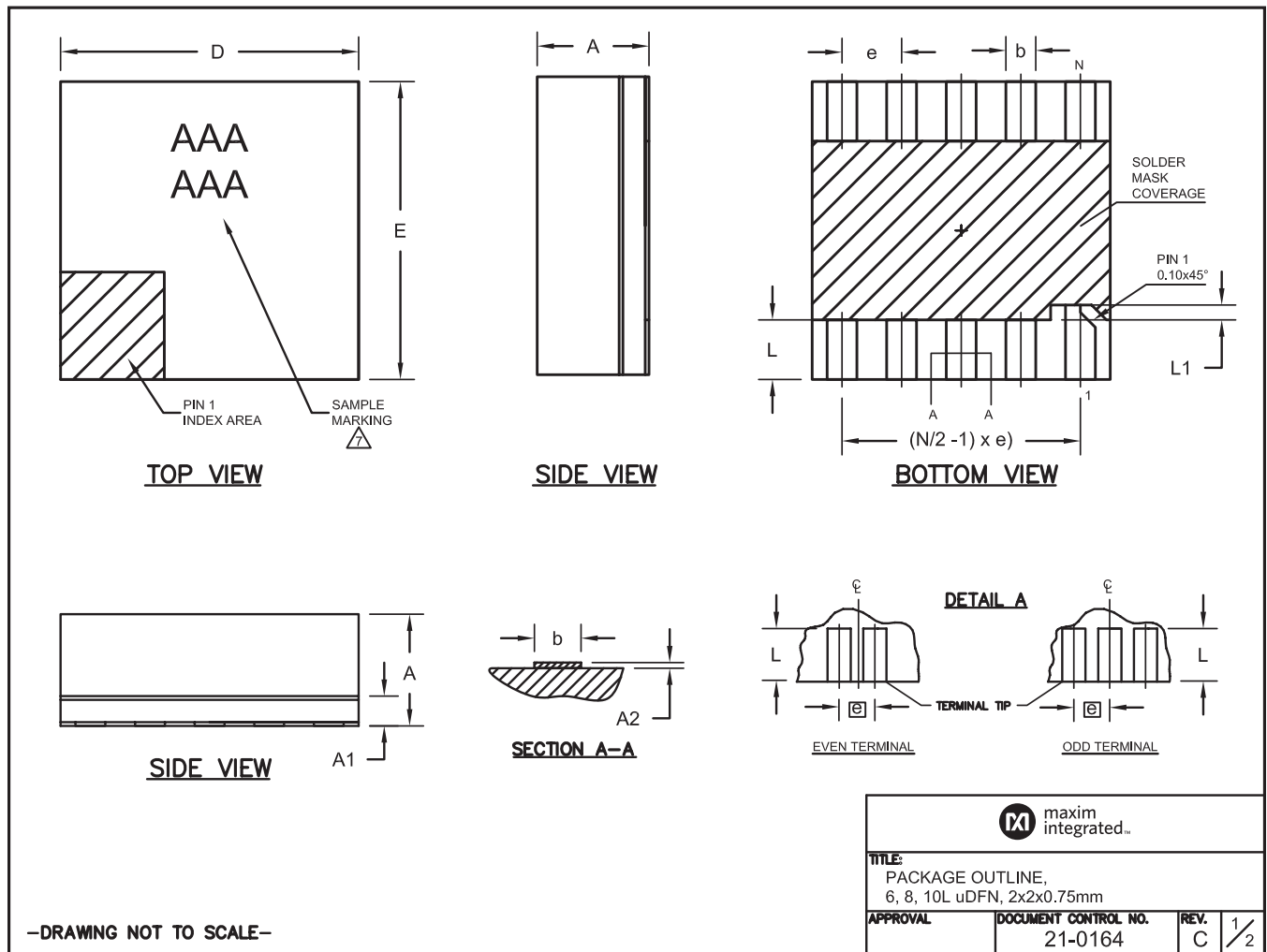
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SOT-23 5L .EPS

**Package Information (continued)**

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PKG. CODES							
[U5-1 / U5+1] [U5-2 / U5+2]							
<p>The drawing shows a top-down view of the package land pattern. It features four rectangular pads arranged in a 2x2 grid. The horizontal distance between the centers of the two pads in a row is 2.50 mm. The vertical distance between the centers of the two pads in a column is 0.95 mm. The width of each pad is 1.30 mm. The distance from the center of each pad to the edge of the pad is 0.55 mm.</p>							
<p>NOTES:</p> <ol style="list-style-type: none"> <li>1. REFERENCE PKG. OUTLINE: 21-0057.</li> <li>2. LAND PATTERN COMPLIES TO: IPC7351A.</li> <li>3. TOLERANCE: +/- 0.02 MM.</li> <li>4. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.</li> <li>5. ALL DIMENSIONS IN MM.</li> </ol> <p style="text-align: center;">-DRAWING NOT TO SCALE-</p>							
<p>This document (including dimensions, notes &amp; specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depend on many factors unknown to Maxim (eg. user's board manufacturing specs), user must determine suitability for use. This document is subject to change without notice. Contact technical support at <a href="http://www.maxim-ic.com/support">http://www.maxim-ic.com/support</a> for further questions.</p>							
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="3" style="padding: 2px;">TITLE: PACKAGE LAND PATTERN, [U5] 5L SOT23</td> </tr> <tr> <td style="width: 33%; padding: 2px;">APPROVAL</td> <td style="width: 33%; padding: 2px;">DOCUMENT CONTROL NO. 90-0174</td> <td style="width: 33%; padding: 2px;">REV. B 1/1</td> </tr> </table>		TITLE: PACKAGE LAND PATTERN, [U5] 5L SOT23			APPROVAL	DOCUMENT CONTROL NO. 90-0174	REV. B 1/1
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APPROVAL	DOCUMENT CONTROL NO. 90-0174	REV. B 1/1					

**Package Information (continued)**

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">PKG. CODES</td> </tr> <tr> <td style="text-align: center;">[L622-1 / L622+1] [L622+1C]</td> </tr> </table>		PKG. CODES	[L622-1 / L622+1] [L622+1C]										
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[L622-1 / L622+1] [L622+1C]													
<p>The diagram shows a top-down view of a package with four rectangular bumps arranged in a 2x2 grid. Dimension lines indicate the following measurements: 0.65 mm for the width of a single bump, 0.80 mm for the distance between the centers of two bumps in a row, 1.83 mm for the distance between the centers of two bumps in a column, and 0.35 mm for the width of the package body.</p>													
<p>NOTES:</p> <ol style="list-style-type: none"> <li>1. REFERENCE PKG. OUTLINE: 21-0164.</li> <li>2. LAND PATTERN COMPLIES TO: IPC7351A.</li> <li>3. TOLERANCE: +/- 0.02 MM.</li> <li>4. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.</li> <li>5. ALL DIMENSIONS IN MM.</li> </ol>													
<p>—DRAWING NOT TO SCALE—</p>													
<div style="text-align: right;">  maxim integrated.         </div>													
<p>This document (including dimensions, notes &amp; specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depend on many factors unknown to Maxim (eg. user's board manufacturing specs), user must determine suitability for use. This document is subject to change without notice. Contact technical support at <a href="http://www.maximintegrated.com/support">http://www.maximintegrated.com/support</a> for further questions.</p>													
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="3" style="font-size: small;">TITLE:</td> </tr> <tr> <td colspan="3" style="text-align: center;">PACKAGE LAND PATTERN, [L622] uDFN</td> </tr> <tr> <td style="font-size: x-small;">APPROVAL</td> <td style="font-size: x-small;">DOCUMENT CONTROL NO.</td> <td style="font-size: x-small;">REV.</td> </tr> <tr> <td></td> <td style="text-align: center;">90-0004</td> <td style="text-align: center;">C 1/1</td> </tr> </table>		TITLE:			PACKAGE LAND PATTERN, [L622] uDFN			APPROVAL	DOCUMENT CONTROL NO.	REV.		90-0004	C 1/1
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## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/08	Initial release	—
1	9/08	Added $\mu$ DFN package information	1, 2, 4, 5, 9
2	2/09	Added G45 designation to part number	1
3	10/09	Added <i>Input Filters</i> section and MAX9938W to the data sheet	1, 2, 6–9
4	2/10	Updated EC table and <i>Input Filters</i> section	2, 8
5	8/10	Removed Power-Up Time parameter	2
6	1/11	Corrected error on Figure 2	8
7	4/17	Updated title of data sheet to include “nanoPower”	1–14
7.1		Corrected broken links in <i>Package Information</i>	10

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