ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
I/O to GND (I/O1, I/O2, I/O3) .....-0.3V to +30V
I/O Sink Current (I/O1, I/O2, I/O3),
Internally Limited .....-1mA to +50mA
Digital Inputs to GND (SMBCLK, SMBDATA, $\overline{SMBSUS}$, $\overline{ALERT}$) .....-0.3V to +6V
ADD to GND .....-0.3V to (V_{CC} + 0.3V)
SMBDATA Current, $\overline{ALERT}$ Current .....-1mA to +50mA

Continuous Power Dissipation (T_A = +70°C)
10-pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range
MAX166_EUB .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are for T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range			2.7		5.5	V
Supply Current		Static condition; SMBDATA, SMBCLK, ADD, $\overline{ALERT}$ = V_{CC} or GND (Note 2)		3	10	µA
Undervoltage Lockout/ Power-On Reset Threshold		V_{CC} falling	1.2	1.6	2.5	V
I/O Sink Current		$V_{I/O\_}$ = 0.4V, V_{CC} = 2.7V or 5.5V	2			mA
		$V_{I/O\_}$ = 1.0V, V_{CC} = 4.5V	8	13		
I/O Current Limit		I/O1, I/O2, or I/O3; V_{CC} = 4.5V	15	20	50	mA
Thermal Shutdown		Typical hysteresis of 10°C		140		°C
I/O Leakage Current		$V_{I/O\_}$ = 28V, high-impedance state		0.5	5	µA
		$V_{I/O\_}$ = 0V, V_{CC}; high-impedance state	-1	0.5	1	
Digital Input Current		$V_{SMBDATA}$, V_{SMBCLK}, $V_{\overline{SMBSUS}}$, V_{ADD} = 0V, V_{CC}	-1		1	µA
SMBus Logic Input Voltage Range		V_{CC} = 2.7V to 5.5V; SMBDATA, SMBCLK, $\overline{SMBSUS}$	0		5.5	V
Logic Input High Voltage		I/O_, $\overline{SMBSUS}$, SMBCLK, SMBDATA	2.4			V
Logic Input Low Voltage		I/O_, $\overline{SMBSUS}$, SMBCLK, SMBDATA			0.8	V
SMBDATA Output Low Sink Current		$V_{SMBDATA}$ = 0.6V	6			mA
$\overline{ALERT}$ Output Low Sink Current		$V_{\overline{ALERT}}$ = 0.4V	1			mA
$\overline{ALERT}$ Output Leakage Current		$V_{\overline{ALERT}}$ = 5.5V, high-Z state			1	µA
SMBus Input Capacitance		SMBCLK, SMBDATA		5		pF
SMBus Clock Frequency		(Notes 3, 4)			100	kHz
SMBCLK High Time	t_{HIGH}	Measured between the 90% level of the rising edge and the 90% level of the falling edge	4			µs
SMBCLK Low Time	t_{LOW}	Measured between the 10% level of the falling edge and the 10% level of the rising edge	4.7			µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are for T_A = +25°C.) (Note 1)

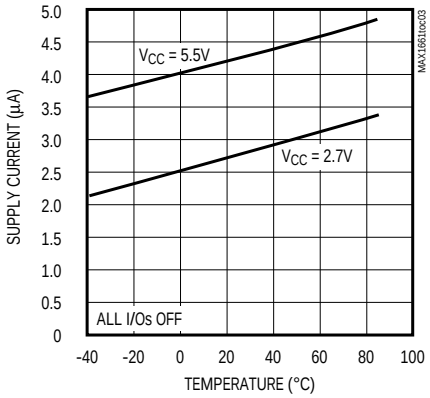
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Start-Condition Setup Time	$t_{SU:STA}$	Measured from 90% of the SMBCLK rising edge to 90% of the SMBDATA falling edge		4.7			µs
Start-Condition Hold Time	$t_{HD:STA}$	Measured from 10% of the falling edge of SMBDATA to 90% of the falling edge of SMBCLK		4			µs
SMBus Stop-Condition Setup Time	$t_{SU:STO}$	Measured from 90% of the rising edge of SMBCLK to 10% of the rising edge of SMBDATA		4			µs
SMBDATA Valid to SMBCLK Rising Edge Time, Slave Clocking in Data	$t_{SU:DAT}$	10% or 90% of SMBDATA to 10% of the rising edge of SMBCLK	V_{CC} = 4.5V to 5.5V	500			ns
			V_{CC} = 2.7V to 4.5V	1000			
SMBCLK Falling Edge to SMBDATA Transition Hold Time	$t_{HD:DAT}$	(Notes 4, 5)		0			µs
SMBCLK Falling Edge to SMBus Data Valid Time	t_{DV}	Tested with a 10kΩ pull-up resistor on SMBDATA (Note 6)				1	µs
SMBus Bus-Free Time	t_{BUF}	Between stop and start conditions (Note 7)		4.7			µs
SMBus Write to I/O_ Propagation Delay	$t_{P:I/O}$	Measured from SMBCLK rising edge to 10% or 90% of I/O (Note 4)			100		ns
I/O Data Valid to SMBCLK Rising-Edge Setup Time	$t_{SU:I/O}$	Measured from 10% or 90% of $V_{I/O}$ to 10% of the rising edge of SMBCLK (Note 8)		15			µs
I/O Data Hold Time	$t_{HD:I/O}$	(Note 8)		0			µs
START-STOP Software-Interrupt Pulse Width	$t_{LOW:SS}$	Measured from the 10% point of the falling edge of SMBDATA to the 10% point of the rising edge of SMBDATA (Note 7)		10	15	30	µs

Note 1: Specifications from 0°C to -40°C are guaranteed by design, not production tested.
Note 2: Supply current is specified for static state only.
Note 3: The SMBus logic block is a static design that works with clock frequencies down to DC. While slow operation is possible, it violates the 10kHz minimum clock frequency of the SMBus specifications, and may monopolize the bus.
Note 4: Refer to Figures 2a and 2b for SMBus timing parameter definitions (write and read diagrams).
Note 5: A transition must internally provide a hold time of 300ns to accommodate for the undefined region of the falling edge.
Note 6: Refer to Figure 3 for the acknowledge timing diagram and t_{DV} parameter definition.
Note 7: Refer to Figure 5 for START-STOP interrupt timing diagrams and parameter definitions.
Note 8: Refer to Figure 4 for I/O setup and hold timing parameter definitions.

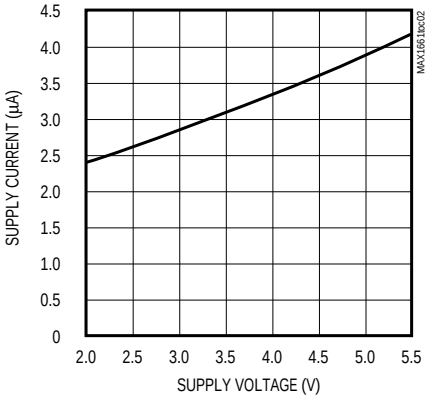
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

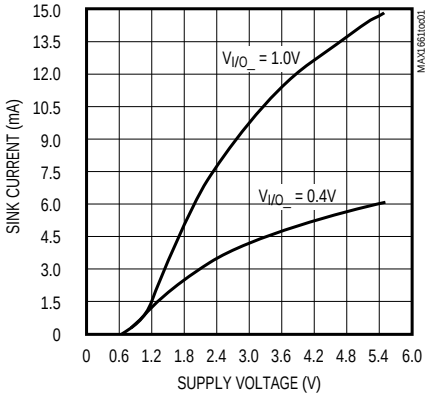
SUPPLY CURRENT vs. TEMPERATURE



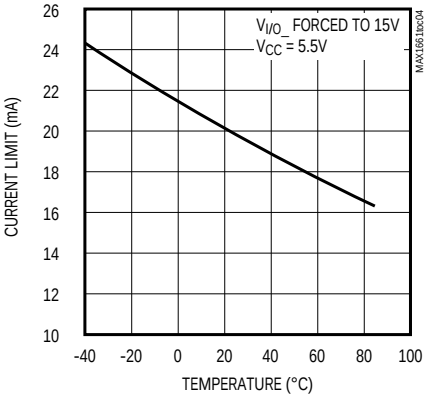
SUPPLY CURRENT vs. SUPPLY VOLTAGE



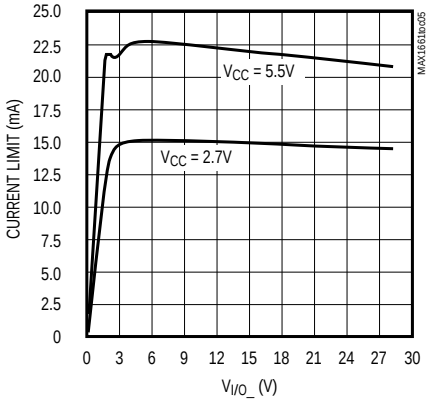
I/O_ SINK CURRENT vs. SUPPLY VOLTAGE



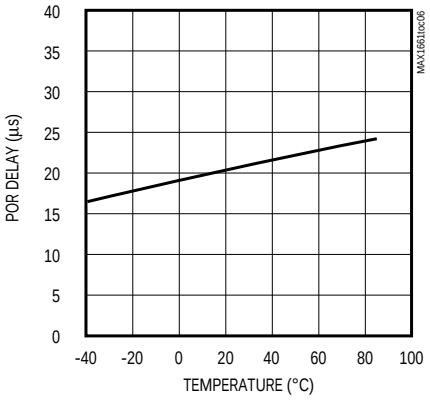
I/O_ CURRENT LIMIT vs. TEMPERATURE



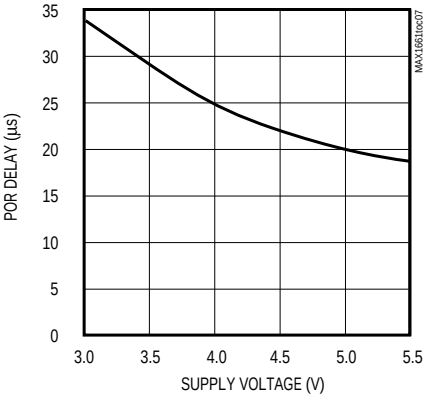
I/O_ CURRENT LIMIT vs. I/O_ VOLTAGE



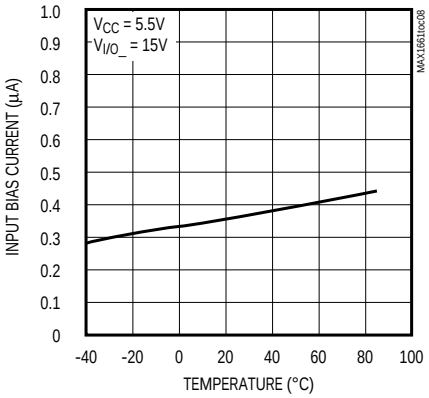
POR DELAY vs. TEMPERATURE



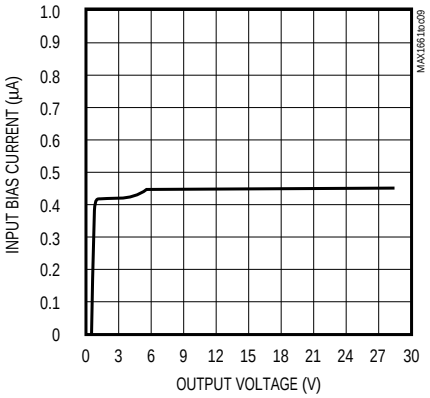
POR DELAY vs. SUPPLY VOLTAGE



I/O_ INPUT BIAS CURRENT vs. TEMPERATURE



I/O_INPUT BIAS CURRENT vs. OUTPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Supply Voltage Input, 2.7V to 5.5V.
2	I/O1	Input 1 or Output 1 (open drain). This pin can tolerate up to 28V.
3	I/O2	Input 2 or Output 2 (open drain). This pin can tolerate up to 28V.
4	I/O3	Input 3 or Output 3 (open drain). This pin can tolerate up to 28V.
5	GND	Ground
6	ADD	SMBus Address Select Pin (see Table 1 for details).
7	$\overline{SMBSUS}$	SMBus Suspend-Mode Control Input. Drive low to select the suspend-mode register. Drive high to select the normal-mode register. (See *Detailed Description*.)
8	SMBDATA	SMBus Serial-Data Input/Output (open drain)
9	SMBCLK	SMBus Serial Clock Input
10	$\overline{ALERT}$	Interrupt Output, active low, open drain

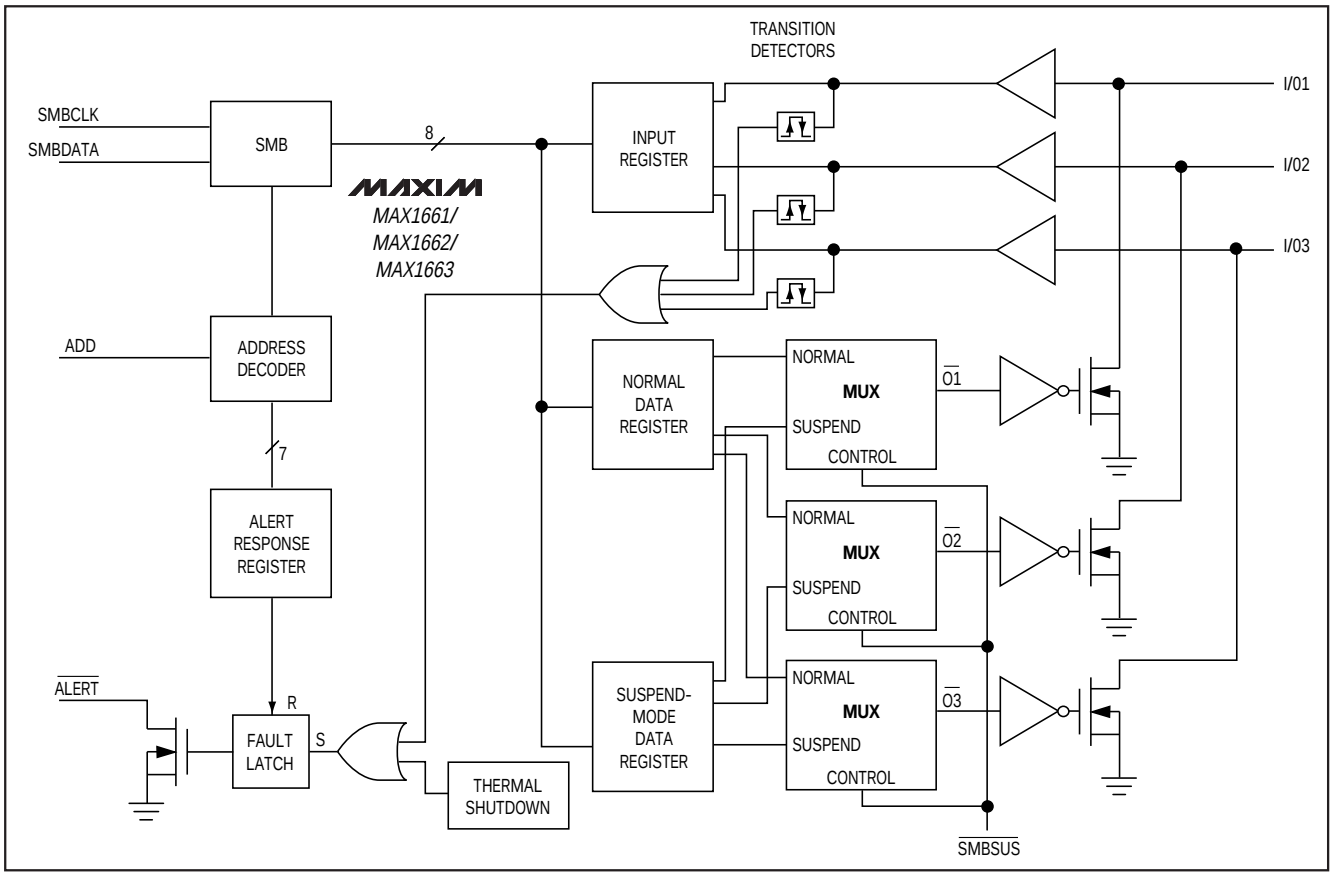


Figure 1. Functional Diagram

Detailed Description

The MAX1661/MAX1662/MAX1663 convert 2-wire SMBus serial data into three latched parallel outputs (I/O1, I/O2, I/O3). These devices are intended to drive N-channel and P-channel, high-side MOSFET switches in load power-management systems. Readback capabilities allow them to function as parallel-to-serial devices. The MAX1661/MAX1662/MAX1663 operate from a single supply with a typical quiescent current of 3µA, making them ideal for portable applications (Figure 1).

SMBus Interface Operation

The SMBus serial interface is a 2-wire interface with multi-mastering capability. From a software perspective, the MAX1661/MAX1662/MAX1663 appears as a set of byte-wide registers that contain information controlling the I/O_ pins, masking capabilities, and a control bit that determines which register is being addressed. The 2-wire slave interface employs standard SMBus send-byte and receive-byte protocols. SMBDATA and SMBCLK are Schmitt-triggered inputs that can accommodate slower edges; however, the rising and falling edges should still be faster than 1µs and 300ns, respectively. Except for the stop and start conditions, the SMBDATA input never transitions while SMBCLK is high. A third interface line ($\overline{SMBSUS}$) is used to execute commands asynchronously from previously stored registers (see the section *$\overline{SMBSUS}$ (Suspend-Mode) Input)*. This reduces the inherent delay in a standard 2-wire serial interface. In the receive-byte operation, the SMBus interface reads back I/O states and thermal-shutdown status.

SMBus Addressing

Each slave device only responds to two addresses: its own unique address and the alert response address. The device's unique address is determined at power-up (Table 1). The three-level state of the address-select pin (ADD) is only sampled upon power-on reset (POR) causing momentary input bias current of 100µA. The address will not change until the part is power cycled. Stray capacitance in excess of 50pF on the ADD pin when floating may cause address recognition problems.

The normal start condition consists of a high-to-low transition on SMBDATA while SMBCLK is high. After the start condition, the master transmits a 7-bit address followed by a single bit to determine whether the device is sending or receiving (high = READ, low = WRITE). If the address is correct, the MAX1661/MAX1662/MAX1663 sends an acknowledgment pulse by pulling SMBDATA low. Otherwise, the address is not recognized and the device stays off the bus and waits until another start condition occurs.

Table 1. SMBus Addresses

ADD	MAX1661	MAX1662	MAX1663
GND	0100000	0100001	0100010
High-Z (floating)	0111100	0111101	0111110
V_{CC}	1001000	1001001	1001010

SMBus Send-Byte Commands

If the MAX1661/MAX1662/MAX1663 receives its correct slave address (Table 1) followed by R/$\overline{W}$ low, it expects to receive a byte of information. If the device detects a start or stop condition prior to clocking in the byte of data, it considers this an error condition and disregards all of the data.

The MAX1661/MAX1662/MAX1663 generates a first acknowledge after the write bit and another acknowledge after the data. It executes the data byte at the rising edge of SMBCLK following the second acknowledge, just prior to the stop condition (Figure 2a). See Table 2 for send-byte operations.

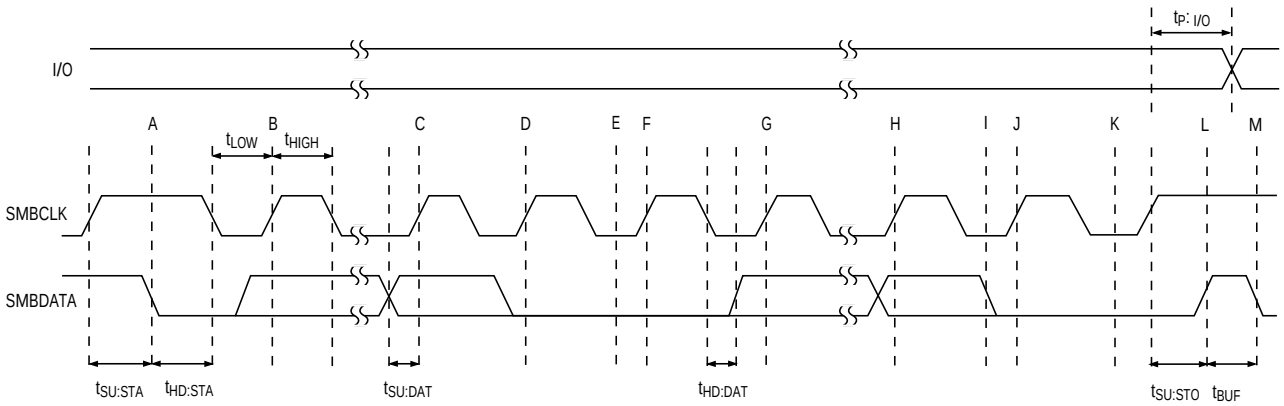
$\overline{SMBSUS}$ (Suspend-Mode) Input

The SMBus can write to either of the normal-data and suspend-mode registers via the MSB (bit 7) of the send-byte word (Table 2). The state of the $\overline{SMBSUS}$ input selects which register contents (normal data or suspend mode) are applied to the I/O_ pins. Driving $\overline{SMBSUS}$ low selects the suspend-mode register, while driving $\overline{SMBSUS}$ high selects the normal-data register. This feature allows the system to select between two different power-plane configurations asynchronously, eliminating latencies introduced by the serial bus. $\overline{SMBSUS}$ typically connects to the SUSTAT# signal in a notebook computer.

SMBus Receive-Byte Operation

If the MAX1661/MAX1662/MAX1663 receives its correct slave address, followed by R/$\overline{W}$ high, the device becomes a slave transmitter (Figure 2b). After receiving the address data, the device generates an acknowledge during the acknowledge clock pulse and drives SMBDATA in sync with SMBCLK. The SMB protocol requires that the master terminate the read transmission by not acknowledging during the acknowledge bit of SMBCLK. See Table 3 for receive-byte data format. Figure 4 shows the complete receive-byte operation timing diagram.

The logic states of the three I/O pins can be read over the serial interface (Table 3). The state of the I/O pins is sampled at the falling edge of the SMBCLK pulse that follows the R/$\overline{W}$ bit and acknowledge bit (Figure 4). The states of the I/O bits in the status register reflect the



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW

F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO SLAVE (OP/SUS BIT)
H = LSB OF DATA CLOCKED INTO SLAVE
I = SLAVE PULLS SMBDATA LINE LOW

J = ACKNOWLEDGE CLOCKED INTO MASTER
K = ACKNOWLEDGE CLOCK PULSE
L = STOP CONDITION, DATA EXECUTED BY SLAVE
M = NEW START CONDITION

Send-Byte Format

	ADDRESS	WRITE	ACK	DATA	ACK	
START CONDITION	7 bits	1 bit (low)	1 bit (low)	8 bits	1 bit (low)	STOP CONDITION

Shaded = Slave Transmission

Figure 2a. SMBus Send-Byte Timing Diagram and Format

Table 2. Format for Send-Byte Data

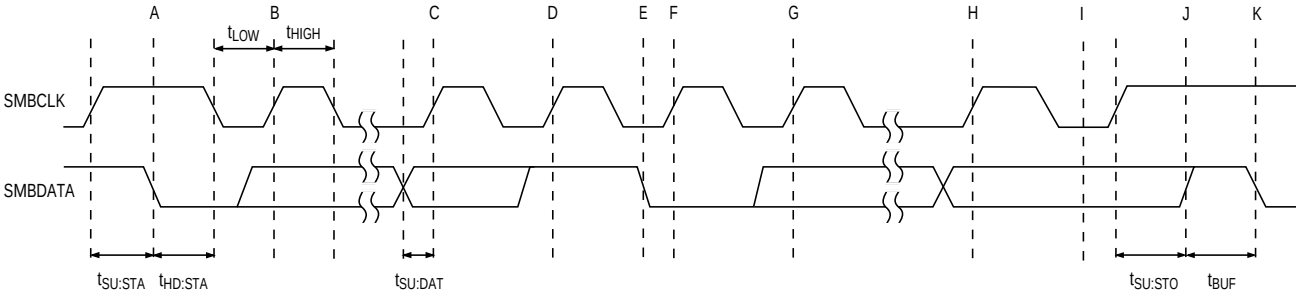
BIT	NAME	POR STATE* (MAX1661)	POR STATE* (MAX1662/MAX1663)	FUNCTION
7 (MSB)	SELECT	N/A	N/A	Writes data to normal register when high; writes data to suspend register when low.
6	Mask SS	1	1	Masks START-STOP software interrupts when high.
5	Mask 3	1	1	Masks I/O3 interrupts when high.
4	Mask 2	1	1	Masks I/O2 interrupts when high.
3	Mask 1	1	1	Masks I/O1 interrupts when high.
2	I/O3	0	1	I/O output enable bit. I/O3 is on when this bit is low (low state).
1	I/O2	0	1	I/O output enable bit. I/O2 is on when this bit is low (low state).
0	I/O1	0	1	I/O output enable bit. I/O1 is on when this bit is low (low state).

***Note:** *POR states apply to both suspend- and normal-mode registers.*

current I/O pin states (i.e., they are not latched). There is a 15µs data-setup time requirement, due to the slow level translators needed for high-voltage (28V) operation. Data-hold time is zero.

Interrupts

The MAX1661/MAX1662/MAX1663 generate interrupts (hardware and software) whenever the logic states of the I/O pins change or when thermal shutdown occurs. Interrupts are signaled with the hardware $\overline{\text{ALERT}}$ pin



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO MASTER
H = LSB OF DATA CLOCKED INTO MASTER
I = ACKNOWLEDGE CLOCK PULSE
J = STOP CONDITION
K = NEW START CONDITION

Receive-Byte Format

	ADDRESS	READ	ACK	DATA	$\overline{\text{ACK}}$	
START CONDITION	7 bits	1 bit (high)	1 bit (low)	8 bits	1 bit (high-Z)	STOP CONDITION

$\overline{ACK}$ = SMBDATA High
Shaded = Slave Transmission

Figure 2b. SMBus Receive-Byte Timing Diagram and Format

Table 3. Format for Receive-Byte Data

BIT	NAME	POR STATE	FUNCTION	LATCHED
7 (MSB)	—	0	Not used	—
6	—	0	Not used	—
5	—	0	Not used	—
4	—	0	Not used	—
3	THSD	N/A	This bit indicates a thermal shutdown.	Yes
2	Data 3	N/A	This bit indicates the state of I/O3 (high or low).	No
1	Data 2	N/A	This bit indicates the state of I/O2 (high or low).	No
0	Data 1	N/A	This bit indicates the state of I/O1 (high or low).	No

and with the software START-STOP method (software interrupts are discussed in the *START-STOP Software Interrupt* section). The I/O interrupts can be masked individually. In addition, the software START-STOP interrupt can be masked independently. The power-on-reset state masks the START-STOP interrupt, as well as the individual I/O interrupts to the $\overline{\text{ALERT}}$ pin (Table 1). The thermal-shutdown interrupt cannot be masked. Note that excessive noise on the supply can cause false interrupts (see *Applications Information*).

The MAX1661/MAX1662/MAX1663 are slave-only devices that never initiate communications, except when asserting an interrupt by forcing $\overline{\text{ALERT}}$ low, or via the software START-STOP interrupt.

Alert Response Address (0001100)

The Alert Response (interrupt pointer) address provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. When a slave device generates an inter-

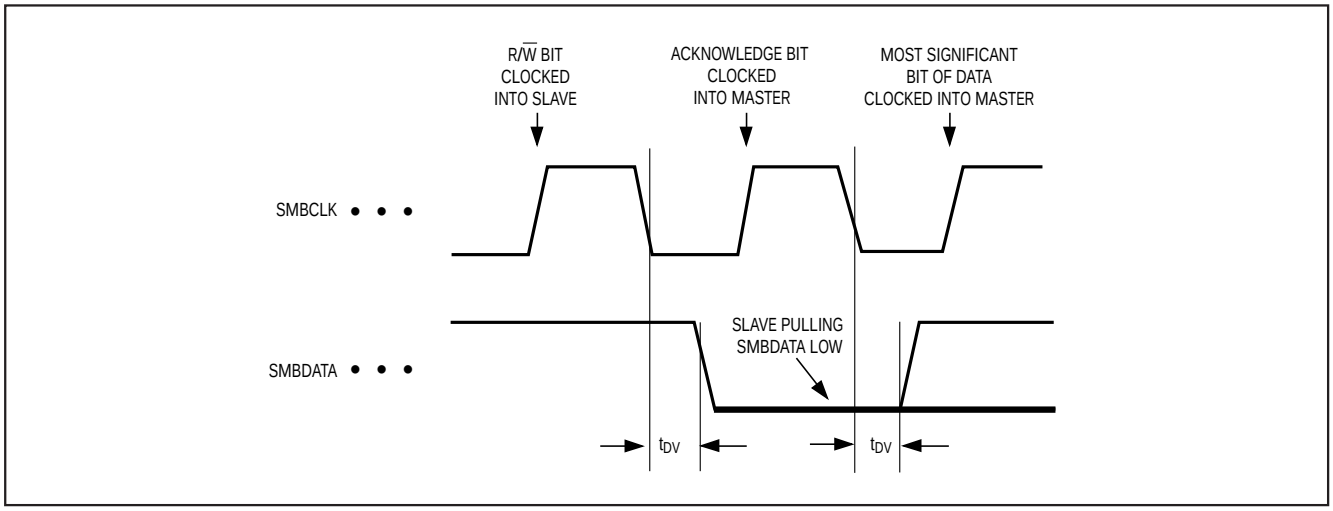


Figure 3. SMB Serial-Interface Timing—Acknowledge and Data Valid

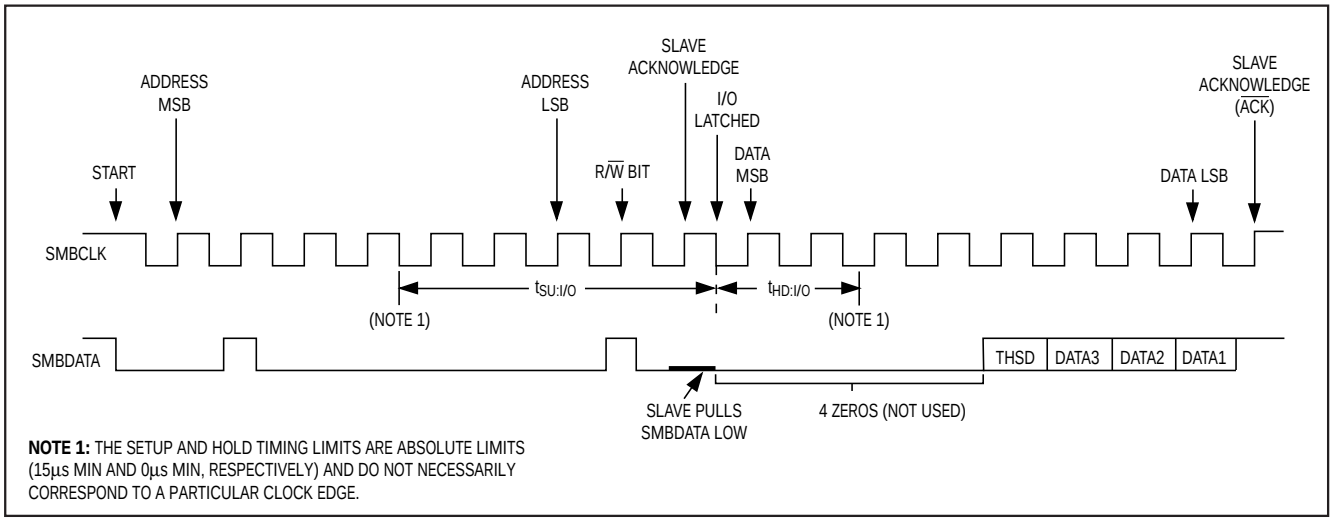


Figure 4. I/O Read Timing Diagram

rupt, the host (Bus Master) interrogates the bus slave devices via a special receive-byte operation that includes the alert response address. The data returned by this receive-byte operation is the address of the offending slave device. The interrupt pointer address can activate several different slave devices simultaneously. If more than one slave attempts to respond, bus arbitration rules apply, with the lowest address code going first. The other device(s) will not generate an acknowledge and will continue to hold the $\overline{ALERT}$ line low or repeat the START-STOP interrupt until serviced.

Clearing Interrupts via Alert Response

When a fault occurs, $\overline{ALERT}$ asserts and latches low. If the fault is momentary and disappears before the device is serviced, $\overline{ALERT}$ remains asserted. Normally, the master sends out the Alert Response address followed by a read bit (00011001). $\overline{ALERT}$ clears when the device responds by successfully putting its address on the bus. **Reading the Alert Response address is the *only* method for clearing hardware and software interrupt latches.** Clearing the interrupt has no effect on the state of the status registers.

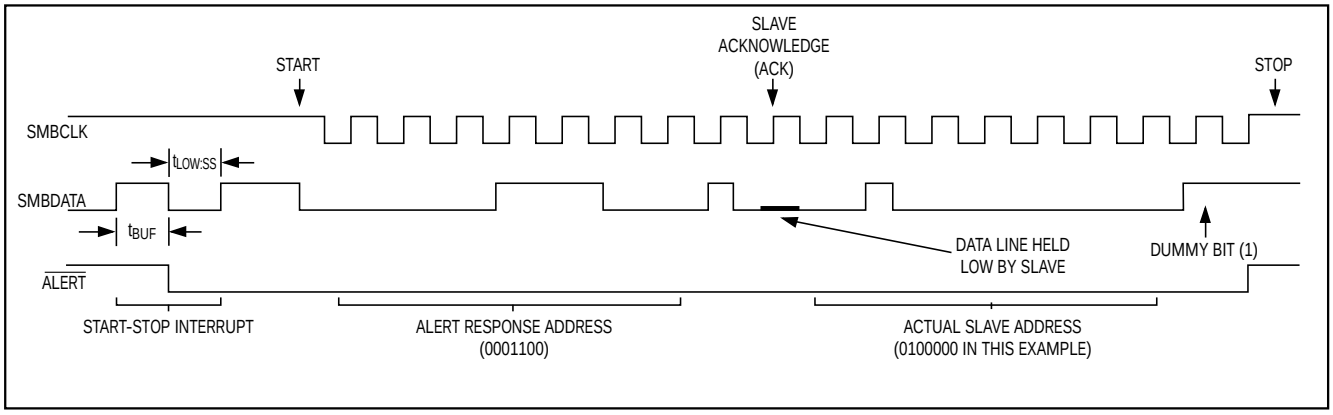


Figure 5. START-STOP Software Interrupt Timing Diagram and Alert Response

START-STOP Software Interrupt

The START-STOP interrupt is a method for the slave device to initiate a signal over the 2-wire interface without the need for a third (interrupt) wire. A START-STOP interrupt is a start condition followed by a stop condition; in other words, SMBDATA goes low and then high with SMBCLK high (Figure 5 shows the START-STOP interrupt and a subsequent Alert Response transmission used to clear the interrupt). The START-STOP function can be disabled (masked) by setting the data register mask SS (bit 6) high.

In order to avoid bus collisions, the START-STOP interrupt will not occur when the bus is busy. If the device begins a start condition simultaneously with another transmitter on the bus, it recognizes the falling SMBCLK as a collision and re-transmits the interrupt when the bus becomes available. Upon thermal shutdown or a transition on an I/O line, the device issues only one START-STOP interrupt, and won't repeat it unless there has been a collision. However, thermal-shutdown faults, not being edge triggered, may result in a continuous stream of START-STOP bits.

Input/Output Pins

Each input/output (I/O) is protected by an internal 20mA (typical) current-limit circuit. The I/O current limit depends on the supply voltage and the voltage applied to the I/O pins (see *Typical Operating Characteristics*). The typical I/O bias current is 0.5µA to $V_{I/O\_}$ = 28V.

The ability of the I/Os to sink current depends on V_{CC} as well as the voltage on the I/O. Typical pull-down on-resistance at V_{CC} = 2.7V and 5.5V is 106Ω and 66Ω, respectively. I/O source and sink capability can affect the rise and fall times of external power MOSFETs commonly used in power-switching applications. Other factors include the V_{GS}, the input capacitance of the MOSFET, and the pull-up resistor value used in the circuit. Typical MOSFET gate capacitance ranges from 150pF to 2000pF. Increasing the RC time constant slows down the MOSFET's response, but provides for a smoother transition.

Power-On Reset

The power-on reset circuit keeps the external MOSFETs off during a power-up sequence. When the supply voltage falls below the power-on reset threshold voltage, the MAX1662/MAX1663's outputs reset to a high-impedance state, and the MAX1661's outputs reset to a low state. During the initial power-up sequence, as V_{CC} increases, the $\overline{ALERT}$ pin goes low and then high, which indicates the device is powered on. The time between the low and high state on $\overline{ALERT}$ is the power-on delay time. Below V_{CC} = 0.8V (typical) the POR states can't be enforced, and the I/O pins of all versions exhibit increasingly weak pull-down current capability, eventually becoming high impedance.

Thermal Shutdown

These devices have internal thermal-shutdown circuitry that turns off all output stages (I/O pins) when the junction temperature exceeds +140°C typical. Thermal shutdown only occurs during an overload condition on the I/O pins. The device cycles between thermal shutdown and the overcurrent condition until the overload condition is removed. This could cause a sustained START-STOP interrupt and, in the extreme case, tie up the master controller. However, the device asserts $\overline{ALERT}$ low, indicating this fault status.

Applications Information

Bypassing and Grounding Considerations

Voltage transients exceeding 500mV at 25V/µs may trigger a false interrupt and thermal-shutdown indication. If large V_{CC} transients are expected, add a 100Ω resistor in series with V_{CC}. Retain the 0.1µF capacitor from V_{CC} to GND to act as a filter.

P-Channel/N-Channel Load Switch with Controlled Turn-On

For a more controlled voltage-switching application, add a series resistor to slow the switch turn-on time. The external MOSFET gate has typical capacitance of 150pF to 2000pF, but an optional external capacitance can be added to further slow the switching time (Figure 6).

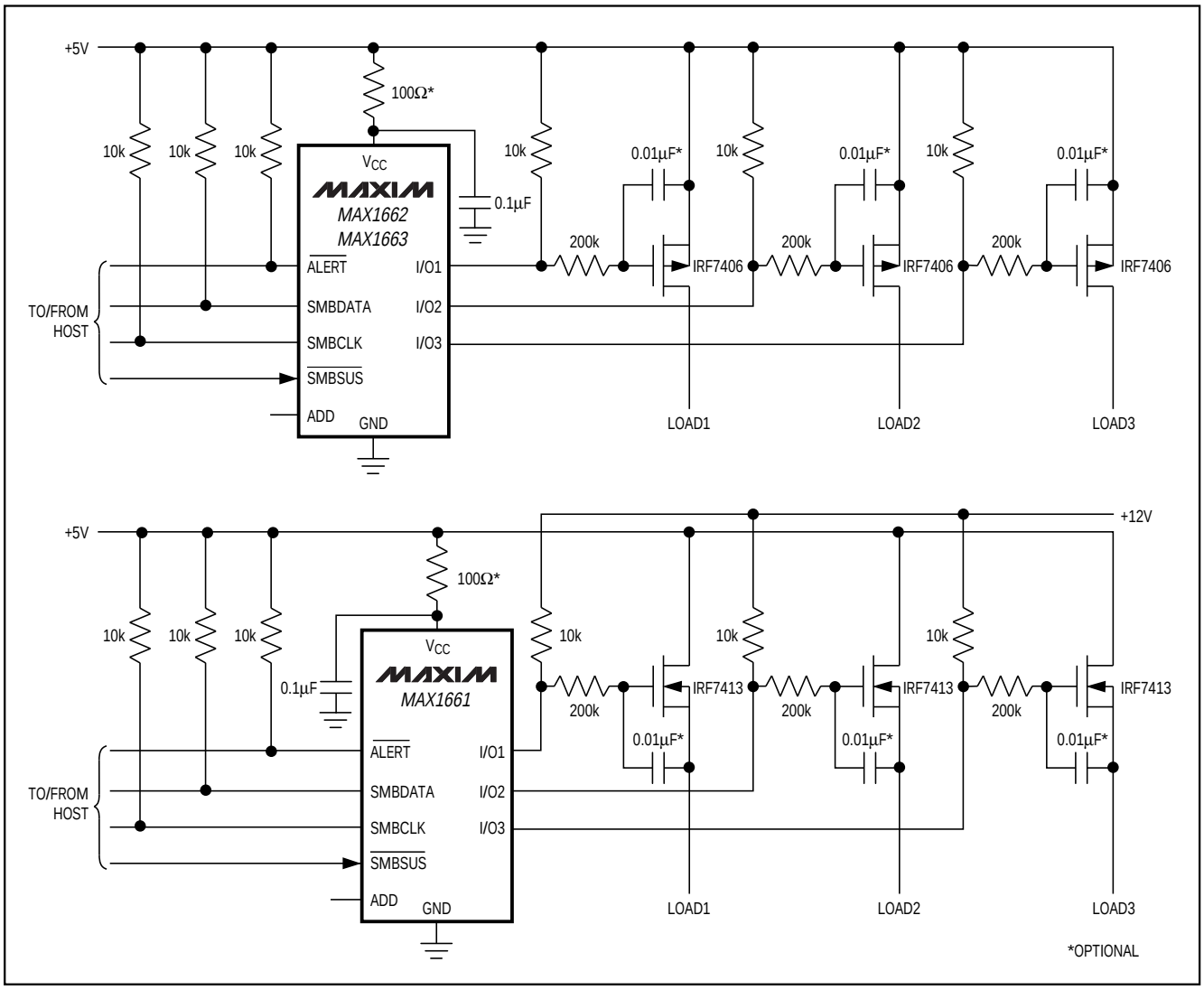


Figure 6. Load Switch with Controlled Turn-On

Serial-to-Parallel/Parallel-to-Serial Converters and Load-Switch Controllers with SMBus Interface

Battery Switch with Back-to-Back MOSFETs

For battery-operated applications, use back-to-back MOSFETs to keep reverse currents from flowing from the load to the supply (Figure 7). This protects the battery from potential damage, and isolates the load from the power source.

LED Drivers

A MAX1661/MAX1662/MAX1663 can be used as a programmable LED driver (Figure 8). With their low quiescent current, these devices are ideal for use as indicator light drivers on the front panel of a notebook computer.

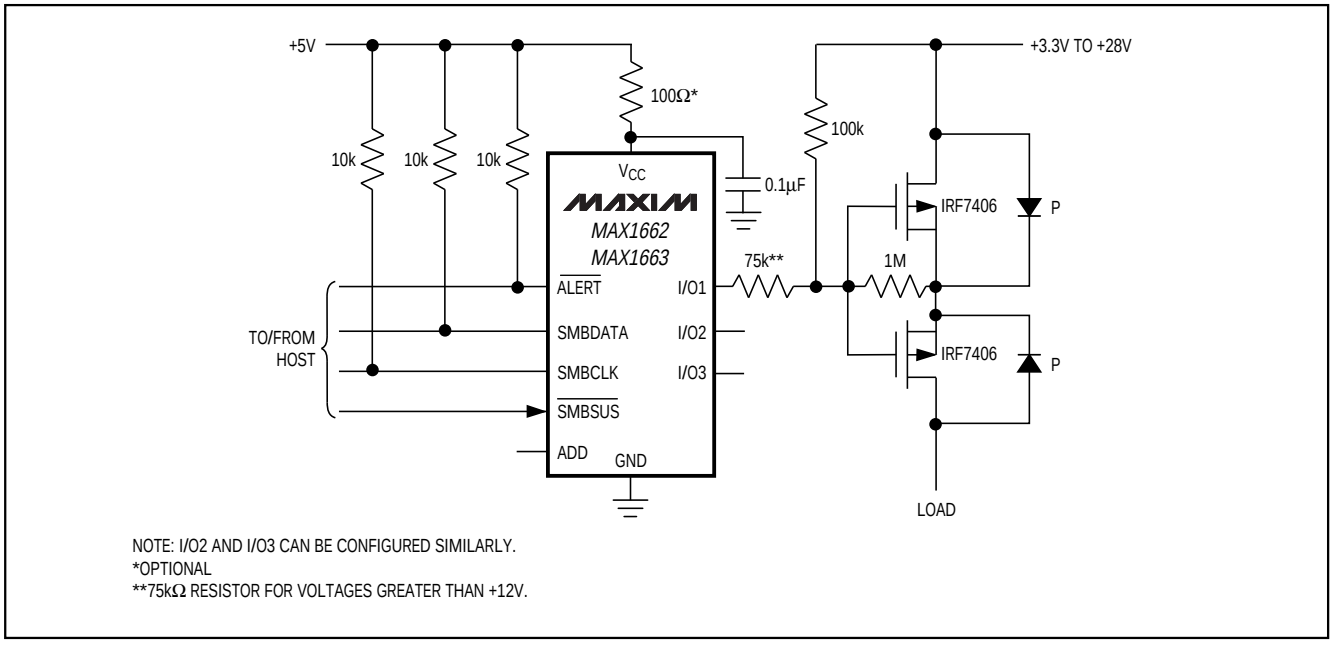


Figure 7. Battery Switch with Back-to-Back MOSFETs

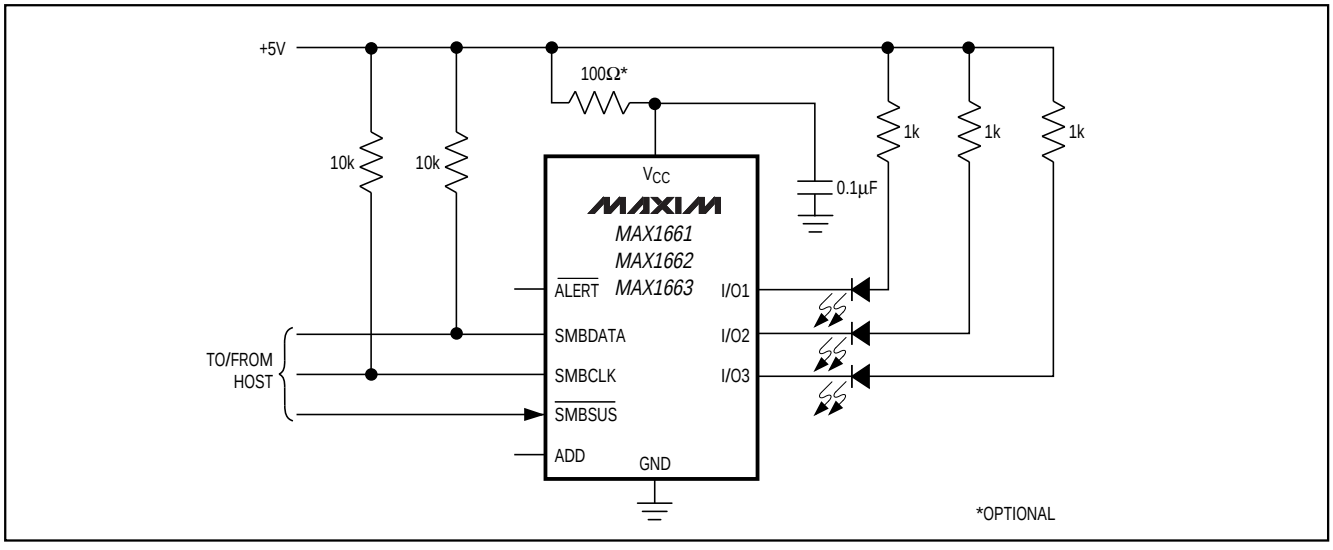


Figure 8. LED Drivers

Mechanical Switch Monitor

The ability of the MAX1661/MAX1662/MAX1663 to read back the logic state of the I/Os makes them suitable for checking system status. They can be used as an "open-lid indicator", sensing a change in the I/O and sending an interrupt to the master to indicate a change in status (Figure 9). The same can be done to detect a chassis intrusion.

Simple High-Voltage Switch

For applications requiring a higher voltage, use a simple resistive divider to protect the gate from breakdown yet allow the MOSFETs to handle higher-voltage applications (Figure 10).

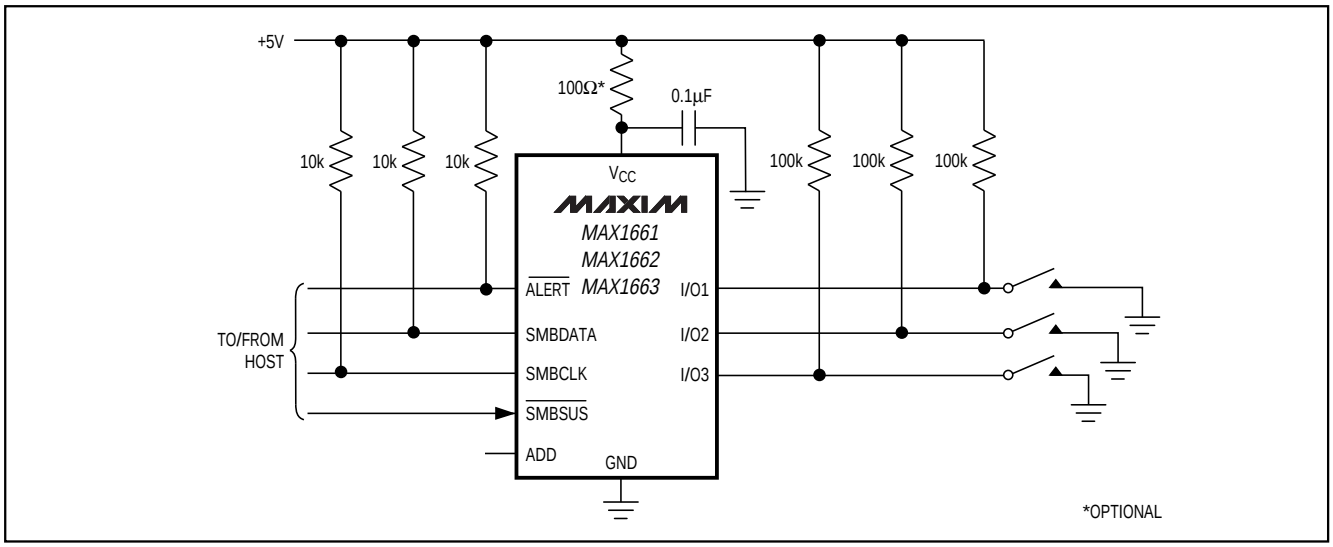


Figure 9. Open-Lid Detect or Chassis Intrusion Detector

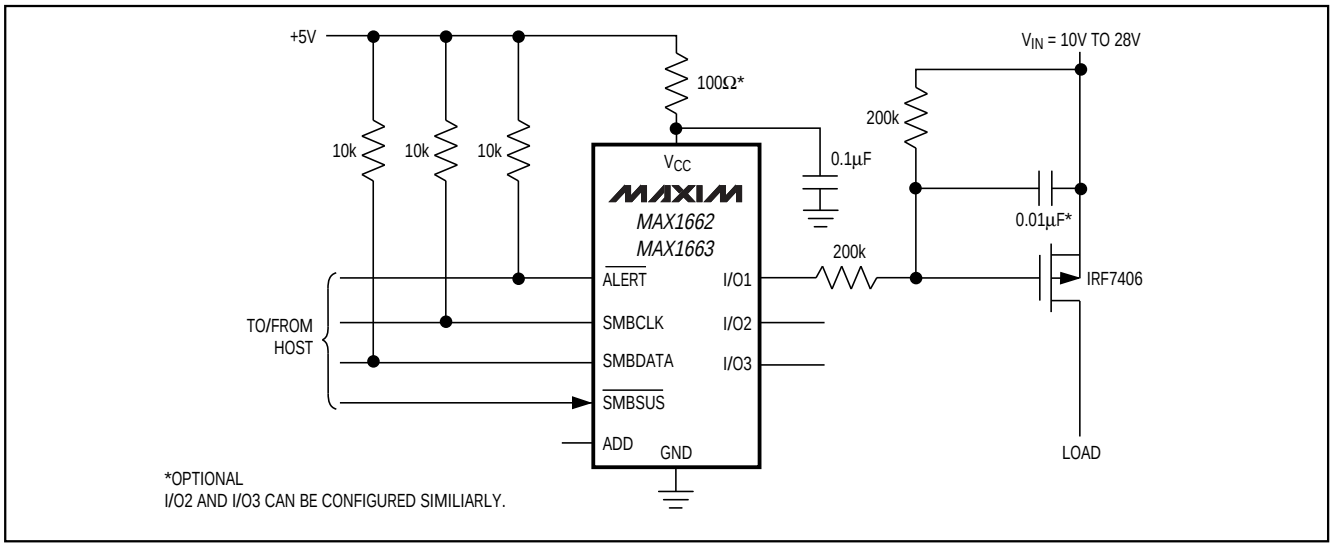
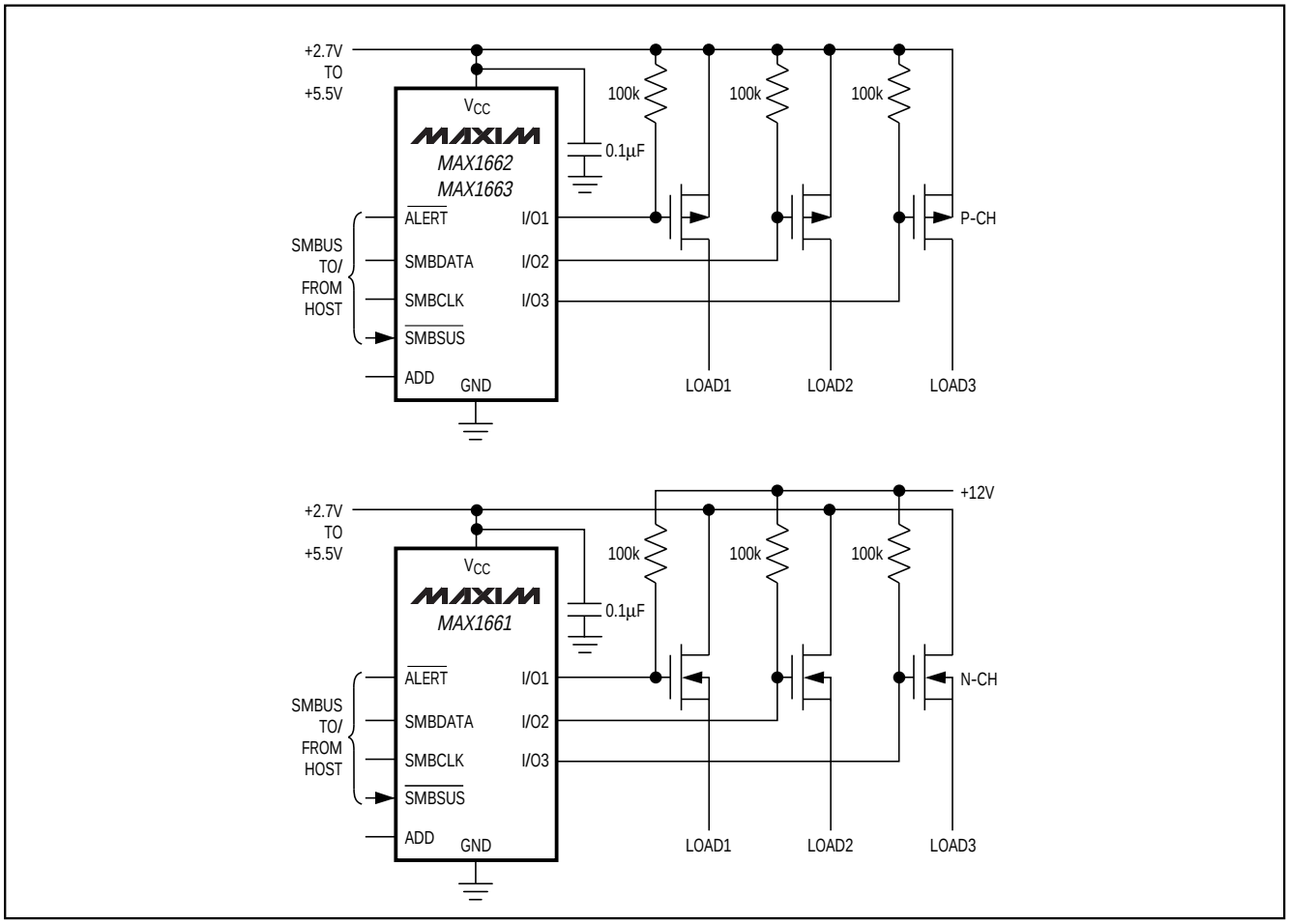


Figure 10. Simple High-Voltage Switch

Serial-to-Parallel/Parallel-to-Serial Converters and Load-Switch Controllers with SMBus Interface

Typical Operating Circuit



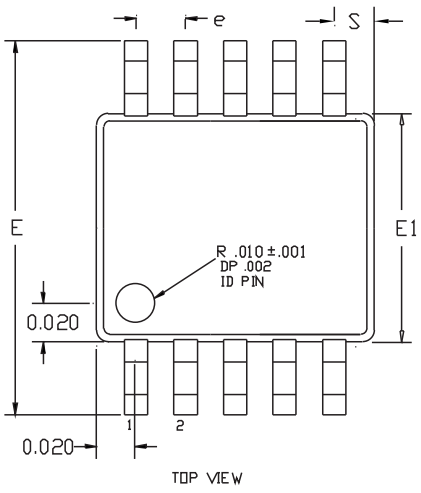
Chip Information

TRANSISTOR COUNT: 3334

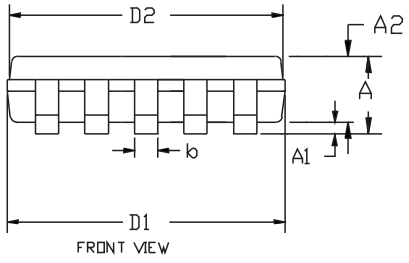
SUBSTRATE CONNECTED TO GND

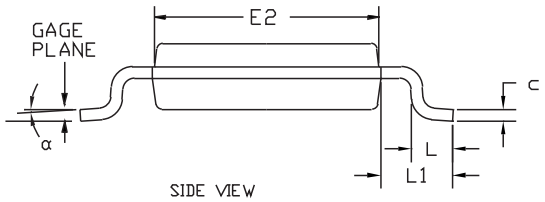
Package Information

10LUMAXB.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.037	0.043	0.939	1.092
A1	0.002	0.006	0.051	0.152
A2	0.030	0.038	0.762	0.965
D1	0.112	0.124	2.845	3.150
D2	0.110	0.122	2.794	3.099
E1	0.112	0.124	2.845	3.150
E2	0.110	0.122	2.794	3.099
E	0.185	0.201	4.699	5.105
L	0.0155	0.0275	0.394	0.699
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, 10L MICRO MAX

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0061	B	1/1

NOTES

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX708RESA+ MAX708SCSA+ MAX708SESA+ MAX708TCSA+ MAX708TEPA+ MAX708TESA+ MAX708TCUA+T MAX706AREPA+ MAX706ARESA+ MAX706ARESA+T MAX706AREUA+ MAX706AREUA+T MAX706ASEPA+ MAX706ASESA+ MAX706ASESA+T MAX706ASEUA+ MAX706ASEUA+T MAX706ATEPA+ MAX706ATESA+ MAX706ATESA+T MAX706ATEUA+ MAX706ATEUA+T MAX708RCPA+ MAX708RCSA+ MAX708RCSA+T MAX708RCUA+ MAX708RCUA+T MAX708RESA+T MAX708REUA+ MAX708REUA+T MAX708SCSA+T MAX708SCUA+ MAX708SCUA+T MAX708SESA+T MAX708TCPA+ MAX708TCSA+T MAX708TCUA+ MAX706APEPA+ MAX706APESA+ MAX706APESA+T MAX706APEUA+ MAX706APEUA+T MAX708REPA MAX708RMJA MAX708TMJA 5962-9326703MPA 5962-9312502MEA 5962-9312501MEA MAX708SEUA+T MAX708RESA MAX19538ETL+ MAX19538ETL+T 5962-9326704M2C