

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND.....	-0.3V to 6V	Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
AGND to DGND.....	-0.3V to 0.3V	Plastic DIP (derate 11.11mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	889mW
CH0–CH7, COM to AGND, DGND	-0.3V to ($V_{DD} + 0.3\text{V}$)	SSOP (derate 8.00mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	640mW
VREF, REFADJ to AGND	-0.3V to ($V_{DD} + 0.3\text{V}$)	CERDIP (derate 11.11mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....	889mW
Digital Inputs to DGND	-0.3V to 6V	Operating Temperature Ranges	
Digital Outputs to DGND	-0.3V to ($V_{DD} + 0.3\text{V}$)	MAX146_C_P/MAX147_C_P	0°C to $+70^\circ\text{C}$
Digital Output Sink Current	25mA	MAX146_E_P/MAX147_E_P	-40°C to $+85^\circ\text{C}$
		MAX146_MJP/MAX147_MJP	-55°C to $+125^\circ\text{C}$
		Storage Temperature Range	-60°C to $+150^\circ\text{C}$
		Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = +2.7\text{V}$ to $+3.6\text{V}$ (MAX146); $V_{DD} = +2.7\text{V}$ to $+5.25\text{V}$ (MAX147); COM = 0; $f_{SCLK} = 2.0\text{MHz}$; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX146—4.7 μF capacitor at VREF pin; MAX147—external reference, VREF = 2.500V applied to VREF pin; $T_A = T_{MIN}$ to T_{MAX} ; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL	MAX14_A			± 0.5	LSB
		MAX14_B			± 1.0	
		MAX147C			± 2.0	
No Missing Codes	NMC		12			Bits
Differential Nonlinearity	DNL	MAX14_A/MAX14_B			± 1.0	LSB
		MAX147C			± 0.8	
Offset Error		MAX14_A			± 0.5 ± 3	LSB
		MAX14_B/MAX147C			± 0.5 ± 4	
Gain Error (Note 3)					± 0.5 ± 4	LSB
Gain Temperature Coefficient					± 0.25	ppm/ $^\circ\text{C}$
Channel-to-Channel Offset Matching					± 0.25	LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500V _{p-p} , 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD	MAX14_A/MAX14_B		70	73	dB
		MAX147C			73	
Total Harmonic Distortion	THD	Up to the 5th harmonic	MAX14_A/MAX14_B		-88 -80	dB
			MAX147C			
Spurious-Free Dynamic Range	SFDR	MAX14_A/MAX14_B		80	90	dB
		MAX147C			90	
Channel-to-Channel Crosstalk		65kHz, 2.500V _{p-p} (Note 4)			-85	dB
Small-Signal Bandwidth		-3dB rolloff			2.25	MHz
Full-Power Bandwidth					1.0	MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{\text{SHDN}} = \text{FLOAT}$		5.5	7.5	μs
		Internal clock, $\overline{\text{SHDN}} = V_{DD}$		35	65	
		External clock = 2MHz, 12 clocks/conversion		6		

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MAX146/MAX147

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.7V$ to $+3.6V$ (MAX146); $V_{DD} = +2.7V$ to $+5.25V$ (MAX147); $COM = 0$; $f_{SCLK} = 2.0MHz$; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX146— $4.7\mu F$ capacitor at VREF pin; MAX147—external reference, VREF = 2.500V applied to VREF pin; $T_A = T_{MIN}$ to T_{MAX} ; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Track/Hold Acquisition Time	t_{ACQ}				1.5	μs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN} = \text{FLOAT}$		1.8		MHz
		$\overline{SHDN} = V_{DD}$		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, $COM = 0V$			0 to VREF	V
		Bipolar, $COM = V_{REF} / 2$			$\pm V_{REF} / 2$	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_} = 0V$ or V_{DD}		± 0.01	± 1	μA
Input Capacitance				16		pF
INTERNAL REFERENCE (MAX146 only, reference buffer enabled)						
VREF Output Voltage		$T_A = +25^\circ C$	2.480	2.500	2.520	V
VREF Short-Circuit Current					30	mA
VREF Temperature Coefficient		MAX146_C		± 30	± 50	ppm/ $^\circ C$
		MAX146_E		± 30	± 60	
		MAX146_M		± 30	± 80	
Load Regulation (Note 7)		0 to 0.2mA output load		0.35		mV
Capacitive Bypass at VREF		Internal compensation mode		0		μF
		External compensation mode		4.7		
Capacitive Bypass at REFADJ				0.047		μF
REFADJ Adjustment Range				± 1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled)						
VREF Input Voltage Range (Note 8)			1.0		$V_{DD} + 50mV$	V
VREF Input Current		VREF = 2.5V		100	150	μA
VREF Input Resistance			18	25		k Ω
Shutdown VREF Input Current				0.01	10	μA
REFADJ Buffer Disable Threshold			$V_{DD} - 0.5$			V
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode		0		μF
		External compensation mode		4.7		
Reference Buffer Gain		MAX146		2.06		V/V
		MAX147		2.00		
REFADJ Input Current		MAX146			± 50	μA
		MAX147			± 10	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.7V$ to $+3.6V$ (MAX146); $V_{DD} = +2.7V$ to $+5.25V$ (MAX147); $COM = 0$; $f_{SCLK} = 2.0MHz$; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksp/s); MAX146— $4.7\mu F$ capacitor at VREF pin; MAX147—external reference, VREF = 2.500V applied to VREF pin; $T_A = T_{MIN}$ to T_{MAX} ; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
DIGITAL INPUTS (DIN, SCLK, \overline{CS} , SHDN)							
DIN, SCLK, \overline{CS} Input High Voltage	V_{IH}	$V_{DD} \leq 3.6V$	2.0			V	
		$V_{DD} > 3.6V$, MAX147 only	3.0				
DIN, SCLK, \overline{CS} Input Low Voltage	V_{IL}				0.8	V	
DIN, SCLK, \overline{CS} Input Hysteresis	V_{HYST}			0.2		V	
DIN, SCLK, \overline{CS} Input Leakage	I_{IN}	$V_{IN} = 0V$ or V_{DD}		± 0.01	± 1	μA	
DIN, SCLK, \overline{CS} Input Capacitance	C_{IN}	(Note 9)			15	pF	
\overline{SHDN} Input High Voltage	V_{SH}		$V_{DD} - 0.4$			V	
\overline{SHDN} Input Mid Voltage	V_{SM}		1.1	$V_{DD} - 1.1$		V	
\overline{SHDN} Input Low Voltage	V_{SL}				0.4	V	
\overline{SHDN} Input Current	I_S	SHDN = 0V or V_{DD}			± 4.0	μA	
\overline{SHDN} Voltage, Floating	V_{FLT}	SHDN = FLOAT		$V_{DD} / 2$		V	
\overline{SHDN} Maximum Allowed Leakage, Mid Input		SHDN = FLOAT			± 100	nA	
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	$I_{SINK} = 5mA$			0.4	V	
		$I_{SINK} = 16mA$			0.8		
Output Voltage High	V_{OH}	$I_{SOURCE} = 0.5mA$	$V_{DD} - 0.5$			V	
Three-State Leakage Current	I_L	$\overline{CS} = V_{DD}$		± 0.01	± 10	μA	
Three-State Output Capacitance	C_{OUT}	$\overline{CS} = V_{DD}$ (Note 9)			15	pF	
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	MAX146	2.70		3.60	V	
		MAX147	2.70		5.25		
Positive Supply Current, MAX146	I_{DD}	$V_{DD} = 3.6V$	Operating mode, full-scale input		1.2	2.0	mA
			Fast power-down		30	70	μA
			Full power-down		1.2	10	
Positive Supply Current, MAX147	I_{DD}	Operating mode, full-scale input	$V_{DD} = 5.25V$		1.8	2.5	mA
			$V_{DD} = 3.6V$		0.9	1.5	
Positive Supply Current, MAX147	I_{DD}	Full power-down	$V_{DD} = 5.25V$		2.1	15	μA
			$V_{DD} = 3.6V$		1.2	10	
Supply Rejection (Note 10)	PSR	Full-scale input, external reference = 2.5V, $V_{DD} = 2.7V$ to $V_{DD}(MAX)$		± 0.3		mV	

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MAX146/MAX147

TIMING CHARACTERISTICS

($V_{DD} = +2.7V$ to $+3.6V$ (MAX146); $V_{DD} = +2.7V$ to $+5.25V$ (MAX147); $T_A = T_{MIN}$ to T_{MAX} ; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			μs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}			0			ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	MAX14_ _C/E	20		200	ns
			MAX14_ _M	20		240	
\overline{CS} Fall to Output Enable	t_{DV}	Figure 1				240	ns
\overline{CS} Rise to Output Disable	t_{TR}	Figure 2				240	ns
\overline{CS} to SCLK Rise Setup	t_{CSS}			100			ns
\overline{CS} to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
\overline{CS} Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
\overline{CS} Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 9)		0			ns

Note 1: Tested at $V_{DD} = 2.7V$; $COM = 0$; unipolar single-ended input mode.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

Note 3: MAX146—internal reference, offset nulled; MAX147—external reference ($V_{REF} = +2.5V$), offset nulled.

Note 4: Ground “on” channel; sine wave applied to all “off” channels.

Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.

Note 6: The common-mode range for the analog inputs is from AGND to V_{DD} .

Note 7: External load should not change during conversion for specified accuracy.

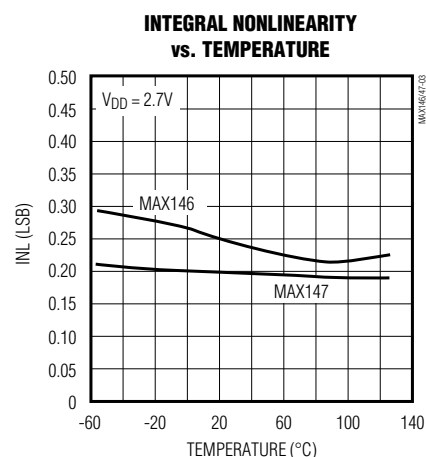
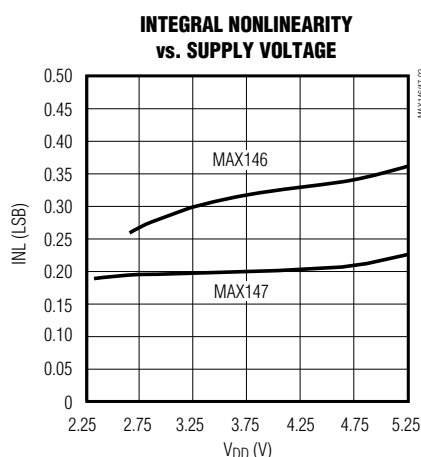
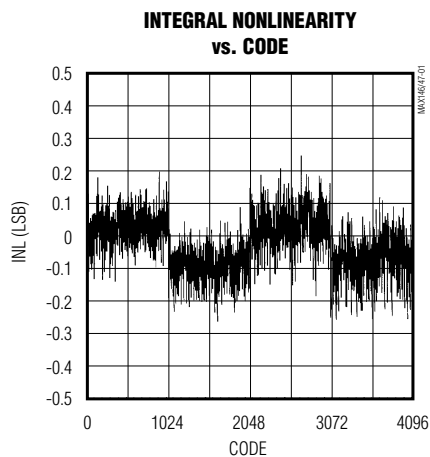
Note 8: ADC performance is limited by the converter’s noise floor, typically $300\mu V_{p-p}$.

Note 9: Guaranteed by design. Not subject to production testing.

Note 10: Measured as $|V_{FS}(2.7V) - V_{FS}(V_{DD, MAX})|$.

Typical Operating Characteristics

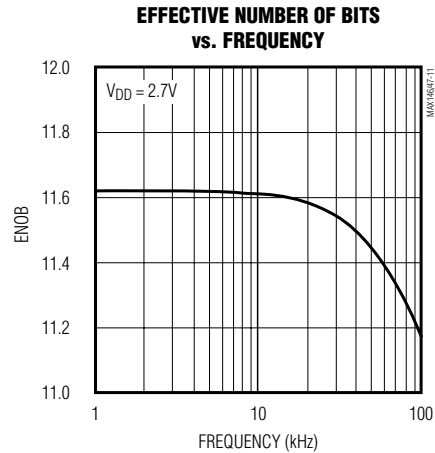
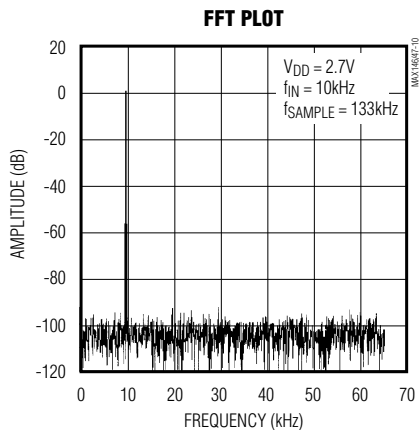
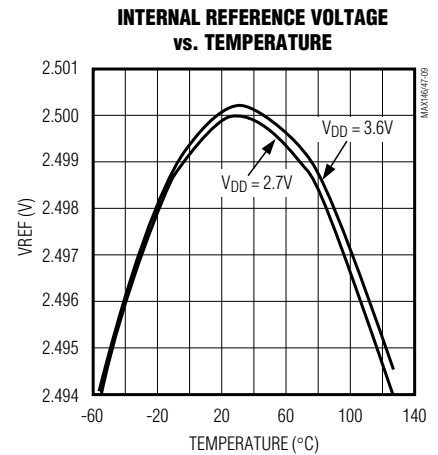
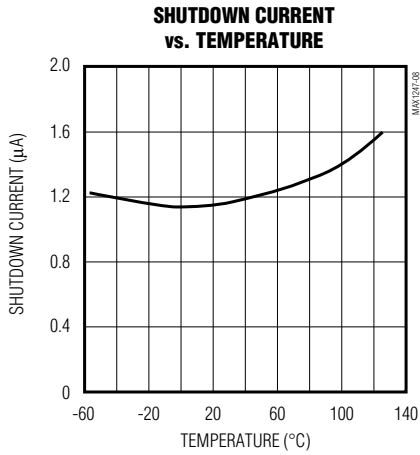
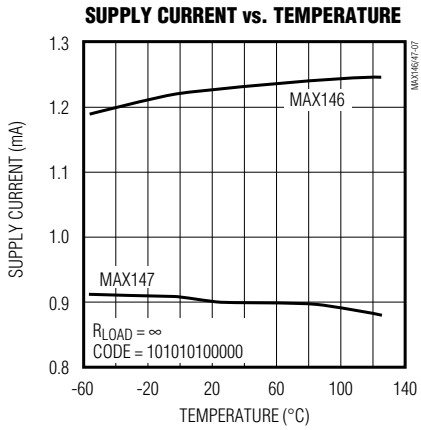
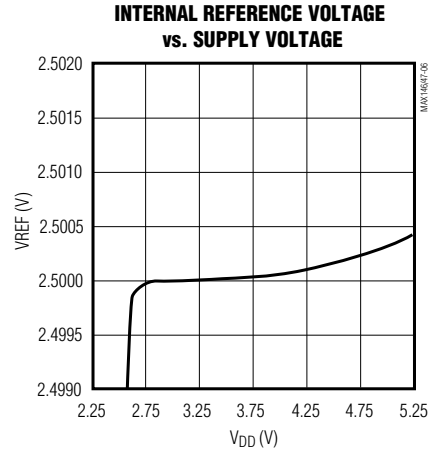
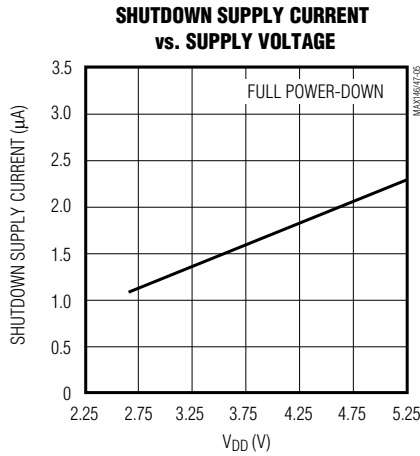
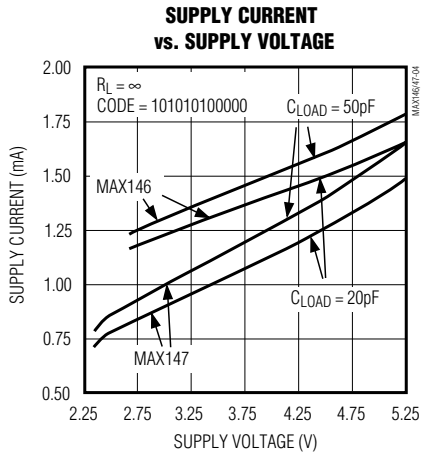
($V_{DD} = 3.0V$, $V_{REF} = 2.5V$, $f_{SCLK} = 2.0MHz$, $C_{LOAD} = 20pF$, $T_A = +25^\circ C$, unless otherwise noted.)



+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

Typical Operating Characteristics (continued)

($V_{DD} = 3.0V$, $V_{REF} = 2.5V$, $f_{SCLK} = 2.0MHz$, $C_{LOAD} = 20pF$, $T_A = +25^\circ C$, unless otherwise noted.)

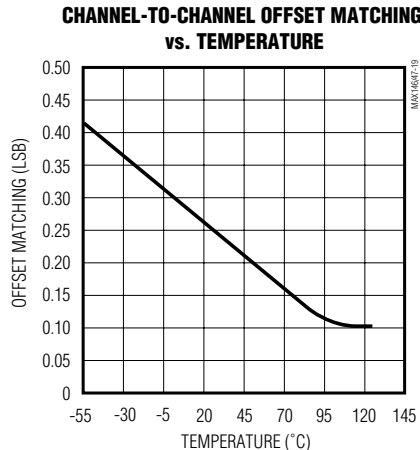
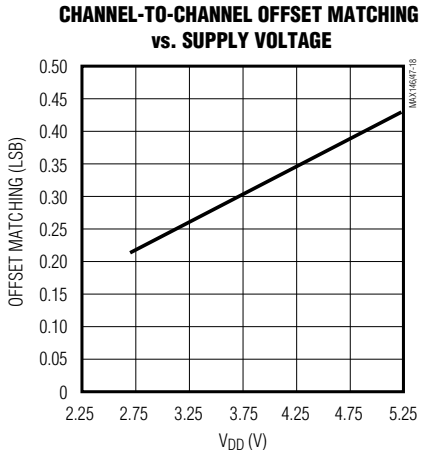
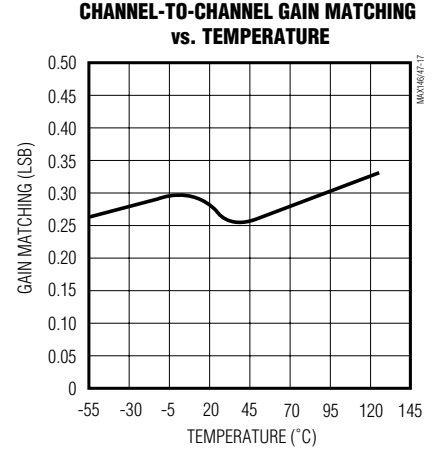
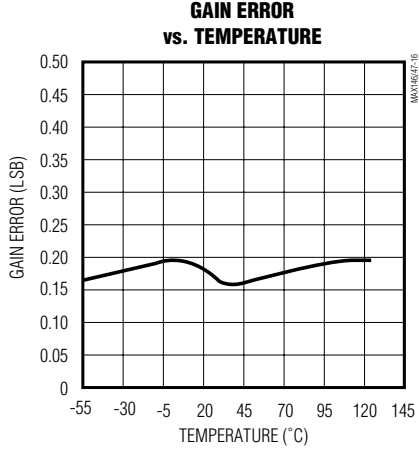
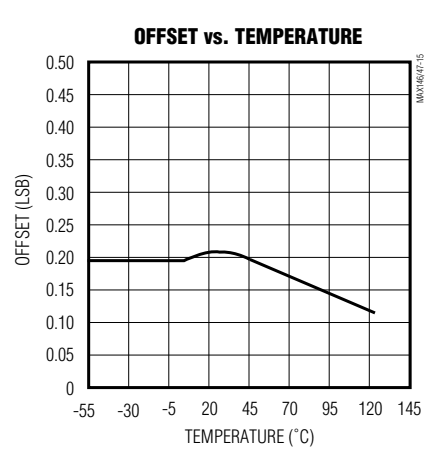
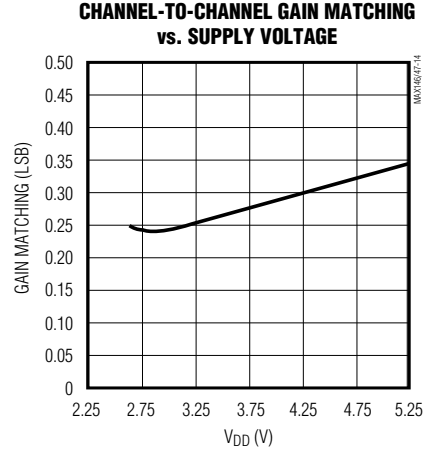
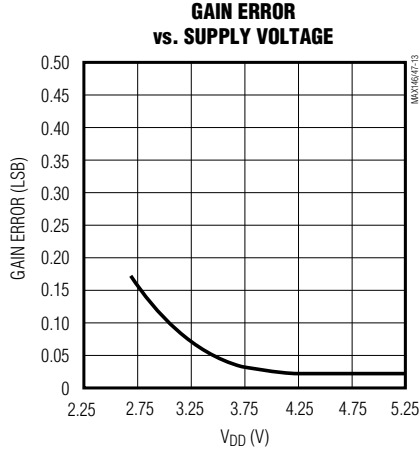
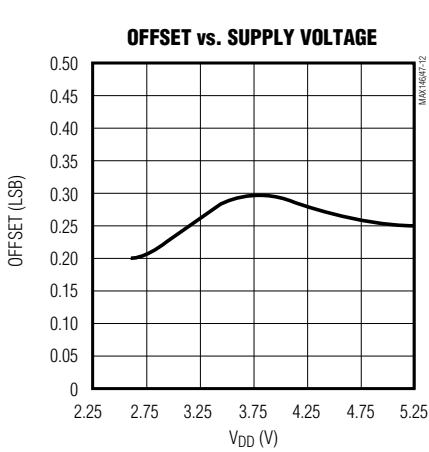


+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

MAX146/MAX147

Typical Operating Characteristics (continued)

($V_{DD} = 3.0V$, $V_{REF} = 2.5V$, $f_{SCLK} = 2.0MHz$, $C_{LOAD} = 20pF$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	COM	Ground reference for analog inputs. COM sets zero-code voltage in single-ended mode. Must be stable to $\pm 0.5\text{LSB}$.
10	$\overline{\text{SHDN}}$	Three-Level Shutdown Input. Pulling $\overline{\text{SHDN}}$ low shuts the MAX146/MAX147 down; otherwise, they are fully operational. Pulling $\overline{\text{SHDN}}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{\text{SHDN}}$ float puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode (MAX146 only), the reference buffer provides a 2.500V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD} .
12	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD} .
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{\text{CS}}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX146/MAX147 begin the A/D conversion, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{\text{CS}}$ is high (external clock mode).
17	DIN	Serial Data Input. Data is clocked in at SCLK's rising edge.
18	$\overline{\text{CS}}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)
20	V_{DD}	Positive Supply Voltage

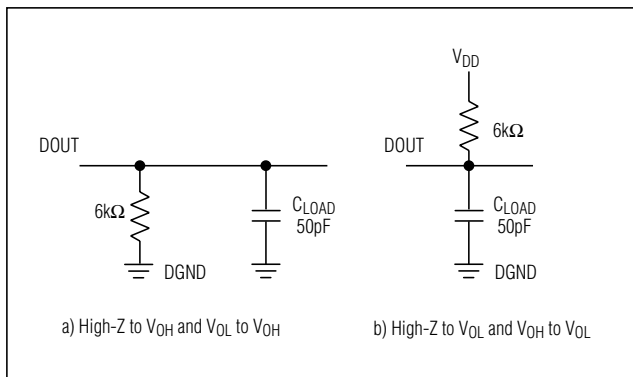


Figure 1. Load Circuits for Enable Time

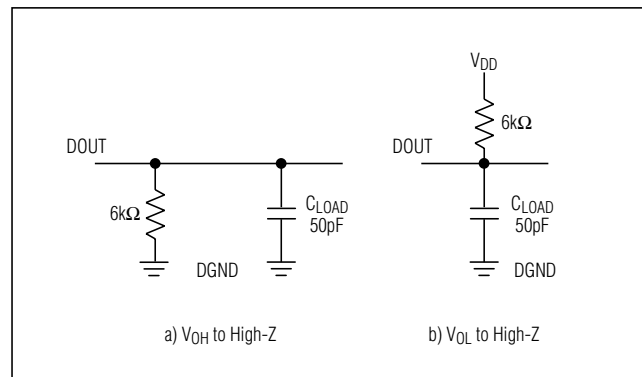


Figure 2. Load Circuits for Disable Time

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Detailed Description

The MAX146/MAX147 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (μ Ps). Figure 3 is a block diagram of the MAX146/MAX147.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, $IN+$ is internally switched to $CH0$ – $CH7$, and $IN-$ is switched to COM . In differential mode, $IN+$ and $IN-$ are selected from the following pairs: $CH0/CH1$, $CH2/CH3$, $CH4/CH5$, and $CH6/CH7$. Configure the channels with Tables 2 and 3.

In differential mode, $IN-$ and $IN+$ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at $IN+$ is sampled. The return side ($IN-$) must remain stable within $\pm 0.5LSB$ ($\pm 0.1LSB$ for best results) with respect to $AGND$ during a conversion. To accomplish this, connect a $0.1\mu F$ capacitor from $IN-$ (the selected analog input) to $AGND$.

During the acquisition interval, the channel selected as the positive input ($IN+$) charges capacitor C_{HOLD} . The acquisition interval spans three $SCLK$ cycles and ends

on the falling $SCLK$ edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at $IN+$.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input ($IN+$) to the negative input ($IN-$). In single-ended mode, $IN-$ is simply COM . This unbalances node $ZERO$ at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node $ZERO$ to $0V$ within the limits of 12-bit resolution. This action is equivalent to transferring a $16pF \times [(V_{IN+}) - (V_{IN-})]$ charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, $IN-$ is connected to COM , and the converter samples the "+" input. If the converter is set up for differential inputs, $IN-$ connects to the "-" input, and the difference of $|IN+ - IN-|$ is sampled. At the end of the conversion, the positive input connects back to $IN+$, and C_{HOLD} charges to the input signal.

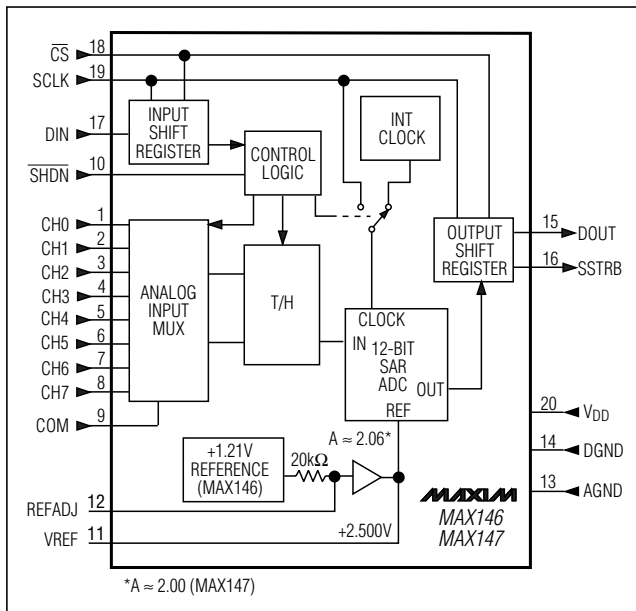


Figure 3. Block Diagram

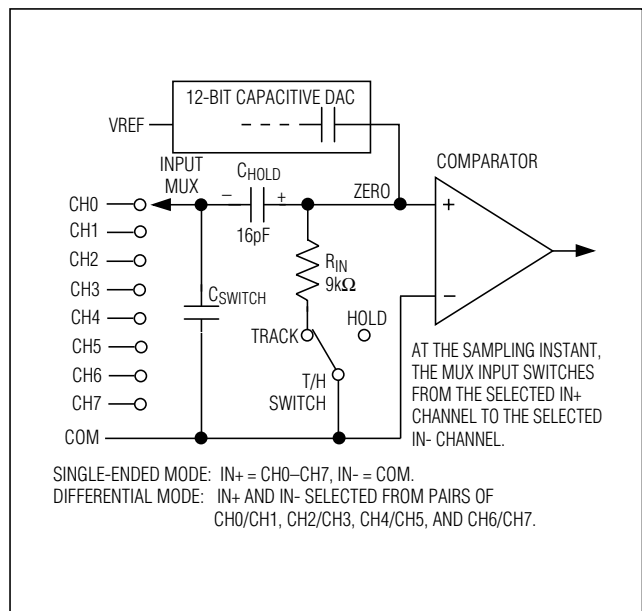


Figure 4. Equivalent Input Circuit

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The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ} , is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 16pF$$

where $R_{IN} = 9k\Omega$, R_S = the source impedance of the input signal, and t_{ACQ} is never less than $1.5\mu s$. Note that source impedances below $1k\Omega$ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a $0.01\mu F$ capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from $AGND - 0.3V$ to $V_{DD} + 0.3V$ without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.

Quick Look

To quickly evaluate the MAX146/MAX147's analog performance, use the circuit of Figure 5. The MAX146/MAX147 require a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds in control bytes of \$FF (HEX), which trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 will alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

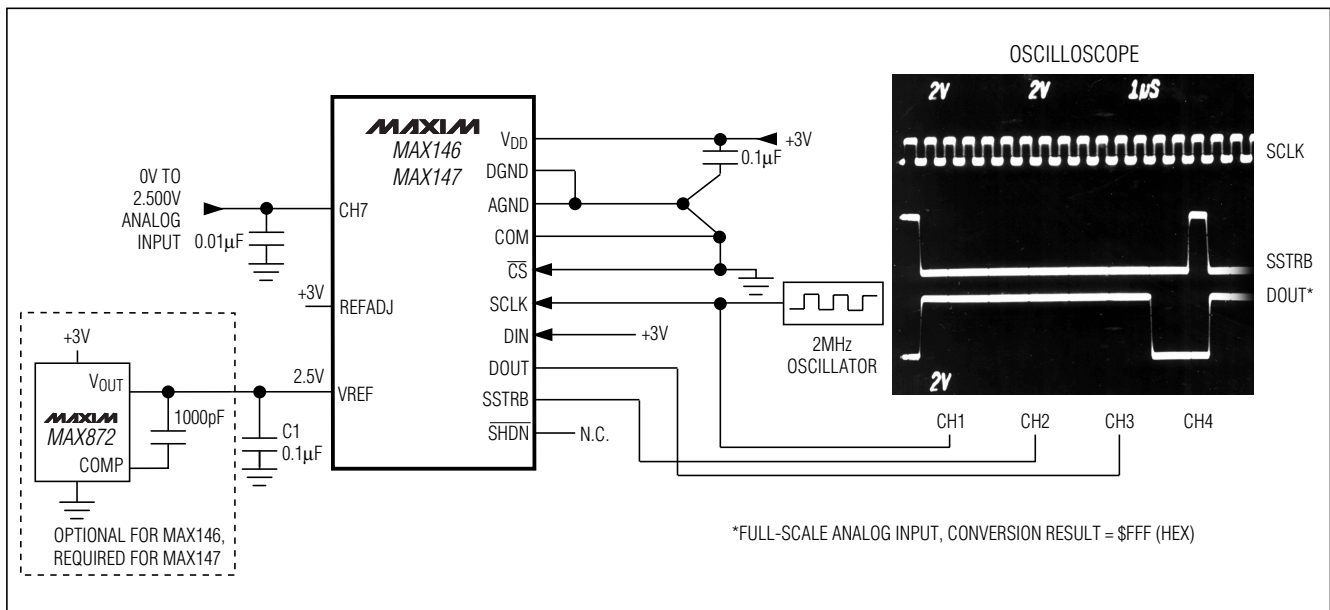


Figure 5. Quick-Look Circuit

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MAX146/MAX147

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/BIP	SGL/DIF	PD1	PD0
BIT	NAME	DESCRIPTION					
7(MSB)	START	The first logic "1" bit after \overline{CS} goes low defines the beginning of the control byte.					
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion (Tables 2 and 3).					
3	UNI/BIP	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.					
2	SGL/DIF	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).					
1 0(LSB)	PD1 PD0	Selects clock and power-down modes.					
		PD1	PD0	Mode			
		0	0	Full power-down			
		0	1	Fast power-down (MAX146 only)			
		1	0	Internal clock mode			
		1	1	External clock mode			

Table 2. Channel Selection in Single-Ended Mode (SGL/DIF = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								-
1	0	0		+							-
0	0	1			+						-
1	0	1				+					-
0	1	0					+				-
1	1	0						+			-
0	1	1							+		-
1	1	1								+	-

Table 3. Channel Selection in Differential Mode (SGL/DIF = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	-						
0	0	1			+	-				
0	1	0					+	-		
0	1	1							+	-
1	0	0	-	+						
1	0	1			-	+				
1	1	0					-	+		
1	1	1							-	+

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How to Start a Conversion

Start a conversion by clocking a control byte into DIN. With \overline{CS} low, each rising edge on SCLK clocks a bit from DIN into the MAX146/MAX147's internal shift register. After \overline{CS} falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX146/MAX147 are compatible with SPI™/QSPI™ and Microwire™ devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result). See Figure 20 for MAX146/MAX147 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

- 1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
- 2) Use a general-purpose I/O line on the CPU to pull \overline{CS} low.
- 3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.

- 4) Transmit a byte of all zeros (\$00 hex) and, simultaneously, receive byte RB2.
- 5) Transmit a byte of all zeros (\$00 hex) and, simultaneously, receive byte RB3.
- 6) Pull \overline{CS} high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion, padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120μs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 17). For bipolar input mode, the output is two's complement (Figure 18). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX146/MAX147 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX146/MAX147. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

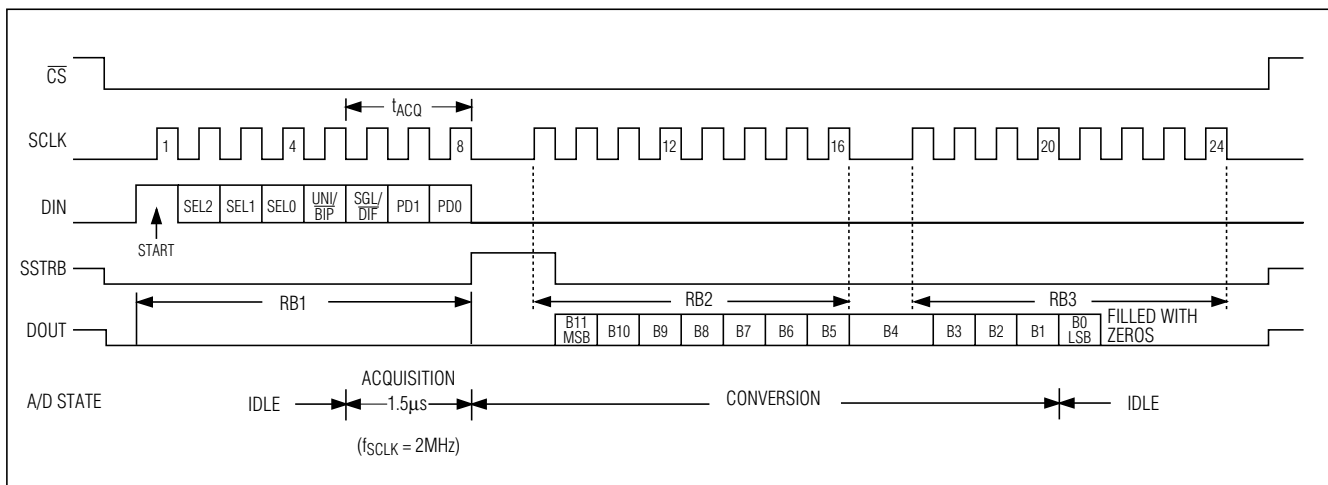


Figure 6. 24-Clock External Clock Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{SCLK} \leq 2\text{MHz}$)

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MAX146/MAX147

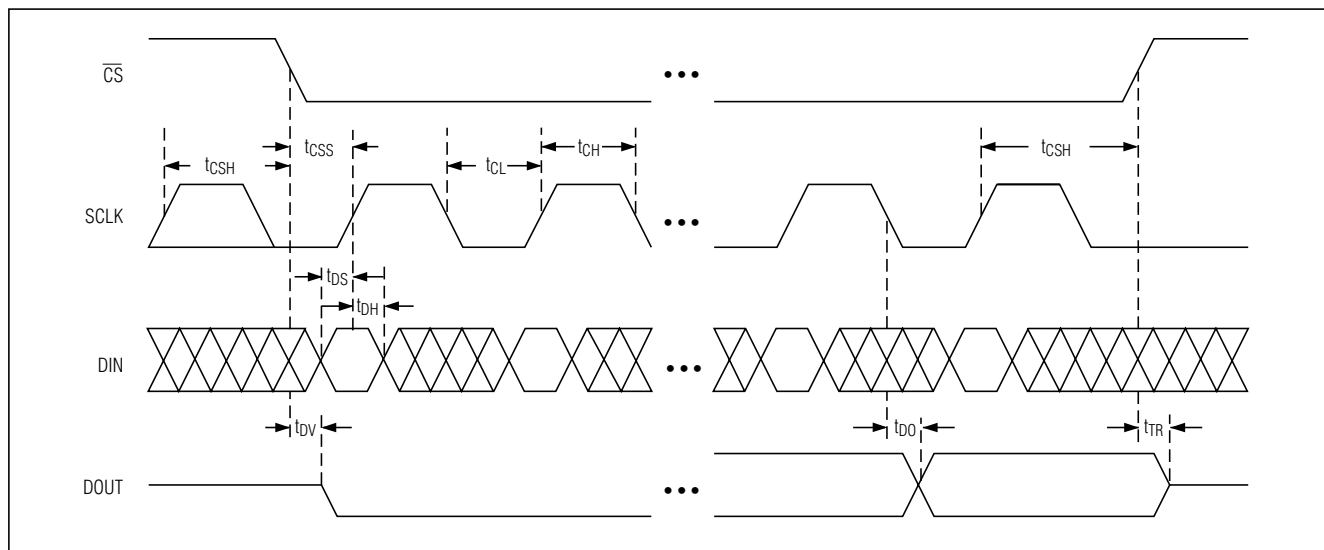


Figure 7. Detailed Serial-Interface Timing

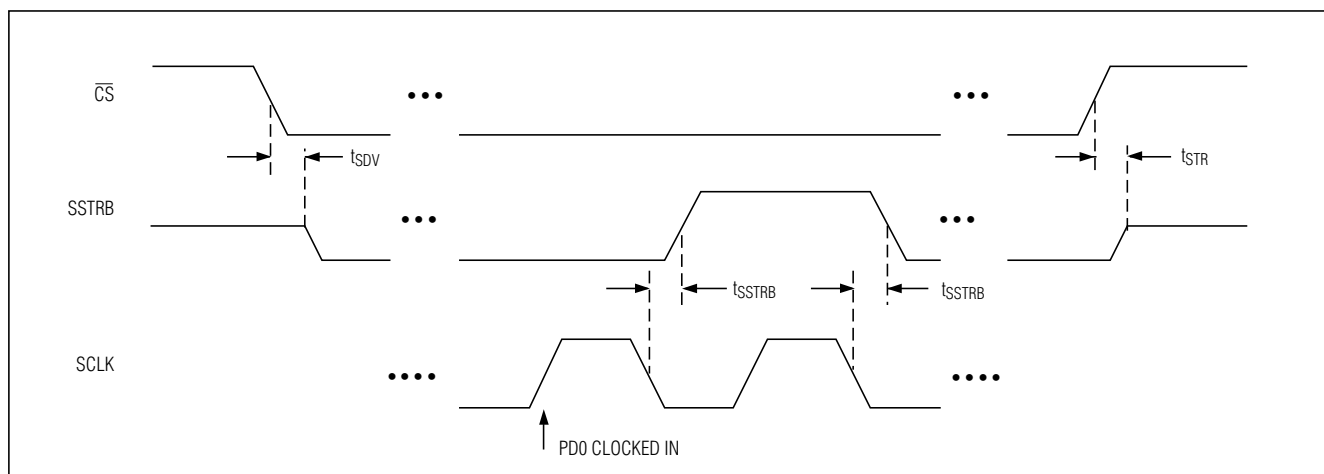


Figure 8. External Clock Mode SSTRB Detailed Timing

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when CS goes high; after the next CS falling edge, SSTRB outputs a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial clock interruptions could cause the conversion interval to exceed 120μs.

Internal Clock

In internal clock mode, the MAX146/MAX147 generate their own conversion clocks internally. This frees the μP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the

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processor's convenience, at any clock rate from 0MHz to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 7.5µs (SHDN = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). CS does

not need to be held low once a conversion is started. Pulling CS high prevents data from being clocked into the MAX146/MAX147 and three-states DOUT, but it does not adversely affect an internal clock mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when CS goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX146/MAX147 at clock rates exceeding 2.0MHz if the minimum acquisition time (t_{ACQ}) is kept above 1.5µs.

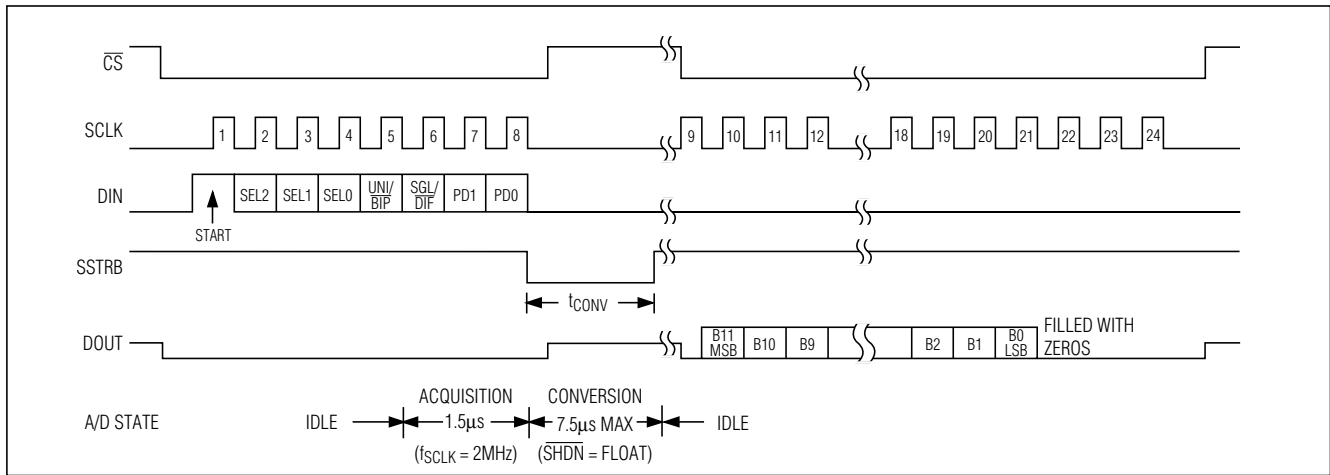


Figure 9. Internal Clock Mode Timing

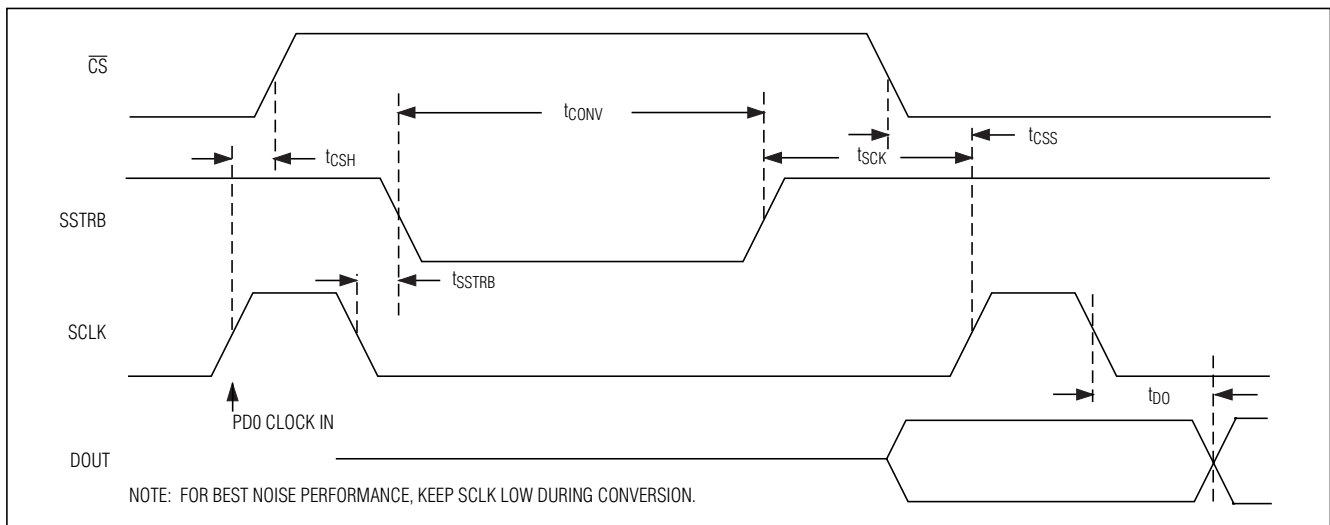


Figure 10. Internal Clock Mode SSTRB Detailed Timing

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Data Framing

The falling edge of \overline{CS} does **not** start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as follows:

The first high bit clocked into DIN with \overline{CS} low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If CS is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX146/MAX147 can run with \overline{CS} held low between conversions is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external

clock mode. If \overline{CS} is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (μ Cs) require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion is typically the fastest that a μ C can drive the MAX146/MAX147. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if \overline{SHDN} is not pulled low, internal power-on reset circuitry activates the MAX146/MAX147 in internal clock mode, ready to convert with SSTRB = high. After the power supplies stabilize, the internal reset time is 10 μ s, and no conversions should be performed during this phase. SSTRB is high on power-up and, if \overline{CS} is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. (Also see Table 4.)

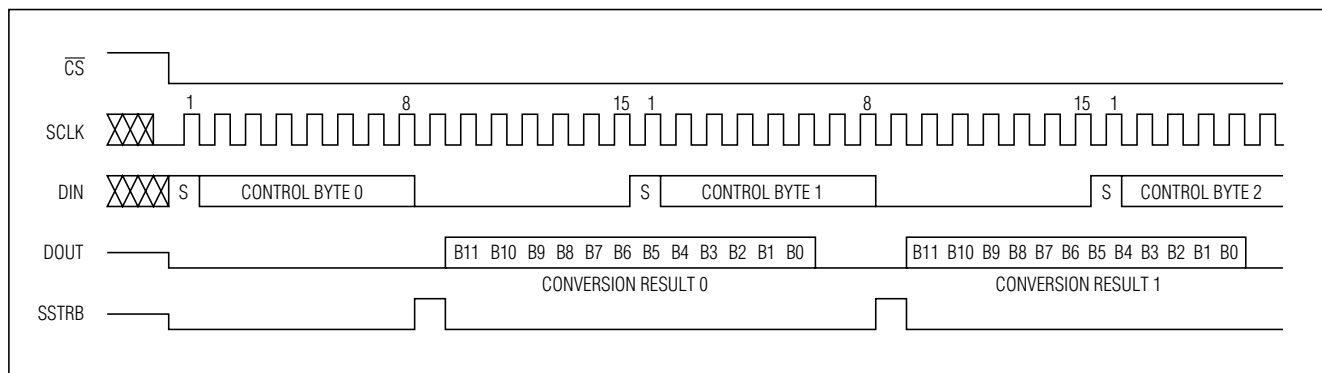


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

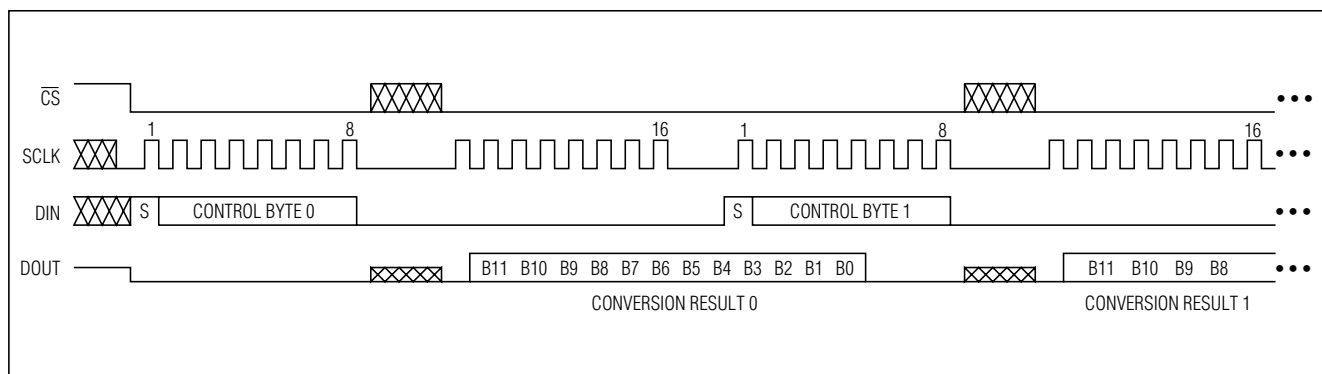


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

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Reference-Buffer Compensation

In addition to its shutdown function, $\overline{\text{SHDN}}$ selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. The 100kHz minimum clock rate is limited by droop on the sample-and-hold and is independent of the compensation used.

Float $\overline{\text{SHDN}}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7 μF capacitor at VREF. A 4.7 μF value ensures reference-buffer stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see the *Choosing Power-Down Mode* section and Table 4).

Pull $\overline{\text{SHDN}}$ high to select internal compensation. Internal compensation requires no external capacitor at VREF and allows for the shortest power-up times. The maximum clock rate is 2MHz in internal clock mode and 400kHz in external clock mode.

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down mode or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{\text{SHDN}}$ high or floating (Tables 1 and 5). In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Pull $\overline{\text{SHDN}}$ low at any time to shut down the converter completely. $\overline{\text{SHDN}}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing supply current to 2 μA (typ). Fast power-down mode turns off all circuitry

except the bandgap reference. With fast power-down mode, the supply current is 30 μA . Power-up time can be shortened to 5 μs in internal compensation mode.

Table 4 shows how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate. In external compensation mode, power-up time is 20ms with a 4.7 μF compensation capacitor when the capacitor is initially fully discharged. From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2LSB while shut down. In power-down, leakage currents at VREF cause droop on the reference bypass capacitor. Figures 12a and 12b show the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 5, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC operates in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX146/MAX147 enter a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX146/MAX147. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Table 4. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	VREF CAPACITOR (μF)	POWER-DOWN MODE	POWER-UP DELAY (μs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal	—	Fast	5	26
Enabled	Internal	—	Full	300	26
Enabled	External	4.7	Fast	See Figure 14c	133
Enabled	External	4.7	Full	See Figure 14c	133
Disabled	—	—	Fast	2	133
Disabled	—	—	Full	2	133

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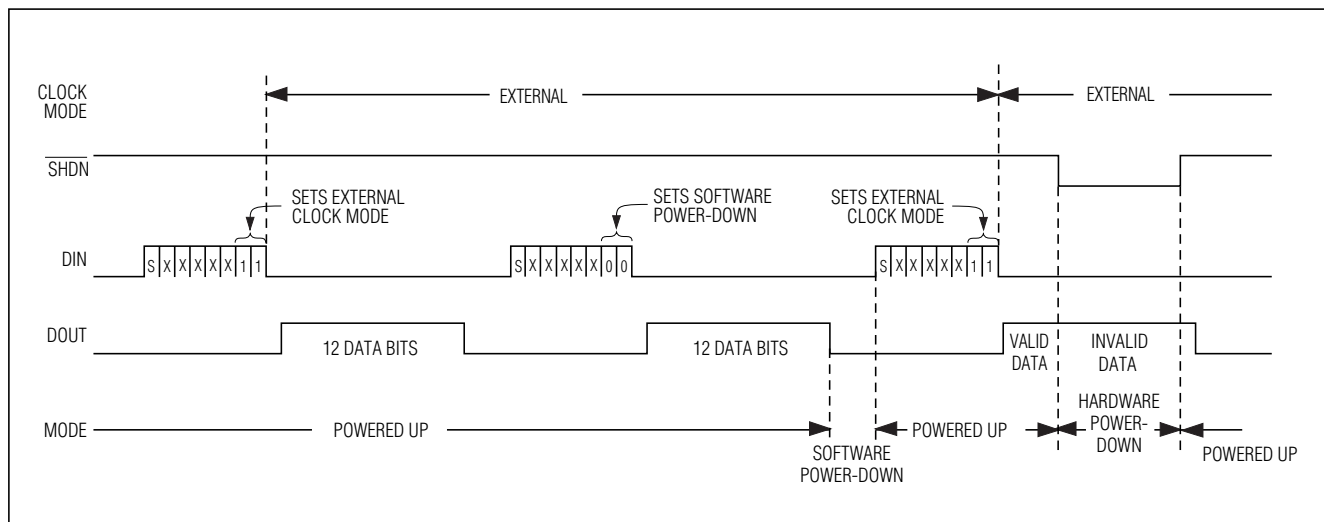


Figure 12a. Timing Diagram Power-Down Modes, External Clock

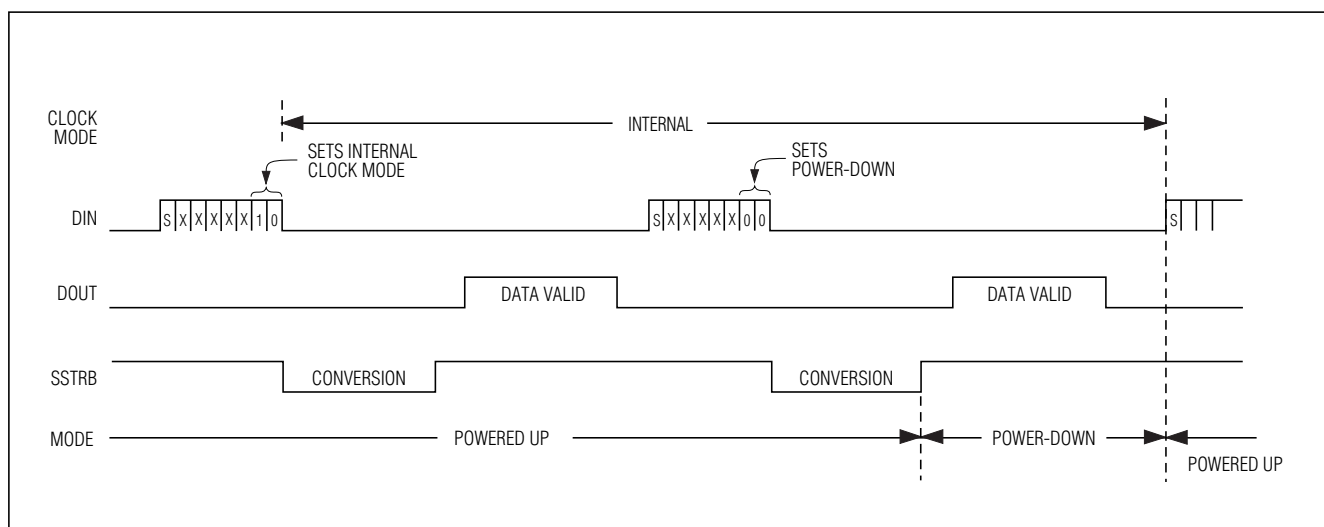


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Hardware Power-Down

Pulling SHDN low places the converter in hardware power-down (Table 6). Unlike software power-down mode, the conversion is not completed; it stops coincidentally with SHDN being brought low. SHDN also controls the clock frequency in internal clock mode. Letting SHDN float sets the internal clock frequency to 1.8MHz. When returning to normal operation with SHDN

floating, there is a t_{RC} delay of approximately $2M\Omega \times C_L$, where C_L is the capacitive loading on the SHDN pin. Pulling SHDN high sets internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage. With an external reference, the MAX146/MAX147 can be considered fully powered up within $2\mu s$ of actively pulling SHDN high.

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Power-Down Sequencing

The MAX146/MAX147 auto power-down modes can save considerable power when operating at less than maximum sample rates. Figures 13, 14a, and 14b show the average supply current as a function of the sampling rate. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples show two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 14a depicts the MAX146 power consumption for one or eight channel conversions utilizing full power-down mode and internal-reference compensation. A 0.047 μ F bypass capacitor at REFADJ forms an RC filter with the internal 20k Ω reference resistor with a 0.9ms time constant. To achieve full 12-bit accuracy, 10 time constants or 9ms are required after power-up. Waiting this 9ms in FASTPD mode instead of in full power-up can reduce power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 15.

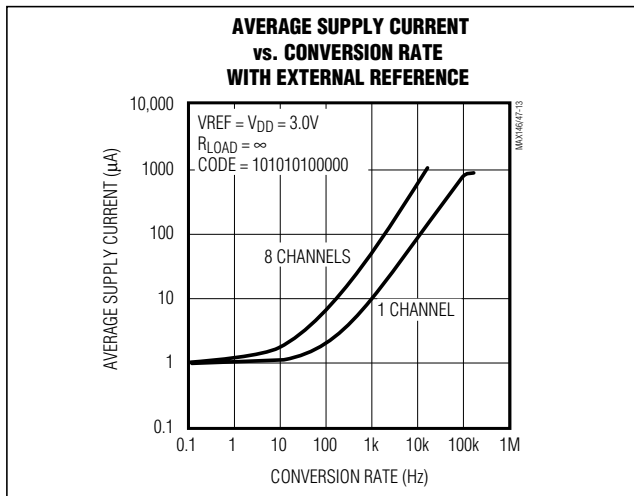


Figure 13. Average Supply Current vs. Conversion Rate with External Reference

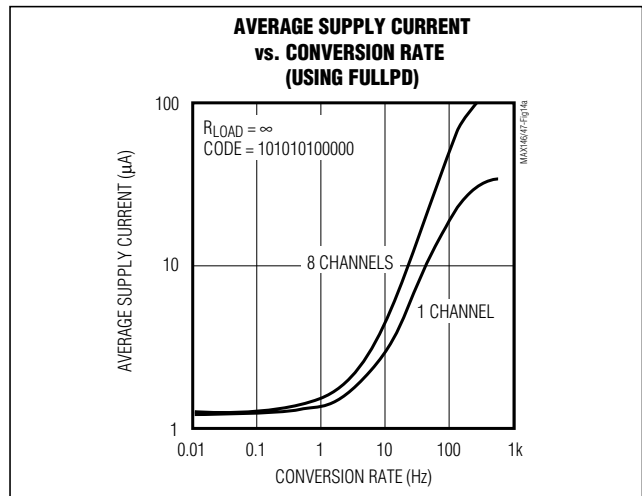


Figure 14a. MAX146 Supply Current vs. Conversion Rate, FULLPD

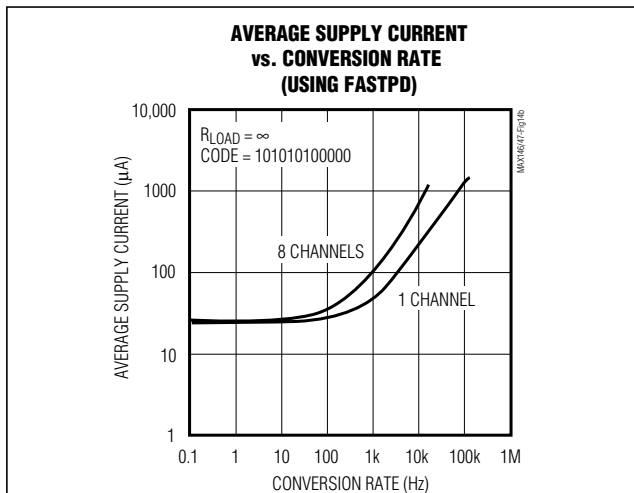


Figure 14b. MAX146 Supply Current vs. Conversion Rate, FASTPD

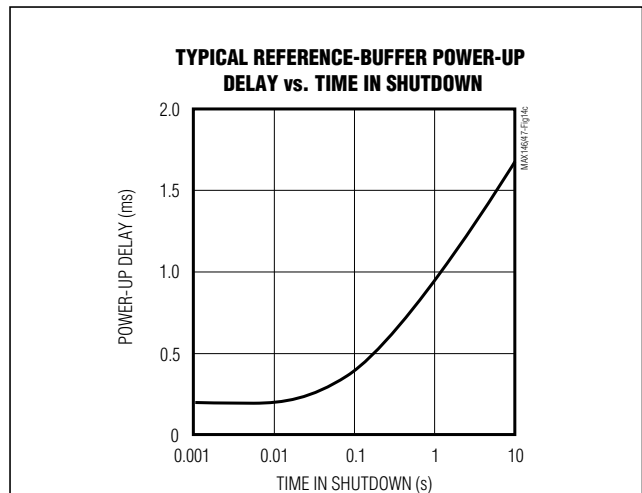


Figure 14c. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown

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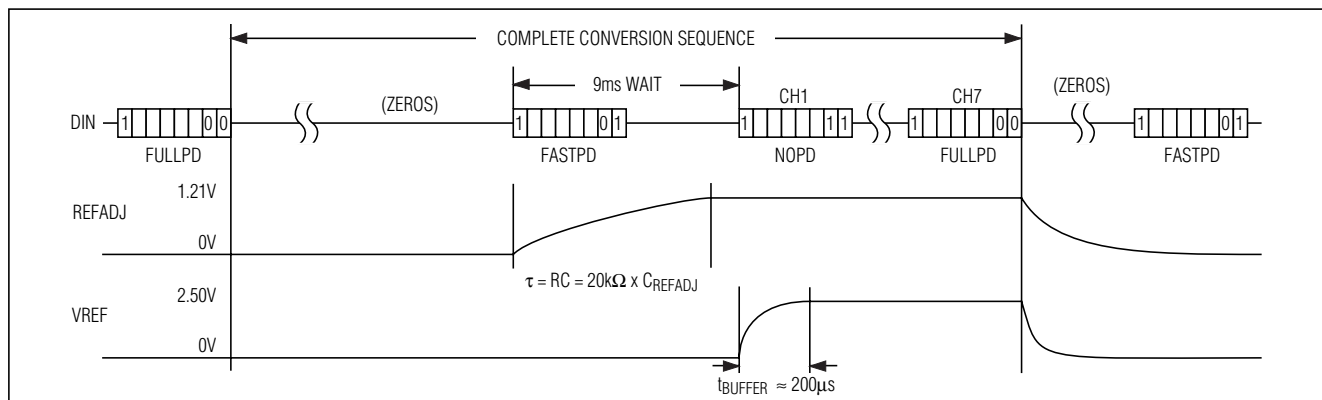


Figure 15. MAX146 FULLPD/FASTPD Power-Up Sequence

Lowest Power at Higher Throughputs

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7μF compensation requires a 200μs wait after power-up with one dummy conversion. This graph shows fast multi-channel conversion with the lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX146/MAX147 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

Internal and External References

The MAX146 can be used with an internal or external reference voltage, whereas an external reference is required for the MAX147. An external reference can be connected directly at VREF or at the REFADJ pin.

An internal buffer is designed to provide 2.5V at VREF for both the MAX146 and the MAX147. The MAX146's internally trimmed 1.21V reference is buffered with a 2.06 gain. The MAX147's REFADJ pin is also buffered with a 2.00 gain to scale an external 1.25V reference at REFADJ to 2.5V at VREF.

Internal Reference (MAX146)

The MAX146's full-scale range with the internal reference is 2.5V with unipolar inputs and ±1.25V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the circuit in Figure 16.

External Reference

With both the MAX146 and MAX147, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX146, and higher than 100kΩ for the MAX147. At

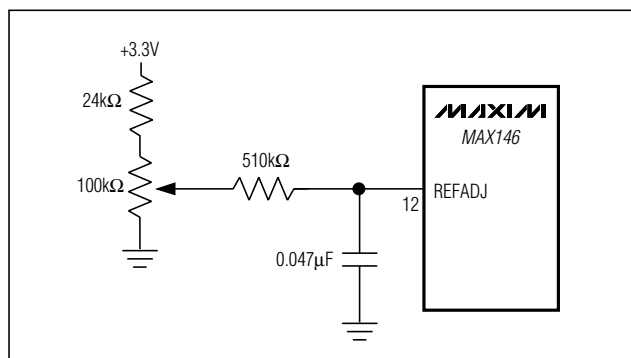


Figure 16. MAX146 Reference-Adjust Circuit

Table 5. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
0	0	Full Power-Down
0	1	Fast Power-Down
1	0	Internal Clock
1	1	External Clock

Table 6. Hard-Wired Power-Down and Internal Clock Frequency

SHDN STATE	DEVICE MODE	REFERENCE BUFFER COMPENSATION	INTERNAL CLOCK FREQUENCY
1	Enabled	Internal	225kHz
Floating	Enabled	External	1.8MHz
0	Power-Down	N/A	N/A

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VREF, the DC input resistance is a minimum of 18kΩ. During conversion, an external reference at VREF must deliver up to 350μA DC load current and have 10Ω or less output impedance. If the reference has a higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7μF capacitor.

Using the REFADJ input makes buffering the external reference unnecessary. To use the direct VREF input, disable the internal buffer by tying REFADJ to VDD. In power-down, the input bias current to REFADJ is typically 25μA (MAX146) with REFADJ tied to VDD. Pull REFADJ to AGND to minimize the input bias current in power-down.

Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

The external reference must have a temperature coefficient of 4ppm/°C or less to achieve accuracy to within 1LSB over the 0°C to +70°C commercial temperature range.

Figure 17 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 18 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 610μV (2.500V / 4096) for unipolar operation, and 1LSB = 610μV [(2.500V / 2 - -2.500V / 2) / 4096] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 19 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. For lowest-noise operation, the ground return to the star ground's power

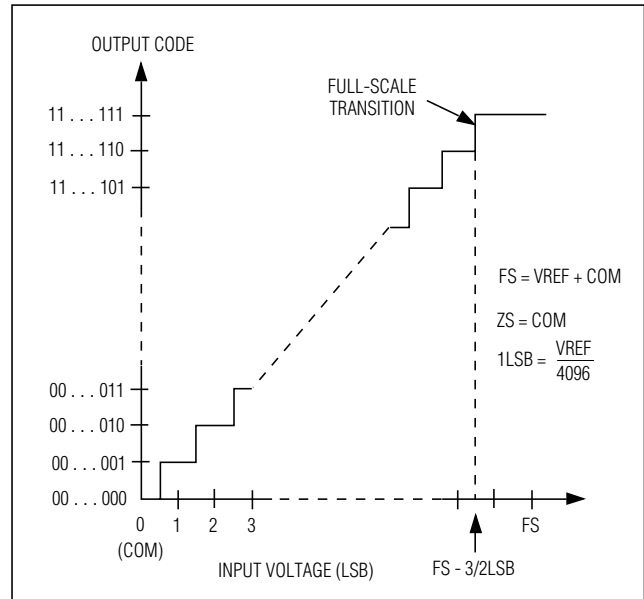


Figure 17. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

supply should be low impedance and as short as possible.

High-frequency noise in the VDD power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1μF and 1μF capacitors close to pin 20 of the MAX146/MAX147. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 19).

High-Speed Digital Interfacing with QSPI

The MAX146/MAX147 can interface with QSPI using the circuit in Figure 20 (fSCLK = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own microsequencer.

The MAX146/MAX147 are QSPI compatible up to the maximum external clock frequency of 2MHz.

Table 7. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF / 2 + COM	COM	-VREF / 2 + COM

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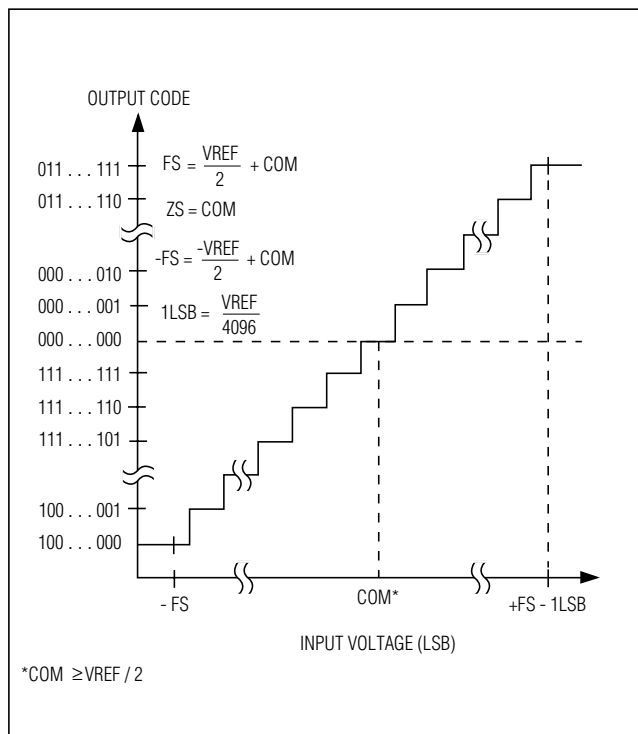


Figure 18. Bipolar Transfer Function, Full Scale (FS) = $V_{REF}/2 + COM$, Zero Scale (ZS) = COM

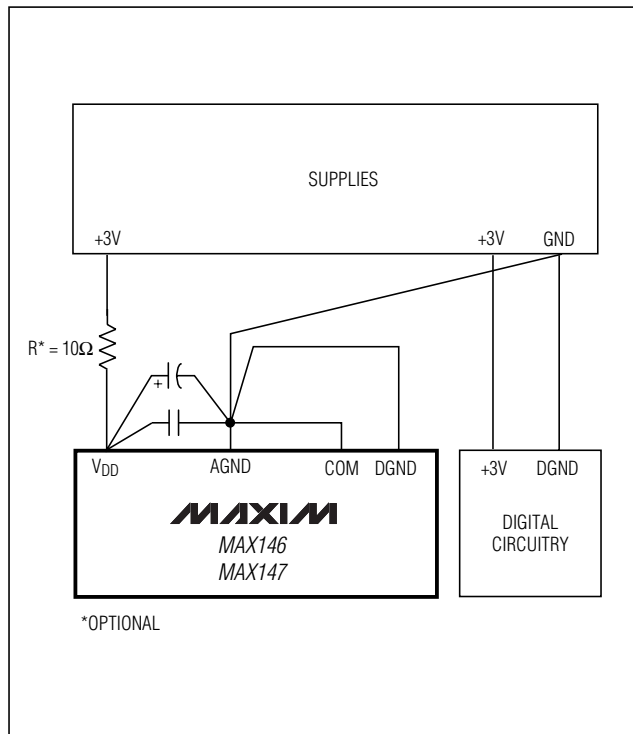


Figure 19. Power-Supply Grounding Connection

TMS320LC3x Interface

Figure 21 shows an application circuit to interface the MAX146/MAX147 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 22.

Use the following steps to initiate a conversion in the MAX146/MAX147 and to read the results:

- 1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX146/MAX147's SCLK input.
- 2) The MAX146/MAX147's \overline{CS} pin is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX146/MAX147's DIN.
- 3) An 8-bit word (1XXXXX11) should be written to the MAX146/MAX147 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.

- 4) The MAX146/MAX147's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX146/MAX147.
- 5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
- 6) Pull \overline{CS} high to disable the MAX146/MAX147 until the next conversion is initiated.

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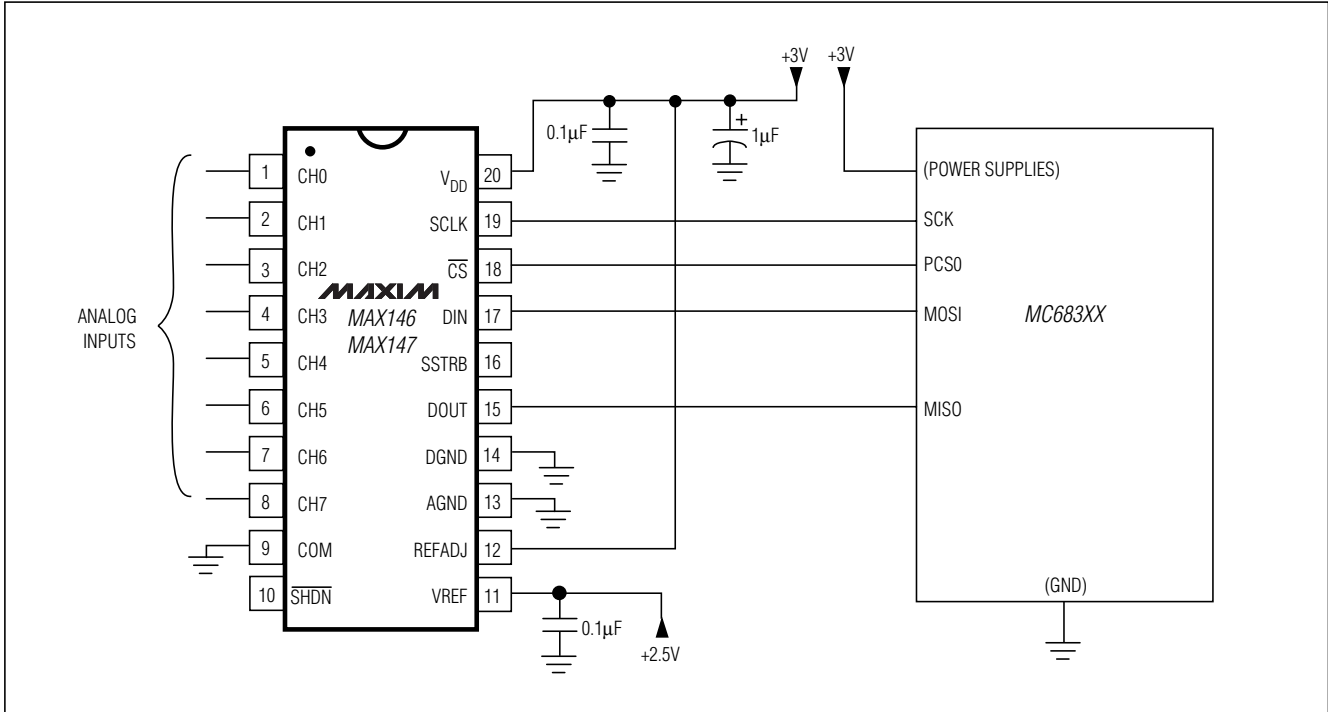


Figure 20. MAX146/MAX147 QSPI Connections, External Reference

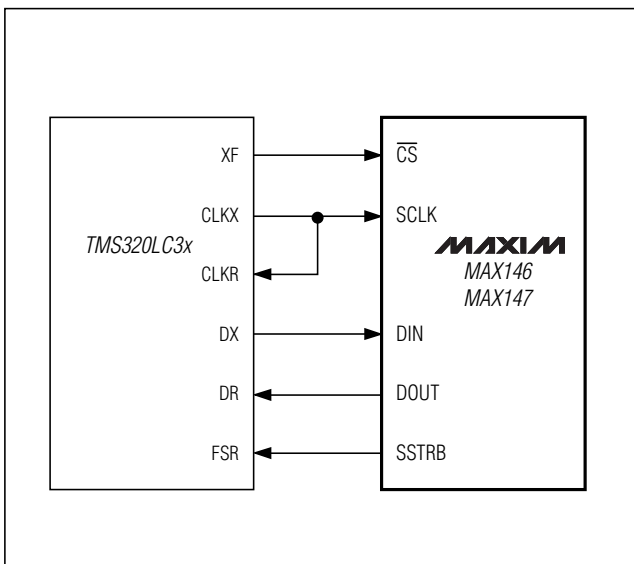


Figure 21. MAX146/MAX147-to-TMS320 Serial Interface

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MAX146/MAX147

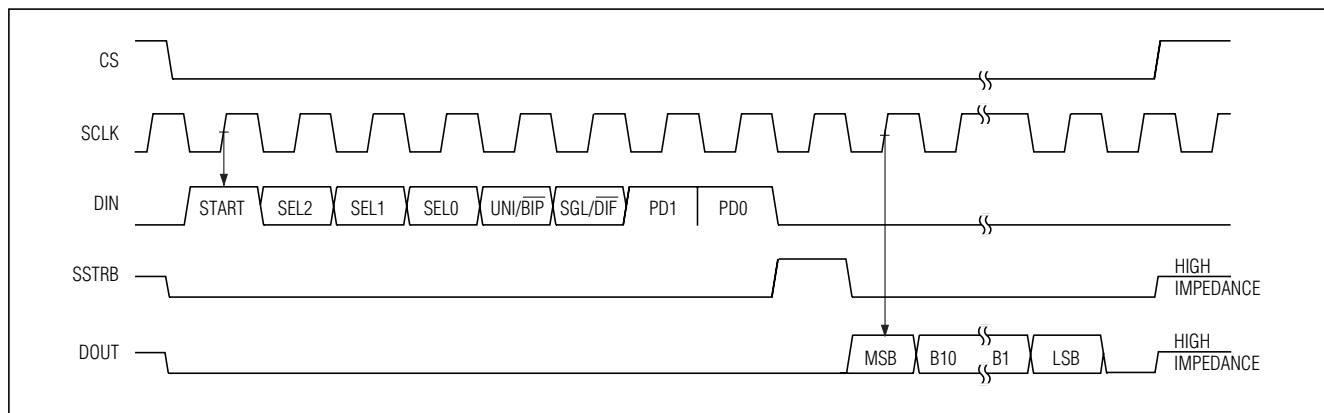


Figure 22. TMS320 Serial-Interface Timing Diagram

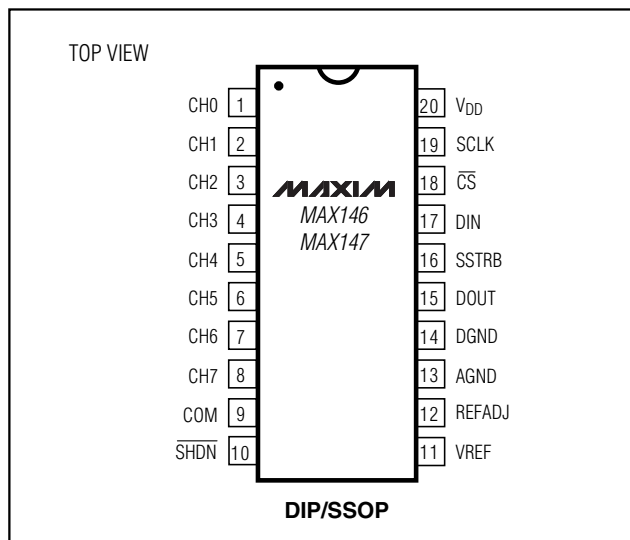
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX146AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX146BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX146AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX146BEAP	-40°C to +85°C	20 SSOP	±1
MAX146AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX146BMJP	-55°C to +125°C	20 CERDIP**	±1
MAX147ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX147BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX147ACAP	0°C to +70°C	20 SSOP	±1/2
MAX147BCAP	0°C to +70°C	20 SSOP	±1
MAX147CCAP	0°C to +70°C	20 SSOP	±2.0
MAX147BC/D	0°C to +70°C	Dice*	±1
MAX147AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX147BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX147AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX147BEAP	-40°C to +85°C	20 SSOP	±1
MAX147CEAP	-40°C to +85°C	20 SSOP	±2.0
MAX147AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX147BMJP	-55°C to +125°C	20 CERDIP**	±1

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

**Contact factory for availability of CERDIP package, and for processing to MIL-STD-883B.

Pin Configuration



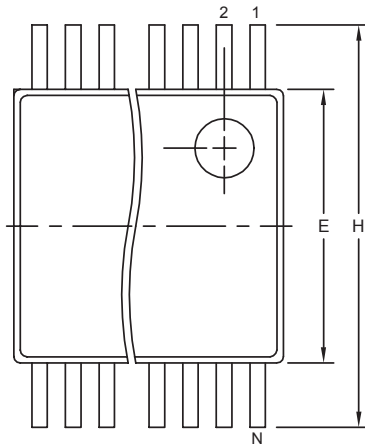
Chip Information

TRANSISTOR COUNT: 2554

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

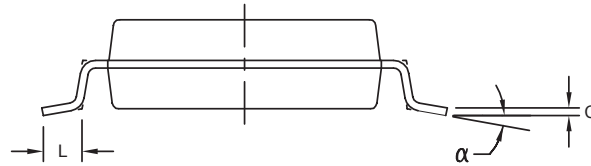
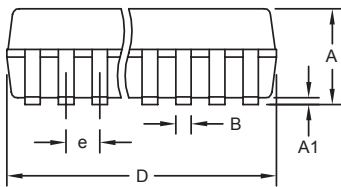
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0 $^{\circ}$	8 $^{\circ}$	0 $^{\circ}$	8 $^{\circ}$

D	INCHES		MILLIMETERS		N
	MIN	MAX	MIN	MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

<small>PROPRIETARY INFORMATION</small>		
TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM		
APPROVAL:	DOCUMENT CONTROL NO. 21-0056	REV. C 1/1

SSOP/EPS

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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[MAX147BEAP+](#) [MAX147EVC16-DIP](#) [MAX147EVC32-DIP](#) [MAX146ACAP+T](#) [MAX146ACPP+](#) [MAX146AEAP+](#)
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[MAX146BEAP-T](#) [MAX146BEAP](#) [MAX14677EZA+T](#) [MAX14629EETJ+T](#)