Upstream CATV Amplifier with On-Chip Anti-Alias Filter

ABSOLUTE MAXIMUM RATINGS

V_{CC}, OUT+, OUT- to GND.....-0.5V to +8.0V
Input Voltage Levels (all inputs),
C_{EXT} to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Input Voltage (IN+, IN-) 2Vp-p
Continuous Current (OUT+, OUT-) 120mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin QFN (derate 20.8mW/°C above +70°C) 1.67W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +125°C
Bump Reflow Temperature .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX3507 EV Kit, V_{CC} = +4.75V to +5.25V, V_{GND} = 0, V_{TXEN} = $V_{\overline{SHDN}}$ = V_{CC}, D7 = 1, T_A = -40°C to +85°C, unless otherwise specified. No input signal applied. A 4:1 (300Ω to 75Ω) impedance ratio balun is connected to differential output ports and balun output is terminated into a 75Ω load. Typical parameters are at V_{CC} = +5.0V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.75		5.25	V
Supply Current Transmit Mode	D7 = 1, gain code = 127 (max gain)		218	280	mA
	D7 = 1, gain code = 119 (gain of 28dB)		164		
	D7 = 1, gain code = 64 (gain of 0dB)		82		
	D7 = 0, gain code = 94 (gain of 0dB)		74		
Supply Current Transmit Disable Mode	V_{TXEN} = V_{EE}, $V_{\overline{SHDN}}$ = V_{CC}		45	59	mA
Shutdown Supply Current	V_{TXEN} = X, $V_{\overline{SHDN}}$ = V_{EE}		1		µA
LOGIC INPUTS					
Input HIGH Voltage Threshold		2.0			V
Input LOW Voltage Threshold				0.8	V
Input HIGH Current				100	µA
Input LOW Current		-100			µA

AC ELECTRICAL CHARACTERISTICS

(MAX3507 EV Kit, V_{CC} = +4.75V to +5.25V, V_{GND} = 0, V_{TXEN} = $V_{\overline{SHDN}}$ = V_{CC}, V_{IN} = +34dBmV differential, T_A = -40°C to +85°C, unless otherwise specified. A 4:1 impedance ratio (300Ω to 75Ω) balun is connected to differential output ports and balun output is terminated into a 75Ω load. Typical parameters are at V_{CC} = +5.0V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Gain (A_V)	f_{IN} = 5MHz, T_A = 0°C to +85°C (Note 2)	D7 = 1, gain code = 125	29.6	31.1	32.6	dB
		D7 = 1, gain code = 119	26.8	28.3	29.8	
		D7 = 1, gain code = 104	19.5	20.9	22.3	
		D7 = 1, gain code = 84	9.7	10.9	12.1	
		D7 = 1, gain code = 64	-0.7	0.5	1.7	
		D7 = 0, gain code = 74	-10.5	-9.3	-8.1	
		D7 = 0, gain code = 54	-20.4	-19.1	-17.8	
		D7 = 0, gain code = 42	-27.2	-25.7	-24.2	
	f_{IN} = 65MHz, T_A = 0°C to +85°C (Note 3)	D7 = 1, gain code = 127	29.0			
Gain Flatness	V_{OUT} = 61dBmV, f_{IN} = 42MHz, equalizer disabled (Note 3)		-1.1	-0.5	+0.2	dB
	V_{OUT} = 61dBmV, f_{IN} = 65MHz, equalizer disabled (Note 3)		-2.1	-0.7	+0.3	
Gain Step Size	f_{IN} = 5MHz to 65MHz, A_V = -26dB to +30dB			0.5		dB
	f_{IN} = 5MHz to 65MHz, A_V = -26dB to +30dB, any 2-bit transition of D0, D1		0.7	1.0	1.3	
	f_{IN} = 5MHz to 42MHz, D7 = 0, gain code = 109; D7 = 1, gain code = 81, T_A = 0°C to +85°C		0.6	1.0	1.4	
Transmit-Disable Mode Noise	Any BW = 160kHz from 5MHz to 65MHz, TXEN = V_{EE} (Note 3)				-64	dBmV
Isolation in Transmit Disable Mode	TXEN = V_{EE}, f_{IN} = 5MHz to 65MHz			70		dB
Transmit Mode Noise	Any BW = 160kHz from 5MHz to 65MHz, gain = -26dB to +30dB (Note 3)				-54.5	dBc
Transmit Enable Transient Duration	TXEN input rise/fall time < 0.1µs, T_A = +25°C (Notes 3, 4)				2	µs
Transmit Disable Transient Duration	TXEN input rise/fall time < 0.1µs, T_A = +25°C (Notes 3, 4)				2	µs
Transmit Disable/Transmit Enable Transient Step Size	D7 = 1, gain code = 119 (A_V = >27dB), T_A = +25°C				100	mVp-p
	D7 = 0, gain code = 94 (A_V = 0), T_A = +25°C (Note 3)			1.5	5.2	
Input Impedance	f_{IN} = 5MHz to 65MHz, single ended (Note 3)		0.8			kΩ
Output Return Loss	f_{IN} = 5MHz to 42MHz in 75Ω system, D7 = 1, gain code = 125 (A_V = 30dB) (Note 5)			10		dB
Output Return Loss in Transmit Disable Mode	f_{IN} = 5MHz to 42MHz in 75Ω system, TXEN = V_{EE} (Note 5)			10		dB

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX3507 EV Kit, V_{CC} = +4.75V to +5.25V, V_{GND} = 0, V_{TXEN} = $V_{\overline{SHDN}}$ = V_{CC}, V_{IN} = +34dBmV differential, T_A = -40°C to +85°C, unless otherwise specified. A 4:1 impedance ratio (300Ω to 75Ω) balun is connected to differential output ports and balun output is terminated into a 75Ω load. Typical parameters are at V_{CC} = +5.0V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Two-Tone Third-Order Distortion	Input tones at 42MHz and 42.2MHz, both at +31dBmV, V_{OUT} = +58dBmV/tone		-55.4		dBc
	Input tones at 65MHz and 65.2MHz, both at +31dBmV, V_{OUT} = +58dBmV/tone		-47.6		
2^{ND} Harmonic Distortion	f_{IN} = 33MHz, V_{OUT} = +63dBmV		-58		dBc
	f_{IN} = 33MHz, V_{OUT} = +60dBmV, T_A = 0°C to +85°C		-56	-50	
	f_{IN} = 65MHz, V_{OUT} = +60dBmV		-61		
3^{RD} Harmonic Distortion	f_{IN} = 22MHz, V_{OUT} = +63dBmV		-53		dBc
	f_{IN} = 22MHz, V_{OUT} = +60dBmV		-58	-51	
	f_{IN} = 65MHz, V_{OUT} = +60dBmV		-57		
1dB Compression Point	Gain = 26dB, f_{IN} = 65MHz		22		dBm
AM to AM	Gain = 28dB, V_{IN} = +34dBmV to +38dBmV, f_{IN} = 65MHz		-0.1		dB
AM to PM	Gain = 28dB, V_{IN} = +34dBmV to +38dBmV, f_{IN} = 65MHz		-1.3		degrees
Rejection at 135MHz	Referenced to 65MHz	36	47		dBc

TIMING CHARACTERISTICS

(MAX3507 EV Kit, V_{CC} = +4.75V to +5.25V, V_{GND} = 0, V_{TXEN} = $V_{\overline{SHDN}}$ = V_{CC}, T_A = +25°C, unless otherwise specified.) (Note 3)

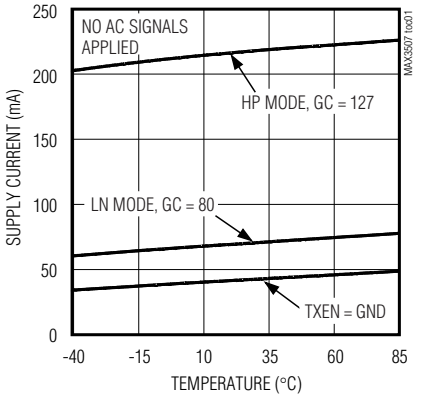
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEN to SCLK Rise Set Time	t_{SENS}		20			ns
SEN to SCLK Rise Hold Time	t_{SENH}		10			ns
SDA to SCLK Setup Time	t_{SDAS}		10			ns
SDA to SCLK Hold Time	t_{SDAH}		20			ns
SDA Pulse-Width High	t_{DATAH}		50			ns
SDA Pulse-Width Low	t_{DATAL}		50			ns
SCLK Pulse-Width High	t_{SCLKH}		50			ns
SCLK Pulse-Width Low	t_{SCLKL}		50			ns

Note 1: Guaranteed by design and characterization to ±3 sigma for T_A < +25°C, unless otherwise specified.
Note 2: AC gain correlated to DC gain measurements to ±3 sigma.
Note 3: Guaranteed by design and characterization to ±6 sigma.
Note 4: All transients comply with DOCSIS 1.1 limits for transmit power ripple of ±0.1dB.
Note 5: Does not include output matching; see *Output Match* in the *Applications* section.

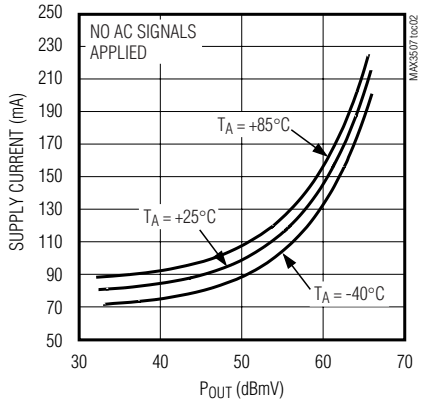
Typical Operating Characteristics

(MAX3507 EV Kit, V_{CC} = +5.0V, V_{IN} = +34dBmV, TXEN = $\overline{SHDN}$ = V_{CC}, f_{IN} = 20MHz, T_A = +25°C, unless otherwise noted.)

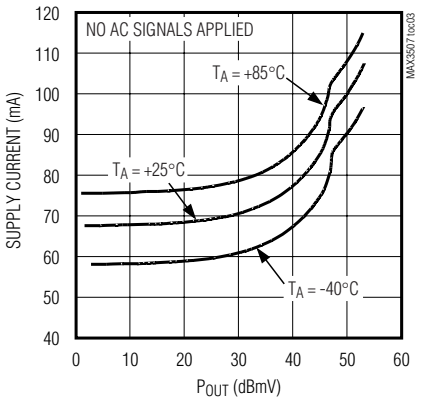
SUPPLY CURRENT vs. TEMPERATURE



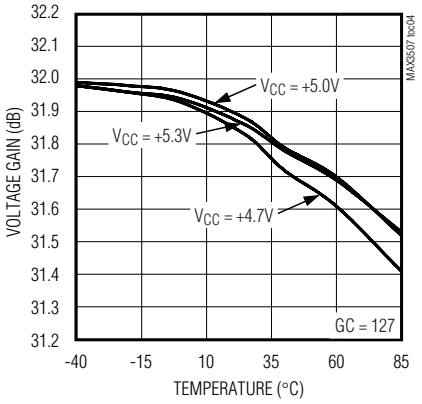
SUPPLY CURRENT IN HIGH-POWER MODE vs. OUTPUT POWER



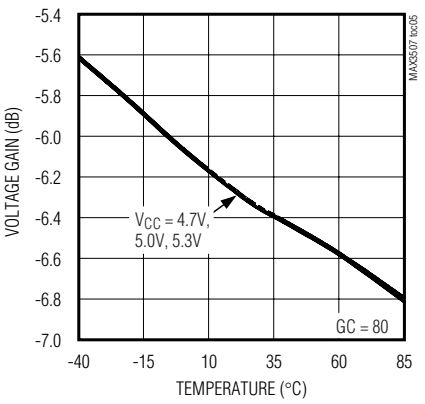
SUPPLY CURRENT IN LOW-NOISE MODE vs. OUTPUT POWER



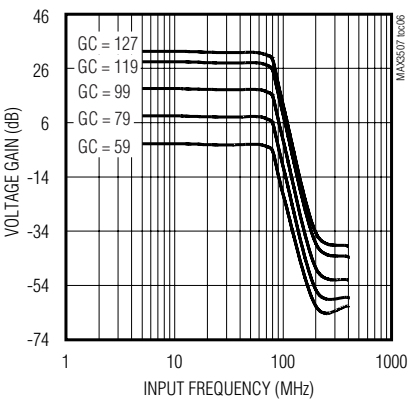
VOLTAGE GAIN IN HIGH-POWER MODE vs. TEMPERATURE



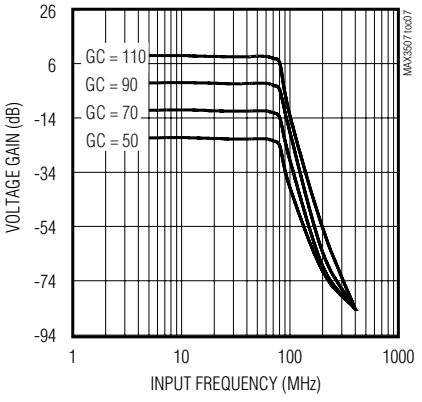
VOLTAGE GAIN IN LOW-NOISE MODE vs. TEMPERATURE



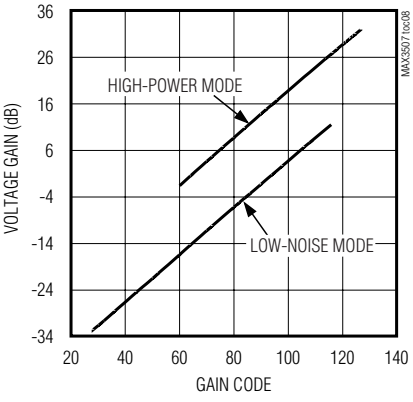
VOLTAGE GAIN IN HIGH-POWER MODE vs. FREQUENCY



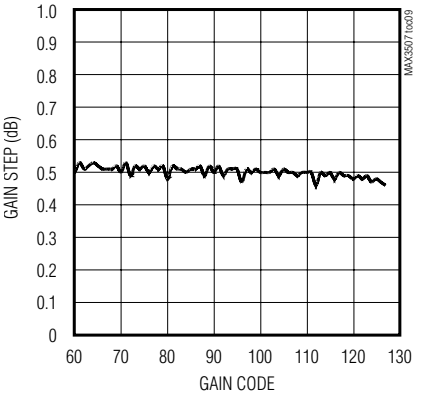
VOLTAGE GAIN IN LOW-NOISE MODE vs. FREQUENCY



VOLTAGE GAIN vs. GAIN CODE



GAIN STEP IN HIGH-POWER MODE vs. GAIN CODE



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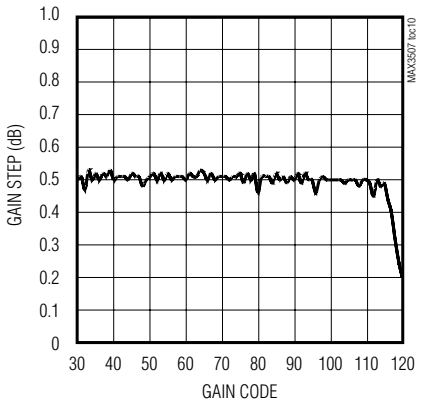
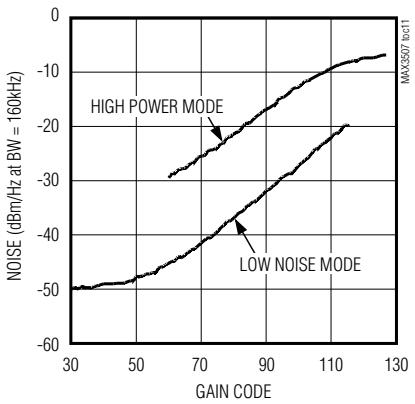
Typical Operating Characteristics (continued)

(MAX3507 EV Kit, V_{CC} = +5.0V, V_{IN} = +34dBmV, TXEN = $\overline{SHDN}$ = V_{CC}, f_{IN} = 20MHz, T_A = +25°C, unless otherwise noted.)

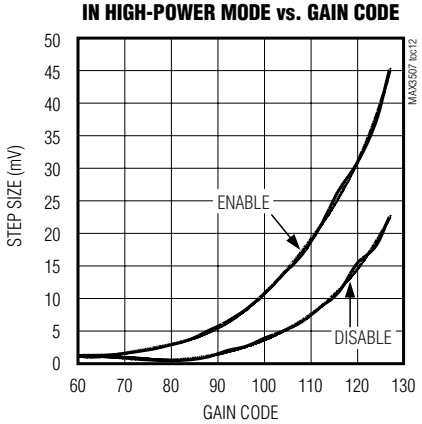
GAIN STEP IN LOW-NOISE MODE vs. GAIN CODE



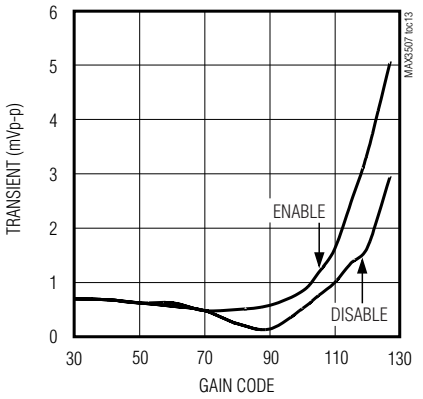
TRANSMIT NOISE vs. GAIN CODE



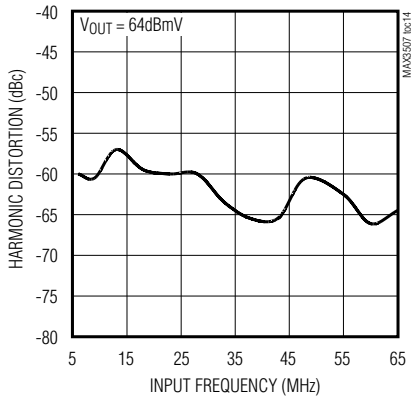
TRANSMIT ENABLE/DISABLE TRANSIENT IN HIGH-POWER MODE vs. GAIN CODE



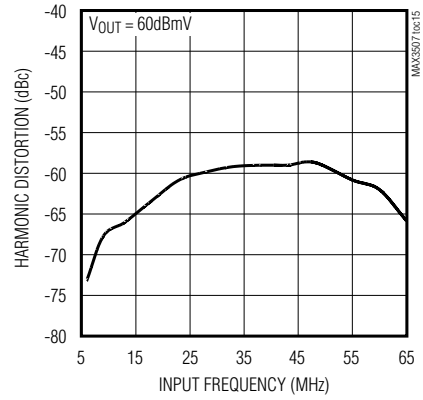
TRANSMIT ENABLE/DISABLE TRANSIENT IN LOW-NOISE MODE vs. GAIN CODE



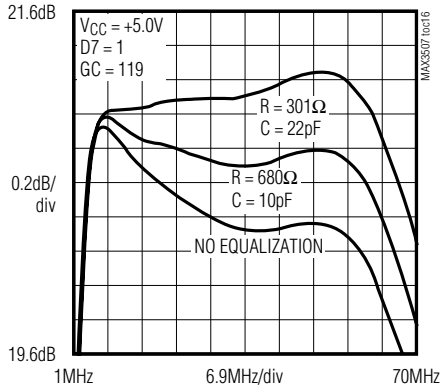
2ND-ORDER HARMONIC DISTORTION IN HIGH-POWER MODE vs. FREQUENCY



3RD-ORDER HARMONIC DISTORTION IN HIGH-POWER MODE vs. FREQUENCY



PASSBAND FLATNESS vs. RC



Pin Description

PIN	NAME	DESCRIPTION
1	BIASF	Filter Bias. Connect to GND.
2	DC+	Filter Offset Correction. Connect 0.1µF capacitor between this pin and DC-.
3	DC-	Filter Offset Correction. Connect 0.1µF capacitor between this pin and DC+.
4, 8, 12, 23, 26	GND	Ground
5, 22, 25	V_{CC}	+5V Supply. Bypass this pin to GND with a 0.1µF capacitor as close to the part as possible.
6	IN+	Positive Input. Along with IN-, this port forms a high-impedance differential input to the filter.
7	IN-	Negative Input. When not used, this port must be AC-coupled to ground. See IN+.
9	$\overline{CS}$	Serial Interface Enable (Chip Select). TTL-compatible input. See *Serial Interface* section.
10	SDA	Serial Interface Data (Serial Data). TTL-compatible input. See *Serial Interface* section.
11	SCLK	Serial Interface Clock (Serial Clock). TTL-compatible input. See *Serial Interface* section.
13, 15, 17, 20, 24	N.C.	No Connection. Not internally connected.
14	$\overline{SHDN}$	Shutdown. When $\overline{SHDN}$ is set low, all functions (including the serial interface) are disabled.
16	CEXT	RF Output Bypass. Bypass to ground with a 0.1µF capacitor.
18	OUT-	Negative Output. Along with OUT+, this port forms a 300Ω impedance output. This port is matched to a 75Ω load using a 2:1 (voltage ratio) transformer.
19	OUT+	Positive Output. See OUT-.
21	TXEN	Signal Path Enable. Setting this pin low turns off the PGA and power amplifier, leaving the filter and serial interface enabled to save the last gain setting.
27	EQ+	Positive Equalizer. Connect an RC network if equalization of the filter passband is desired; leave open otherwise. See *Typical Operating Characteristics*.
28	EQ-	Negative Equalizer. Connect an RC network if equalization of the filter passband is desired; leave open otherwise. See *Typical Operating Characteristics*.

Detailed Description

Internal Filter

The internal filter consists of an input transconductance amplifier, a balanced fifth-order elliptic active lowpass filter, and an offset-correction feedback network. The signal at the output of the filter is level-shifted into the programmable-gain amplifier.

The transconductance amplifier provides a high input impedance to the user, and current drives the filter to minimize insertion loss. The filter is a Gm-C topology to provide sufficient bandwidth and linearity. The cutoff frequency of the filter is fixed at 75MHz, while the specified stopband attenuation is met at 120MHz.

The internal offset-correction feedback network removes any DC offset at the output of the filter. An offset voltage at this node would generate a transient during a TX-enable or -disable transition, which would not be acceptable. The offset-correction loop effectively AC-couples the filter output to the programmable-gain amplifier input. The network generates a highpass corner frequency at:

$$f_{-3dB}(kHz) = 12.5/C(\mu F)$$

Specified performance is achieved when the input is driven differentially. The MAX3507 may be driven single-ended. To drive the device in this manner, one of the input pins must be capacitively coupled to ground. Use a capacitor whose value is large enough to allow for a low-impedance path to ground at the lowest frequency of operation. For operation down to 5MHz, a 0.001µF capacitor is suggested.

Programmable-Gain Amplifier

The programmable-gain amplifier (PGA) consists of the variable-gain amplifier (VGA) and the digital-to-analog converter (DAC), which provide better than 55dB of output-level control in 0.5dB steps. The PGA is implemented as a programmable Gilbert-cell attenuator. It uses a differential architecture to achieve maximum linearity. The gain of the PGA is determined by a 7-bit

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word (D6–D0) programmed through the serial data interface (Tables 1 and 2).

Equalizer Function

It is possible to add passband amplitude equalization to the MAX3507. This is accomplished by adding pole-zero peaking to the Gm stage of the PGA. Placing a series RC network between pins EQ+ and EQ- realizes the peaking function. Refer to *Typical Operating Characteristics* for typical values and the associated degree of equalization.

Power Amplifier

The power amplifier is a Class A differential amplifier capable of driving +64dBmV (QPSK) differentially. This architecture provides superior even-order distortion performance but requires that a transformer be used to convert to a single-ended output. In transmit-disable mode, the output amplifier is shut off. Disabling the output devices also allows the lowest standby noise.

To achieve the proper load line, the output impedance of the power amplifier is 300Ω differential. To match the output impedance to a 75Ω load, the transformer must have a turns ratio (voltage ratio) of 2:1 (4:1 impedance ratio). The differential amplifier is biased directly from the +5V supply using the center tap of the output transformer. This provides a significant benefit when switching between transmit mode and transmit disable mode. Stored energy due to bias currents will cancel within the transformer and prevent switching transients from reaching the load.

Serial Interface

The serial interface has an active-low enable ($\overline{CS}$) to bracket the data, with data clocked in MSB first on the rising edge of SCLK. Data is stored in the storage latch on the rising edge of $\overline{CS}$. The serial interface controls the gain state of the PGA and the output amplifier. Tables 1 and 2 show the register format. Serial interface timing is shown in Figure 1.

Applications Information

Transmit High-Power and Low-Noise Modes

The MAX3507 has two transmit modes, high-power (HP) mode and low-noise (LN) mode. Each of these modes is controlled by D7 (MSB) of the 8-bit programming word. When D7 is a logical 1, HP mode is enabled. When D7 is a logical 0, LN mode is enabled.

Each of these modes is characterized by the activation of a distinct output stage. In HP mode, the output stage exhibits a gain that is 15dB higher than gain in LN mode. In LN mode, the lower gain output stage allows for significantly lower output noise and lower transmit/transmit disable transients.

The full range of gain codes (D6–D0) may be used in either mode. For DOCSIS applications, HP mode is recommended for output levels at or above +42dBmV, and LN mode is recommended for output levels below +42dBmV.

Table 1. Serial-Interface Control Word

BIT	MNEMONIC	DESCRIPTION
7 (MSB)	D7	High-Power/Low-Noise Mode Select
6	D6	Gain Code, Bit 6
5	D5	Gain Code, Bit 5
4	D4	Gain Code, Bit 4
3	D3	Gain Code, Bit 3
2	D2	Gain Code, Bit 2
1	D1	Gain Code, Bit 1
0 (LSB)	D0	Gain Code, Bit 0

Shutdown Mode

In normal operation, the shutdown pin ($\overline{SHDN}$) is held high. When $\overline{SHDN}$ is set low, all circuits within the device are disabled. Only leakage currents flow in this state. Data stored within the serial data interface latches will be lost upon entering this mode. Current consumption is reduced to 1µA (typ) in shutdown mode.

Output Match

The MAX3507 output impedance is internally matched to 300Ω. This 300Ω internal resistor is placed across the OUT+ and OUT- terminals. When used in conjunction with a 2:1 (voltage ratio) transformer, the MAX3507 output impedance is matched to 75Ω.

To improve the output impedance matching for the high-end frequency range (65MHz), a reactive match may be employed as part of the ensuing diplex filter. The reactive match normally consists of a series inductor (180nH typ) followed by a shunt capacitor (33pF typ), and is placed directly after the output transformer. This match will also improve the gain flatness substantially.

As mentioned above, the matching components may be incorporated into the diplex filter design. Optimize the input impedance of the diplex filter to be 35 + j35 (typ) at 65MHz when using the specified output transformer.

Transformer

To match the output of the MAX3507 to a 75Ω load, a 2:1 (voltage ratio) transformer is required. This trans-

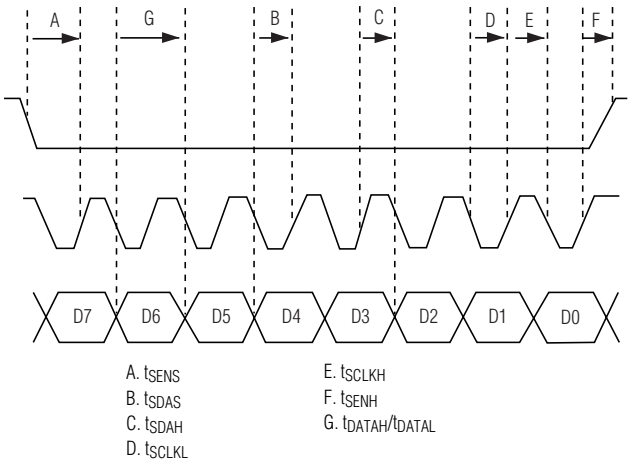

Figure 1. Serial Interface Timing Diagram

Table 2. Chip-State Control Bits

$\overline{SHDN}$	TXEN	D7	D6	D5	D4	D3	D2	D1	D0	GAIN STATE (DECIMAL)	GAIN (dB)	STATES
0	X	X	X	X	X	X	X	X	X	—	—	Shutdown
1	0	X	X	X	X	X	X	X	X	—	—	Transmit Disable Mode
1	1	1	X	X	X	X	X	X	X	—	—	Transmit Enable Mode, High Power
1	1	0	X	X	X	X	X	X	X	—	—	Transmit Enable Mode, Low Noise
1	1	0	0	1	1	0	0	0	0	48	-22.6	—
1	1	0	1	0	1	0	0	0	0	80	-6.29	—
1	1	0	1	1	0	1	1	1	0	110	8.68	—
1	1	1	1	0	1	0	1	1	0	86	11.69	—
1	1	1	1	1	0	1	1	1	0	110	23.7	—
1	1	1	1	1	1	1	1	0	1	125	31.0	—

Typical gain at T_A = +25°C and V_{CC} = +5V.

former must have adequate bandwidth to cover the intended application. Note that most RF transformers specify bandwidth with a 50Ω source on the primary and a matching resistance on the secondary winding. Operating in a 75Ω system will tend to shift the low-frequency edge of the transformer bandwidth specification up by a factor of 1.5, due to primary inductance. Keep this in mind when specifying a transformer.

Bias to the output stage is provided through the center tap on the transformer primary. This greatly diminishes the on/off transients present at the output when switching between transmit and transmit disable modes. Commercially available transformers typically have adequate balance between half-windings to achieve substantial transient cancellation.

Finally, keep in mind that transformer core inductance varies proportionally with temperature. If the application requires low temperature extremes (less than 0°C), adequate primary inductance must be present to sustain low-frequency output capability as temperatures

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drop. In general, this will not be a problem, as modern RF transformers have adequate bandwidth.

Input Circuit

To achieve rated performance, the inputs of the MAX3507 must be driven differentially with an appropriate input level. The differential input impedance is approximately 4kΩ. The MAX3507 has sufficient gain to produce an output level of +64dBmV (QPSK through a 2:1 transformer) when driven with a +34dBmV input signal. Rated performance is achieved with this input level. When a lower input level is present, the maximum output level will be reduced proportionally and output linearity will increase. If an input level greater than +34dBmV is used, the 3rd-order distortion performance will degrade.

If a single-ended source drives the MAX3507, one of the input terminals must be capacitively coupled to ground (IN+ or IN-). The value of this capacitor must be large enough to look like a short circuit at the lowest frequency of interest. For operation at 5MHz with a 75Ω source impedance, a value of 0.001µF will suffice.

Layout Issues

A well-designed PC board is an essential part of an RF circuit. For best performance pay attention to power-supply layout issues as well as the output circuit layout.

Power-Supply Layout

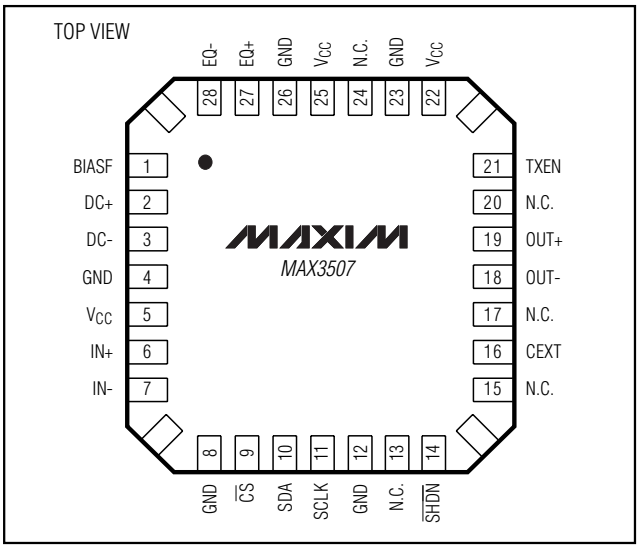
For minimal coupling between different sections of the MAX3507, the ideal power-supply layout is a star configuration. This configuration has a large-value decoupling capacitor at the central power-supply node. The power-supply traces branch out from this node, each going to a separate power-supply node in the circuit. At the end of each of these traces is a decoupling capacitor that provides very low impedance at the frequency of interest. This arrangement provides local power-supply decoupling at each power-supply pin. The power-supply traces must be made as thick as practical.

Ground inductance degrades distortion performance. Therefore, ground plane connections to pins 4, 8, 12, 23, and 26 should be made with multiple vias if necessary.

Output Circuit Layout

The differential implementation of the MAX3507's output has the benefit of significantly reducing even-order distortion, the most significant of which is 2nd-harmonic distortion. The degree of distortion cancellation depends on the amplitude and phase balance of the overall circuit. It is important to keep the trace lengths from the output pins equal.

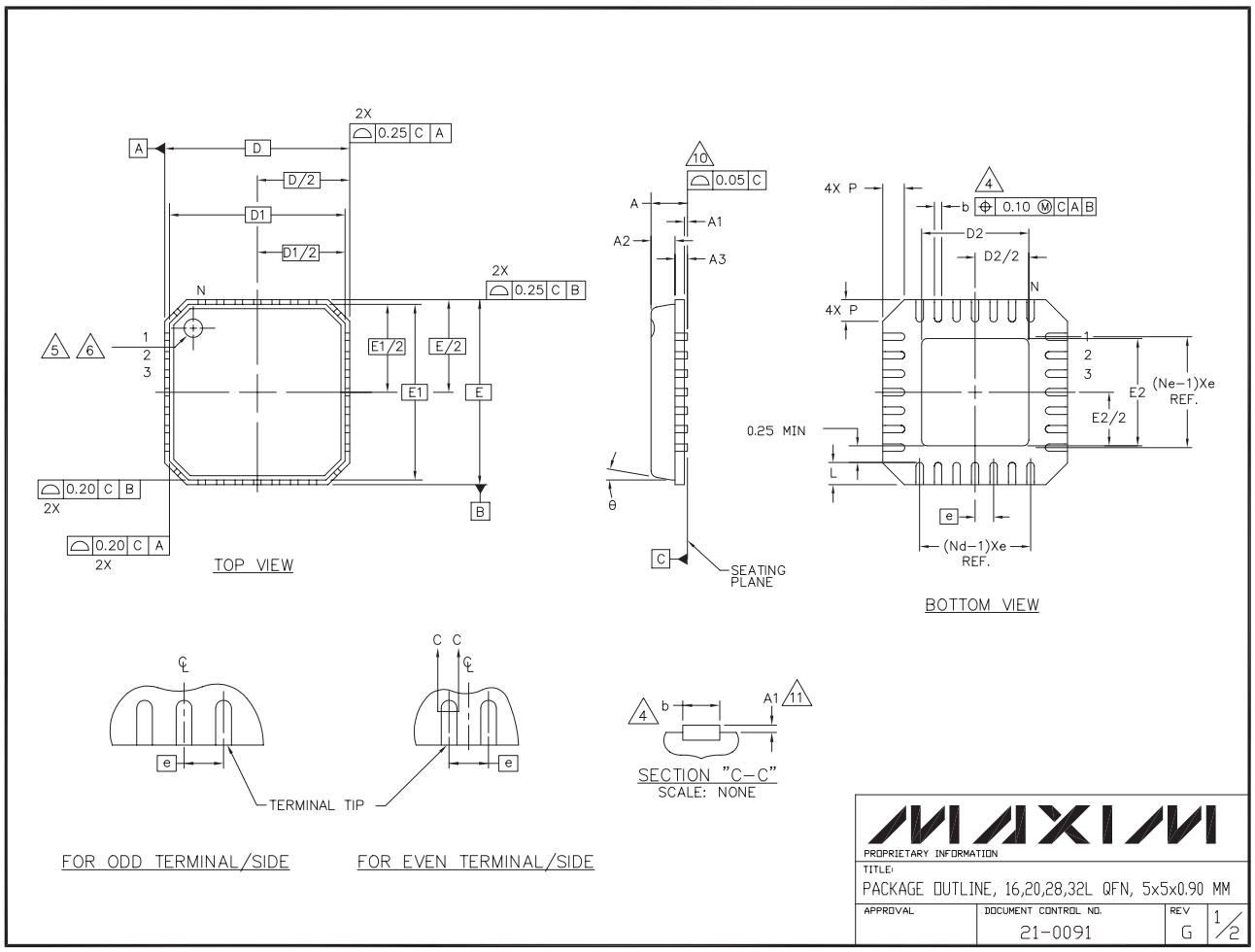
Pin Configuration



Chip Information

TRANSISTOR COUNT: 1457

Package Information



Upstream CATV Amplifier with On-Chip Anti-Alias Filter

Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	G	2/2

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