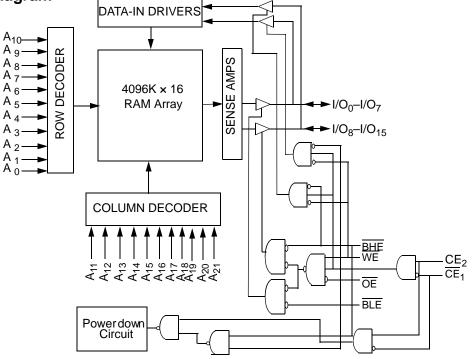




### Logic Block Diagram





# CY62187EV30 MoBL<sup>®</sup>

### Contents

Pin Configuration	4
Product Portfolio	4
Maximum Ratings	
Operating Range	
Electrical Characteristics	
Capacitance	
Thermal Resistance	
AC Test Loads and Waveforms	
Data Retention Characteristics	-
Data Retention Waveform	
Switching Characteristics	
Switching Waveforms	
Truth Table	

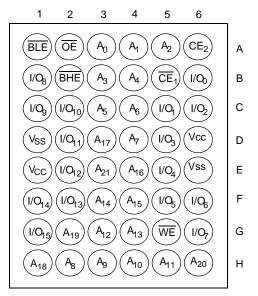
Ordering Information	13
Ordering Code Definitions	
Package Diagram	14
Acronyms	15
Document Conventions	15
Units of Measure	15
Document History Page	16
Sales, Solutions, and Legal Information	18
Worldwide Sales and Design Support	18
Products	18
PSoC® Solutions	18
Cypress Developer Community	18
Technical Support	18





### **Pin Configuration**

Figure 1. 48-ball FBGA pinout



### **Product Portfolio**

				Speed	Power Dissipation					
Product	v	V <sub>CC</sub> Range (V)			Operating I <sub>CC</sub> (mA)			Standby I ()		
				(ns)	f = 1 MHz f = f <sub>Max</sub>		Standby I <sub>SB2</sub> (μA)			
	Min	<b>Typ</b> <sup>[1]</sup>	Max		<b>Typ</b> <sup>[1]</sup>	Max	<b>Typ</b> <sup>[1]</sup>	Max	<b>Typ</b> <sup>[1]</sup>	Max
CY62187EV30LL	2.2	3.0	3.7	55	7.5	9	45	55	8	48

#### Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.



### **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature65 °C to +150 °C
Ambient Temperature with Power Applied
Supply Voltage to Ground Potential0.3 V to V <sub>CC(max)</sub> + 0.3 V
DC Voltage Applied to Outputs in High Z State $^{[2,\ 3]}$ 0.3 V to V_{CC(max)} + 0.3 V

DC Input Voltage $^{[2, 3]}$ 0.3 V to V <sub>CC (max)</sub> + 0.3 V
Output Current into Outputs (LOW)
Static Discharge Voltage (per MIL-STD-883, Method 3015) > 2001 V
Latch Up Current>200 mA

### **Operating Range**

Device	Range	Ambient Temperature	<b>V<sub>CC</sub></b> <sup>[4]</sup>
CY62187EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.7 V

### **Electrical Characteristics**

Over the Operating Range

Parameter	Description	Test Con	ditions		55 ns		Unit
Farameter	Description	Test Con		Min	<b>Typ</b> <sup>[5]</sup>	Max	Unit
V <sub>OH</sub>	Output HIGH voltage	$2.2 V \le V_{CC} \le 2.7 V$	$I_{OH} = -0.1 \text{ mA}$	2.0	-	-	V
		2.7 V <u>&lt;</u> V <sub>CC</sub> ≤ 3.7 V	I <sub>OH</sub> = -1.0 mA	2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	$2.2 V \le V_{CC} \le 2.7 V$	I <sub>OL</sub> = 0.1 mA	-	-	0.4	V
		2.7 V <u>&lt;</u> V <sub>CC</sub> ≤ 3.7 V	I <sub>OL</sub> = 2.1 mA	-	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage	$2.2 V \le V_{CC} \le 2.7 V_{CC}$	$2.2 \text{ V} \le \text{V}_{\text{CC}} \le 2.7 \text{ V}$		-	V <sub>CC</sub> + 0.3 V	V
		$2.7 \text{ V} \leq \text{V}_{CC} \leq 3.7 \text{ V}$		2.2	-	V <sub>CC</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW voltage	2.2 V≤ V <sub>CC</sub> ≤2.7 V		-0.3	-	0.6	V
		$2.7 \text{ V} \le \text{V}_{\text{CC}} \le 3.7 \text{ V}$	$2.7 \text{ V} \le \text{V}_{\text{CC}} \le 3.7 \text{ V}$		-	0.8 <sup>[6]</sup>	V
I <sub>IX</sub>	Input leakage current	$GND \leq V_I \leq V_{CC}$		-1	-	+1	μA
I <sub>OZ</sub>	Output leakage current	$GND \leq V_O \leq V_{CC}, c$	output disabled	-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	$f = f_{Max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$	-	45	55	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS levels	-	7.5	9	mA
I <sub>SB2</sub> <sup>[7]</sup>	Automatic CE power down current — CMOS inputs	$\frac{\overline{CE_{1}} \ge V_{CC} - 0.2 \text{ V c}}{(\text{BHE and BLE}) \ge \text{V}}$ $V_{\text{IN}} \ge V_{\text{CC}} - 0.2 \text{ V or}$ $V_{\text{CC}} = 3.7 \text{ V}$	′ <sub>CC</sub> – 0.2 V,	_	8	48	μΑ

- $V_{IL(min)}$  = -2.0V for pulse durations less than 20 ns. 2.

- V<sub>IL(min)</sub> = -2.0V to place durations less than 20 ns.
   V<sub>IL(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
   Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
   Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ), T<sub>A</sub> = 25 °C.
   Under DC conditions the device meets a V<sub>IL</sub> of 0.8 V. However, in dynamic conditions input LOW Voltage applied to the device must not be higher than 0.7 V.
   Chip enables (CE<sub>1</sub> and CE<sub>2</sub>), Address Pins A<sub>20</sub>, A<sub>21</sub> and Byte Enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB2</sub>/I<sub>CCDR</sub> spec. Other inputs can be left floating. be left floating.



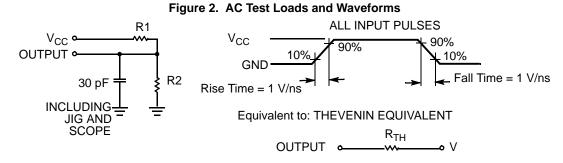
### Capacitance

Parameter <sup>[8]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = V_{CC(typ)}$	25	pF
C <sub>OUT</sub>	Output capacitance		35	pF

### **Thermal Resistance**

Parameter <sup>[8]</sup>	Description	Test Conditions	FBGA	Unit
JA	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	59.06	°C/W
- 30	Thermal resistance (junction to case)		14.08	°C/W

### **AC Test Loads and Waveforms**



### Table 1. AC Test Loads

Parameter	2.5 V	3.3 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

Note
 Tested initially and after any design or process changes that may affect these parameters.

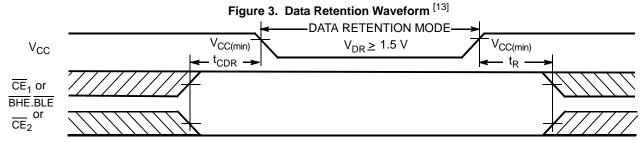


### **Data Retention Characteristics**

#### Over the Operating Range

Parameter	Description	Conditions	Min	<b>Typ</b> <sup>[9]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.5	-	_	V
I <sub>CCDR</sub> <sup>[10]</sup>	Data retention current	$\label{eq:constraint} \begin{array}{l} \frac{V_{CC}}{CE} = 1.5 \text{ V}, \\ \overline{CE}_{1} \geq V_{CC} - 0.2 \text{ V or } CE_{2} \leq 0.2 \text{ V or } \\ (BHE \text{ and } BLE) \geq V_{CC} - 0.2 \text{ V}, \\ \overline{V}_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V} \end{array}$	-	-	48	μΑ
t <sub>CDR</sub> <sup>[11]</sup>	Chip deselect to data retention time		0	-	_	ns
t <sub>R</sub> <sup>[12]</sup>	Operation recovery time		55	_	-	ns

### **Data Retention Waveform**



- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25 \,^{\circ}C$ . 10. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ), Address Pins A<sub>20</sub>, A<sub>21</sub> and Byte Enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can
- be left floating.
- 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub>  $\geq$  100  $\mu$ s or stable at V<sub>CC(min)</sub>  $\geq$  100  $\mu$ s. 13. BHE BLE is the AND of both BHE and BLE. Chip is deselected by either disabling the chip enable signals or by disabling both BHE and BLE.



### **Switching Characteristics**

Over the Operating Range

Parameter [14, 15]	Description	55	ns	Unit
Parameter [11, 10]	Description	Min	Max	Unit
Read Cycle		·		-
t <sub>RC</sub>	Read cycle time	55	-	ns
t <sub>AA</sub>	Address to data valid	-	55	ns
t <sub>OHA</sub>	Data hold from address change	6	-	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid	-	55	ns
t <sub>DOE</sub>	OE LOW to data valid	-	25	ns
t <sub>LZOE</sub>	OE LOW to LOW Z <sup>[16]</sup>	5	-	ns
t <sub>HZOE</sub>	OE HIGH to high Z <sup>[16, 17]</sup>	-	20	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH to low $Z^{[16]}$	10	-	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and $CE_2$ LOW to high $Z^{[16, 17]}$	-	20	ns
t <sub>PU</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to power up	0	-	ns
t <sub>PD</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to power down	-	55	ns
t <sub>DBE</sub>	BLE/BHE LOW to data valid	-	55	ns
t <sub>LZBE</sub>	BLE/BHE LOW to low Z [16]	10	-	ns
t <sub>HZBE</sub>	BLE/BHE HIGH to high Z [16, 17]	-	20	ns
Write Cycle <sup>[18]</sup>		·		
t <sub>WC</sub>	Write cycle time	55	-	ns
t <sub>SCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to write end	45	-	ns
t <sub>AW</sub>	Address setup to write end	45	-	ns
t <sub>HA</sub>	Address hold from write end	0	-	ns
t <sub>SA</sub>	Address setup to write start	0	-	ns
t <sub>PWE</sub>	WE pulse width	40	-	ns
t <sub>BW</sub>	BLE/BHE LOW to write end	45	-	ns
t <sub>SD</sub>	Data setup to write end	25	-	ns
t <sub>HD</sub>	Data hold from write end	0	-	ns
t <sub>HZWE</sub>	WE LOW to high Z <sup>[16, 17]</sup>	-	20	ns
t <sub>LZWE</sub>	WE HIGH to low Z <sup>[16]</sup>	10	-	ns

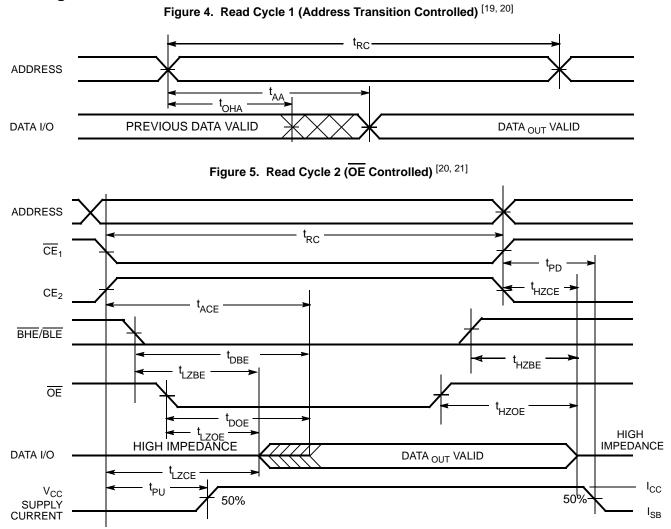
Notes

terminates the write.

<sup>Notes
14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V<sub>TH</sub>, input pulse levels of 0 to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in Figure 2 on page 6.
16. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
17. t<sub>HZOE</sub>, t<sub>HZDE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs <u>enter a high impedence state</u>.
18. The internal Write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.</sup> 



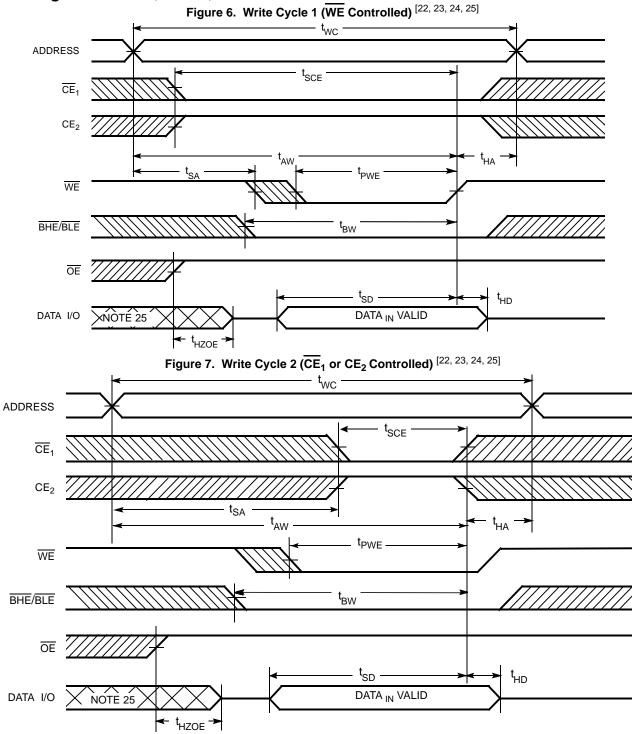
**Switching Waveforms** 



- 19. <u>The</u> device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . 20. WE is HIGH for read cycle.
- 21. Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.



### Switching Waveforms (continued)



- 22. The internal Write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE and/or BLE = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 23. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ . 24. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 25. During this period the I/Os are in output state and input signals should not be applied.



### Switching Waveforms (continued)

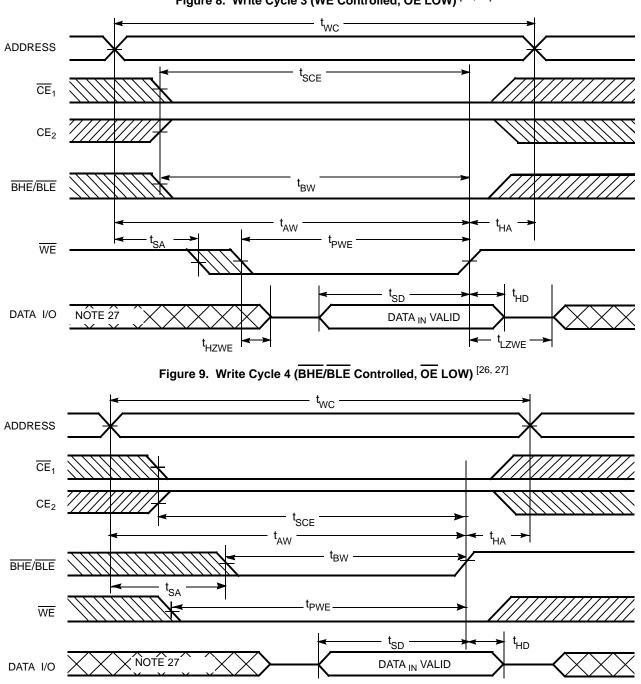


Figure 8. Write Cycle 3 (WE Controlled, OE LOW) <sup>[26, 27]</sup>

Notes 26. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state. 27. During this period the I/Os are in output state and input signals should not be applied.



### **Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	BHE	BLE	Inputs Outputs	Mode	Power
Н	X <sup>[28]</sup>	Х	Х	X <sup>[28]</sup>	X <sup>[28]</sup>	High Z	Deselect/Power Down	Standby (I <sub>SB</sub> )
X <sup>[28]</sup>	L	Х	Х	X <sup>[28]</sup>	X <sup>[28]</sup>	High Z	Deselect/Power Down	Standby (I <sub>SB</sub> )
X <sup>[28]</sup>	X <sup>[28]</sup>	Х	Х	Н	Н	High Z	Deselect/Power Down	Standby (I <sub>SB</sub> )
L	Н	Н	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	L	Н	L	High Z (I/O <sub>8</sub> –I/O <sub>15</sub> ); Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	L	L	Н	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); High Z (I/O <sub>0</sub> –I/O <sub>7</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	L	Х	L	L	Data In (I/O <sub>0</sub> -I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	L	Х	Н	L	High Z (I/O <sub>8</sub> –I/O <sub>15</sub> ); Data In (I/O <sub>0</sub> –I/O <sub>7</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	L	Х	L	Н	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); High Z (I/O <sub>0</sub> –I/O <sub>7</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	Н	Н	L	Н	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	Н	Н	Н	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	Н	Н	L	L	High Z	Output Disabled	Active (I <sub>CC</sub> )

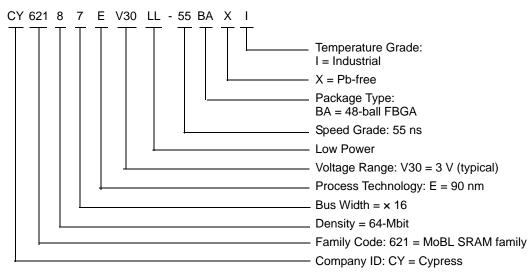
Note 28. The 'X' (Don't care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



### **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62187EV30LL-55BAXI	001-50044	48-ball FBGA (8 × 9.5 × 1.4 mm) Pb-free	Industrial

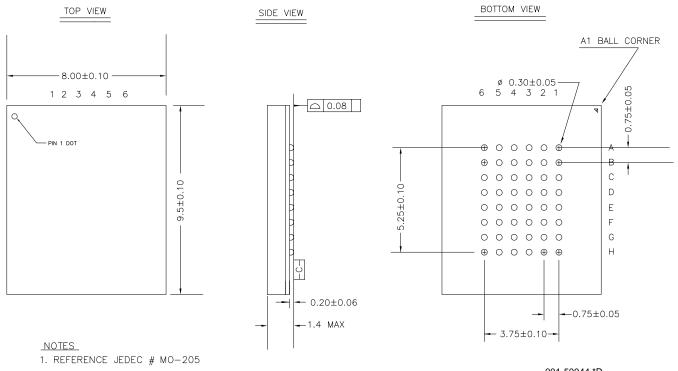
### **Ordering Code Definitions**





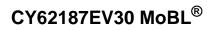
### Package Diagram

Figure 10. 48-ball FBGA (8 × 9.5 × 1.4 mm) BK48L Package Outline, 001-50044



2. ALL DIMENSIONS ARE IN MILLIMETERS

001-50044 \*D





### Acronyms

Acronym	Description			
BHE	Byte High Enable			
BLE	Byte Low Enable			
CMOS	Complementary Metal Oxide Semiconductor			
CE	Chip Enable			
FBGA	Fine-Pitch Ball Grid Array			
I/O	Input/Output			
OE	Output Enable			
SRAM	Static Random Access Memory			
WE	Write Enable			

### **Document Conventions**

### **Units of Measure**

Symbol	Unit of Measure			
°C	degree Celsius			
MHz	megahertz			
μΑ	microampere			
mA	milliampere			
ms	millisecond			
ns	nanosecond			
Ω	ohms			
%	percent			
pF	picofarad			
V	volt			
W	watt			





## **Document History Page**

Document Title: CY62187EV30 MoBL <sup>®</sup> , 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2595932	VKN / PYRS	10/24/08	New data sheet
*A	2644442	VKN / PYRS	01/23/09	Updated the Package diagram on page 10
*В	2672650	VKN / PYRS	03/12/09	Extended the V <sub>CC</sub> range to 3.7V Added 55 ns speed bin and it's related information Changed I <sub>CC</sub> (typ) from 2.5 mA to 3.5 mA at f = 1 MHz Changed I <sub>CC</sub> (max) from 4 mA to 6 mA at f = 1 MHz For 70 ns speed, changed I <sub>CC</sub> (typ) form 33 mA to 28 mA at f = f <sub>MAX</sub> For 70 ns speed, changed I <sub>CC</sub> (max) from 40 mA to 45 mA at f = f <sub>MAX</sub> For 70 ns speed, changed t <sub>CC</sub> (max) from 45 to 50 ns, t <sub>SD</sub> from 30 to 35 ns Modified footnote #6 Changed 48-Ball FBGA package dimensions from 8 x 9.5 x 1.6 mm to 8 x 9.5 x 1.4 mm and updated package diagram on page 10
*C	2737164	VKN/AESA	07/13/09	Converted from preliminary to final Changed I <sub>CC(typ)</sub> from 3.5 mA to 4 mA at f = 1 MHz Changed I <sub>CC(typ)</sub> from 35 mA to 45 mA and from 28 mA to 35 mA for the speeds 50 ns and 70 ns respectively at f = f <sub>max</sub> Included V <sub>CC</sub> range in the test condition of the "Electrical Characteristics" table for the specs V <sub>OH</sub> , V <sub>OL</sub> , V <sub>IH</sub> , V <sub>IL</sub> Changed V <sub>IL(max)</sub> from 0.8V to 0.7V for V <sub>CC</sub> = 2.7V to 3.7V Changed C <sub>IN</sub> spec from 20 pF to 25 pF and C <sub>OUT</sub> spec from 20 pF to 35 pF Included thermal specs for 48-FBGA Included V <sub>CC</sub> range for V <sub>TH</sub> spec in the AC test load table Changed t <sub>LZBE</sub> spec from 5 ns to 10 ns Added footnote #20 related to chip enable
*D	2765892	VKN	09/18/09	Removed 70 ns speed For 55 ns speed, at f = 1 MHz, changed $I_{CC (max)}$ spec from 6 mA to 9 mA Changed $I_{CC(typ)}$ from 4 mA to 7.5 mA at f = 1 MHz
*E	3177000	AJU	02/18/2011	Updated Features (Corrected $I_{CC(typ)}$ from 4 mA to 7.5 mA). Updated Pin Configuration (Renamed Figure 1 as "48-ball FBGA"). Updated Product Portfolio (Corrected $I_{CC(typ)}$ from 4 mA to 7.5 mA). Updated Electrical Characteristics (Included BHE and BLE in $I_{SB2}$ test conditions to reflect Byte power down feature). Updated Table 1 on page 6 (AC Test Loads). Updated Data Retention Characteristics (Included BHE and BLE in $I_{CCDR}$ test conditions to reflect Byte power down feature, corrected $t_{R(min)}$ from $t_{RC}$ to 55 ns). Added Ordering Code Definitions. Updated Package Diagram. Added Acronyms and Units of Measure. Changed all instances of IO to I/O. Updated in new template.
*F	3282088	RAME	06/14/2011	Updated template as per current Cypress standards. Removed reference to AN1064 SRAM system guidelines. Changed the V <sub>IL</sub> parameter max value to 0.8 V for test condition 2.7 V $\leq$ V <sub>CC</sub> $\leq$ 3.7 V and referenced to footnote # 6.
*G	3785005	TAVA	10/18/2012	Minor Text Modifications. Updated Package Diagram (from Rev *C to *D).



## Document History Page (continued)

Document Title: CY62187EV30 MoBL <sup>®</sup> , 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998					
Revision	ECN	Orig. of Change	Submission Date	Description of Change	
*H	4101127	VINI	08/21/2013	Updated Switching Characteristics: Added Note 14 and referred the same note in "Parameter" column. Updated in new template. Completing Sunset Review.	
*	4114808	NILE	09/12/2013	Updated Electrical Characteristics: Updated Note 7. Updated Data Retention Characteristics: Updated Note 10.	



### Sales, Solutions, and Legal Information

#### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products	
Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

### **PSoC<sup>®</sup> Solutions**

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community Community | Forums | Blogs | Video | Training

Technical Support cypress.com/go/support

© Cypress Semiconductor Corporation, 2008-2013. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

#### Document Number: 001-48998 Rev. \*I

#### Revised September 12, 2013

Page 18 of 18

MoBL is a registered trademark, and More Battery Life is a trademark, of Cypress Semiconductor. All products and company names mentioned in this document may be the trademarks of their respective holders.

# **Mouser Electronics**

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Cypress Semiconductor: CY62187EV30LL-55BAXIT