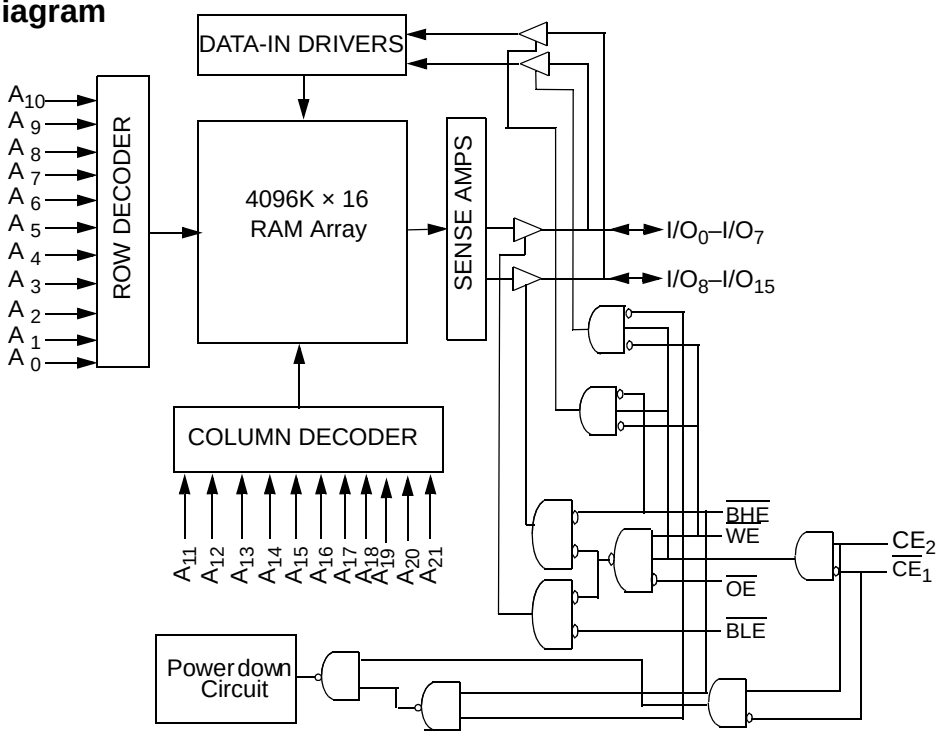
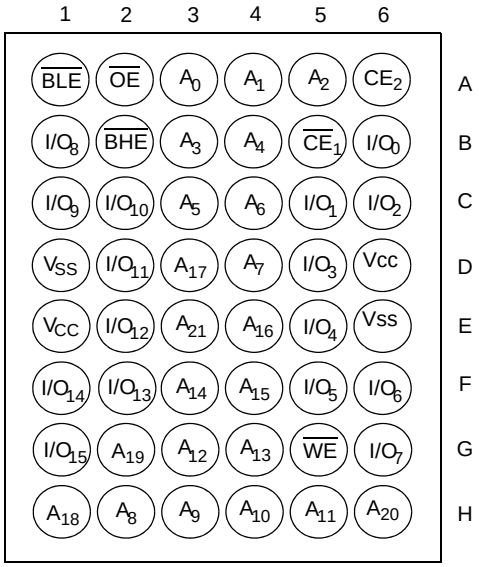
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 48-ball FBGA pinout



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ[1]	Max		Typ[1]	Max	Typ[1]	Max	Typ[1]	Max
CY62187EV30LL	2.2	3.0	3.7	55	7.5	9	45	55	8	48

Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC Voltage Applied to Outputs in High Z State [2, 3] ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC Input Voltage [2, 3] ..... –0.3 V to $V_{CC\ (max)}$ + 0.3 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[4]
CY62187EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.7 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ [5]	Max	
V_{OH}	Output HIGH voltage	2.2 V ≤ V_{CC} ≤ 2.7 V	I_{OH} = –0.1 mA	2.0	–	–	V
		2.7 V ≤ V_{CC} ≤ 3.7 V	I_{OH} = –1.0 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	2.2 V ≤ V_{CC} ≤ 2.7 V	I_{OL} = 0.1 mA	–	–	0.4	V
		2.7 V ≤ V_{CC} ≤ 3.7 V	I_{OL} = 2.1 mA	–	–	0.4	V
V_{IH}	Input HIGH voltage	2.2 V ≤ V_{CC} ≤ 2.7 V		1.8	–	V_{CC} + 0.3 V	V
		2.7 V ≤ V_{CC} ≤ 3.7 V		2.2	–	V_{CC} + 0.3 V	V
V_{IL}	Input LOW voltage	2.2 V≤ V_{CC} ≤ 2.7 V		–0.3	–	0.6	V
		2.7 V ≤ V_{CC} ≤ 3.7 V		–0.3	–	0.8[6]	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{Max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	45	55	mA
		f = 1 MHz		–	7.5	9	mA
I_{SB2} [7]	Automatic CE power down current — CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V or (BHE and BLE) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.7 V		–	8	48	µA

Notes

2. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
3. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
4. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
6. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions input LOW Voltage applied to the device must not be higher than 0.7 V.
7. Chip enables ($\overline{CE_1}$ and CE_2), Address Pins A_{20}, A_{21} and Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	25	pF
C_{OUT}	Output capacitance		35	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	FBGA	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	59.06	°C/W
θ_{JC}	Thermal resistance (junction to case)		14.08	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

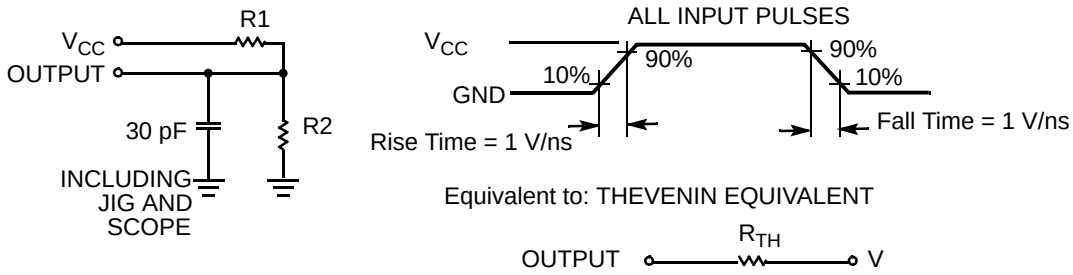


Table 1. AC Test Loads

Parameter	2.5 V	3.3 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

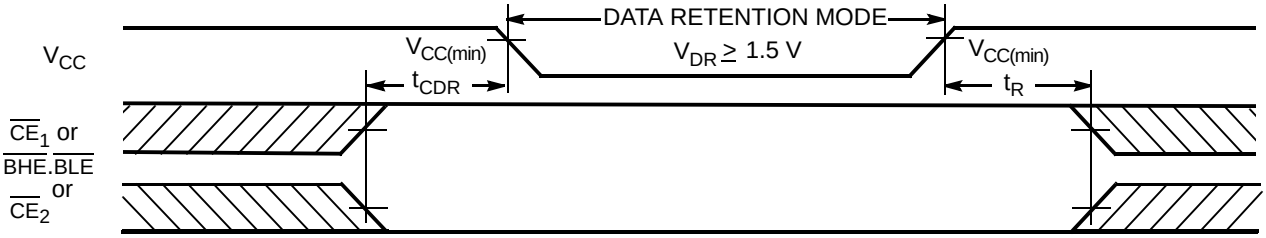
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} [10]	Data retention current	V_{CC} = 1.5 V, $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	48	µA
t_{CDR} [11]	Chip deselect to data retention time		0	–	–	ns
t_R [12]	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform [13]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enables ($\overline{CE_1}$ and CE_2), Address Pins A_{20}, A_{21} and Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip is deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	6	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[16, 17]	–	20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to low Z[16]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to high Z[16, 17]	–	20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power down	–	55	ns
t_{DBE}	BLE/BHE LOW to data valid	–	55	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z [16]	10	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z [16, 17]	–	20	ns
Write Cycle[18]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	45	–	ns
t_{AW}	Address setup to write end	45	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	45	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[16, 17]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[16]	10	–	ns

Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V_{TH}, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 6.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
18. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [19, 20]

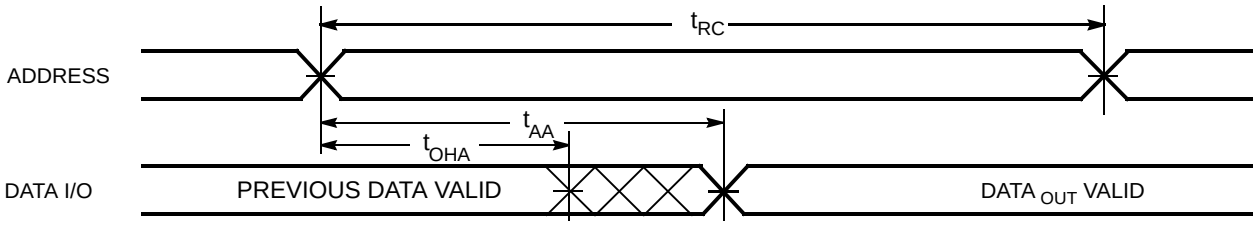
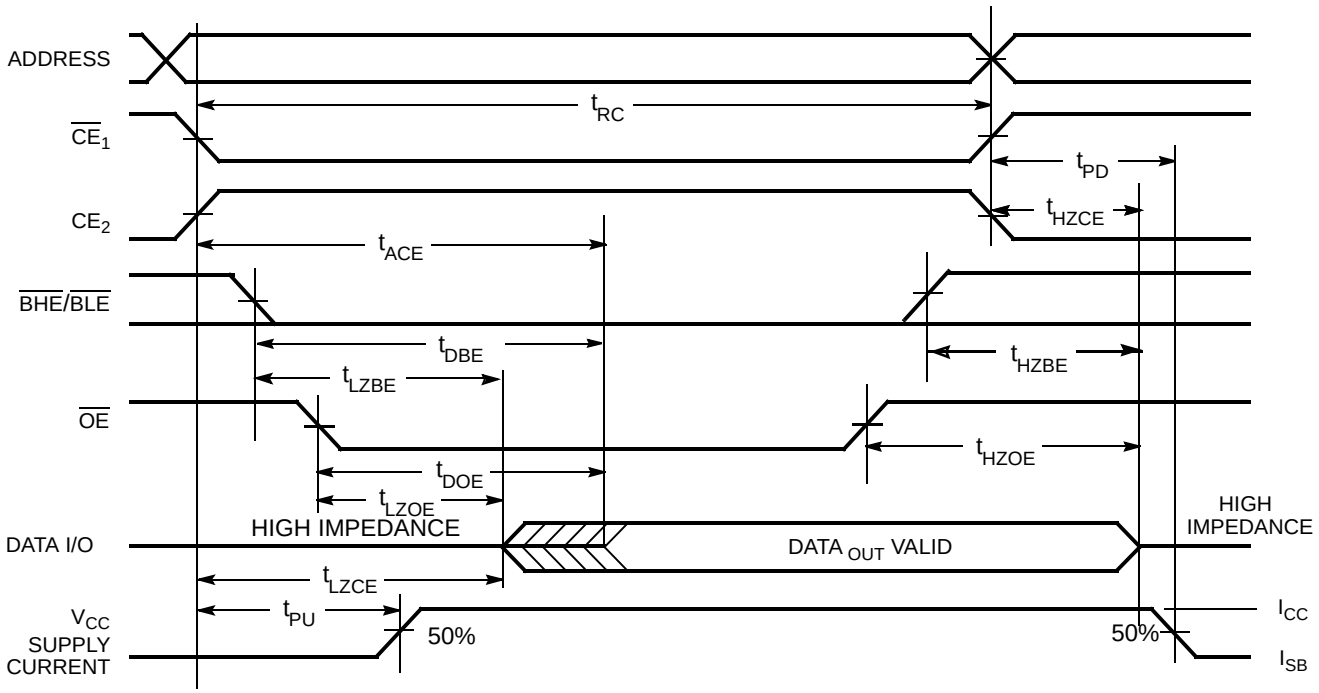


Figure 5. Read Cycle 2 ($\overline{OE}$ Controlled) [20, 21]



Notes
19. The device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms *(continued)*

Figure 6. Write Cycle 1 ($\overline{WE}$ Controlled) [22, 23, 24, 25]

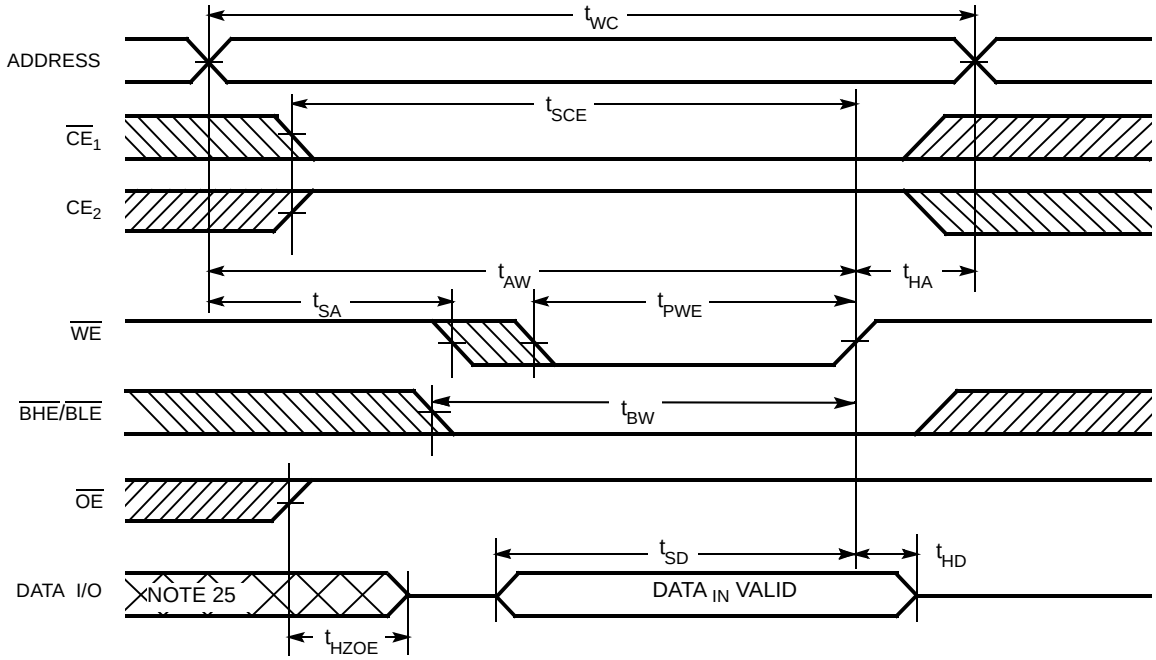
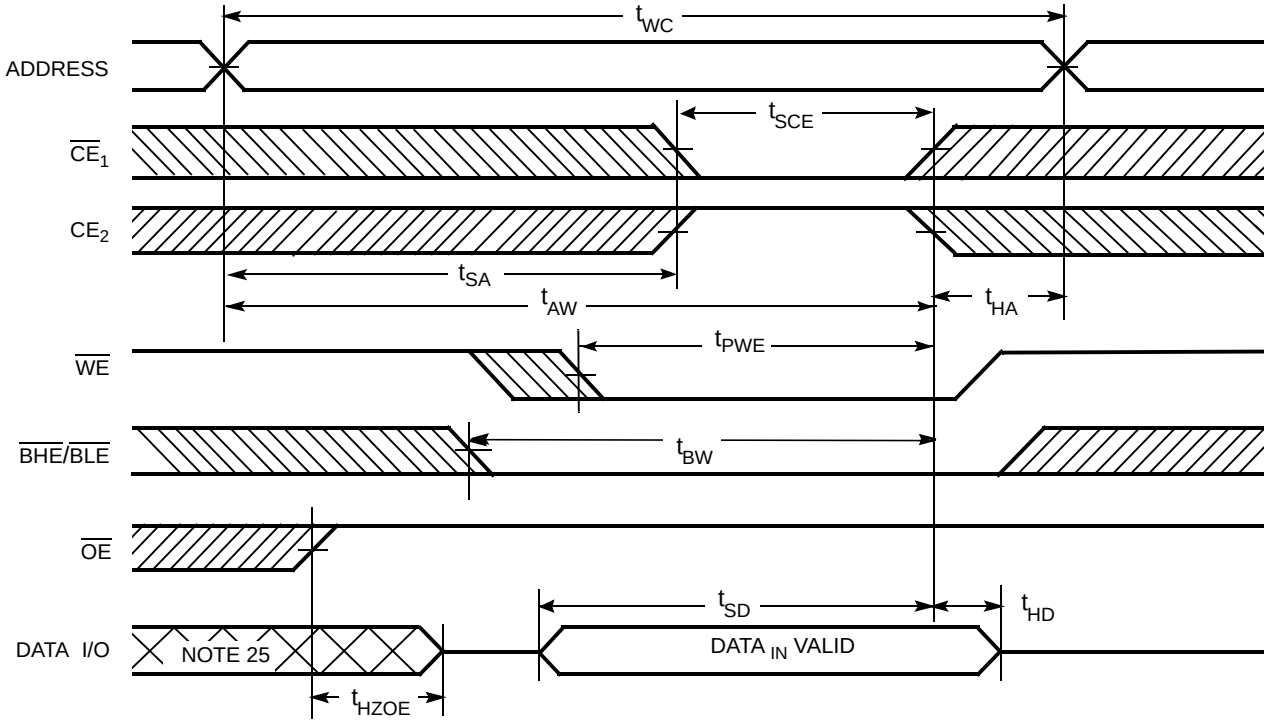


Figure 7. Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled) [22, 23, 24, 25]



Notes

22. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
25. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms *(continued)*

Figure 8. Write Cycle 3 (WE Controlled, OE LOW) [26, 27]

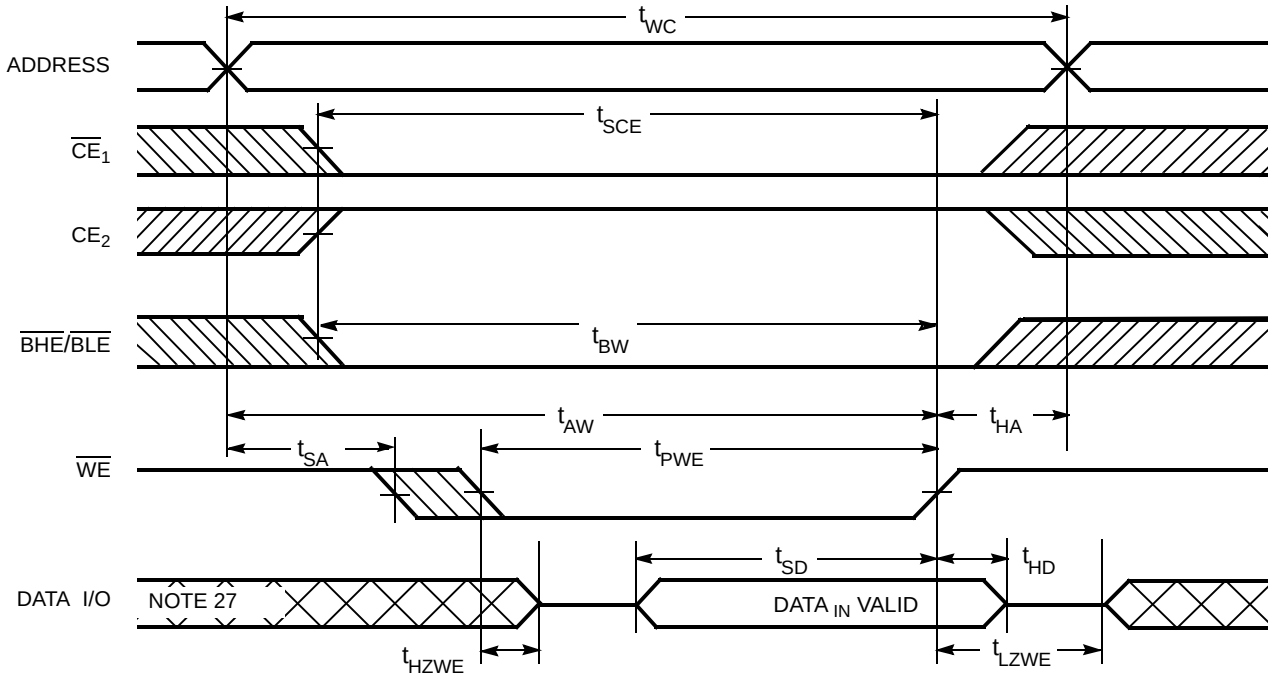
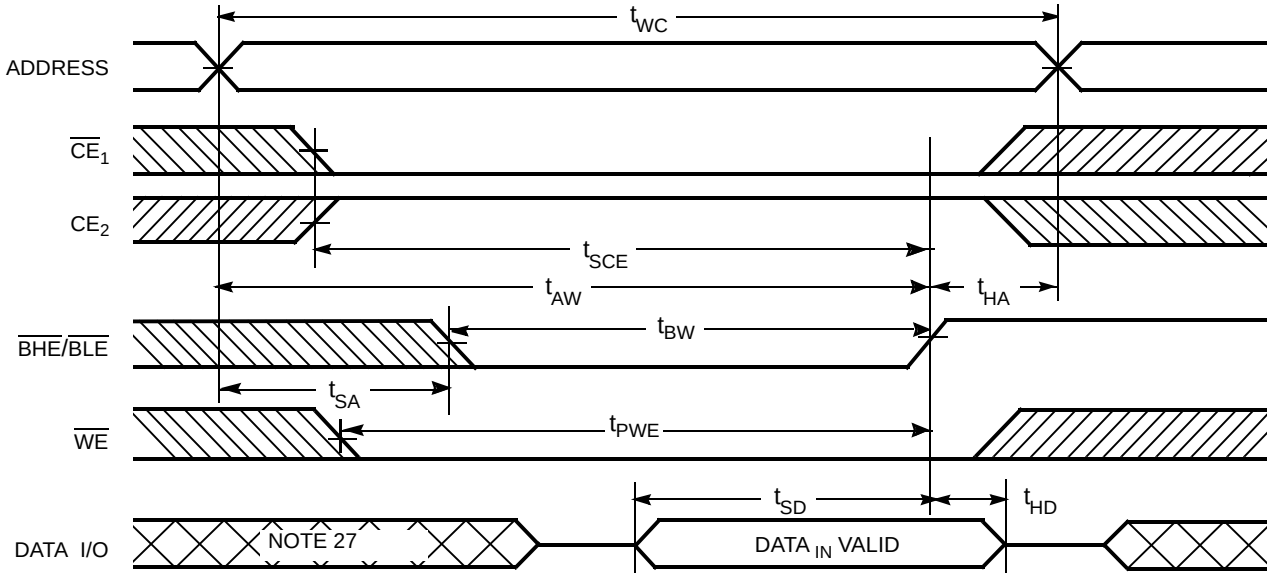


Figure 9. Write Cycle 4 (BHE/BLE Controlled, OE LOW) [26, 27]



Notes
26. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
27. During this period the I/Os are in output state and input signals should not be applied.

Truth Table

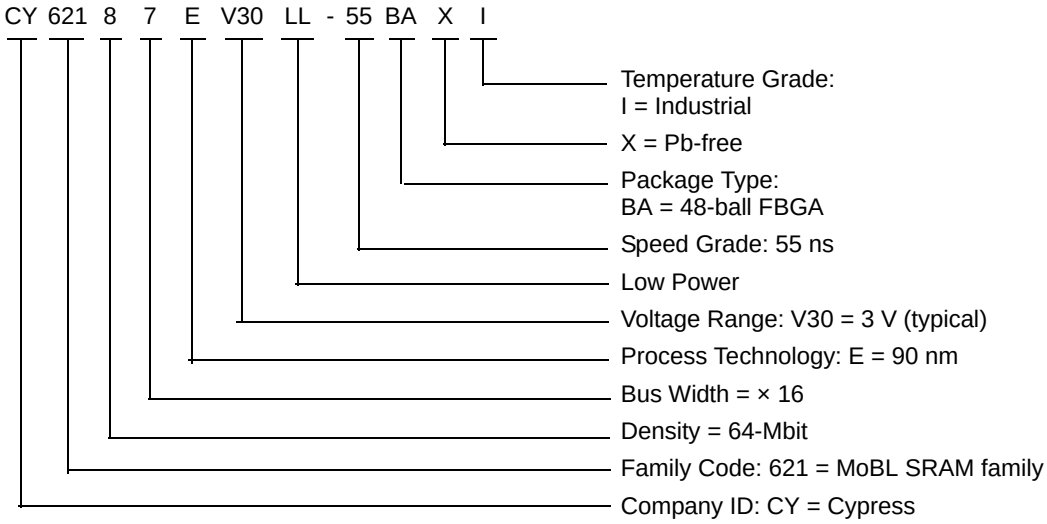
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X[28]	X	X	X[28]	X[28]	High Z	Deselect/Power Down	Standby (I_{SB})
X[28]	L	X	X	X[28]	X[28]	High Z	Deselect/Power Down	Standby (I_{SB})
X[28]	X[28]	X	X	H	H	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High Z (I/O_8–I/O_{15}); Data Out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High Z (I/O_8–I/O_{15}); Data In (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8–I/O_{15}); High Z (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})

Note
28. The 'X' (Don't care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

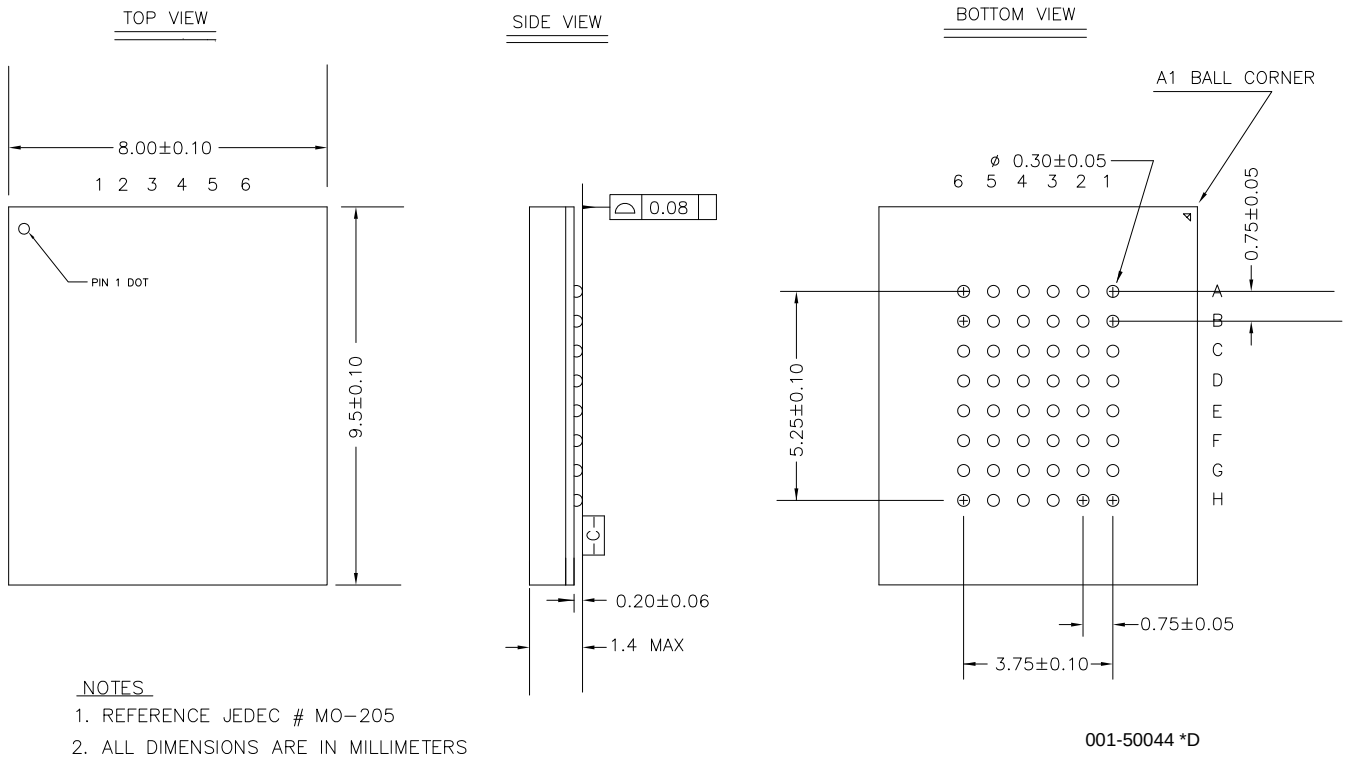
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62187EV30LL-55BAXI	001-50044	48-ball FBGA (8 × 9.5 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagram

Figure 10. 48-ball FBGA (8 × 9.5 × 1.4 mm) BK48L Package Outline, 001-50044



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohms
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62187EV30 MoBL®, 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2595932	VKN / PYRS	10/24/08	New data sheet
*A	2644442	VKN / PYRS	01/23/09	Updated the Package diagram on page 10
*B	2672650	VKN / PYRS	03/12/09	Extended the V_{CC} range to 3.7V Added 55 ns speed bin and it's related information Changed $I_{CC\ (typ)}$ from 2.5 mA to 3.5 mA at f = 1 MHz Changed $I_{CC\ (max)}$ from 4 mA to 6 mA at f = 1 MHz For 70 ns speed, changed $I_{CC\ (typ)}$ form 33 mA to 28 mA at f = f_{MAX} For 70 ns speed, changed $I_{CC\ (max)}$ from 40 mA to 45 mA at f = f_{MAX} For 70 ns speed, changed t_{PWE} from 45 to 50 ns, t_{SD} from 30 to 35 ns Modified footnote #6 Changed 48-Ball FBGA package dimensions from 8 x 9.5 x 1.6 mm to 8 x 9.5 x 1.4 mm and updated package diagram on page 10
*C	2737164	VKN/AESA	07/13/09	Converted from preliminary to final Changed $I_{CC(typ)}$ from 3.5 mA to 4 mA at f = 1 MHz Changed $I_{CC(typ)}$ from 35 mA to 45 mA and from 28 mA to 35 mA for the speeds 50 ns and 70 ns respectively at f = f_{max} Included V_{CC} range in the test condition of the "Electrical Characteristics" table for the specs V_{OH}, V_{OL}, V_{IH}, V_{IL} Changed $V_{IL(max)}$ from 0.8V to 0.7V for V_{CC} = 2.7V to 3.7V Changed C_{IN} spec from 20 pF to 25 pF and C_{OUT} spec from 20 pF to 35 pF Included thermal specs for 48-FBGA Included V_{CC} range for V_{TH} spec in the AC test load table Changed t_{LZBE} spec from 5 ns to 10 ns Added footnote #20 related to chip enable
*D	2765892	VKN	09/18/09	Removed 70 ns speed For 55 ns speed, at f = 1 MHz, changed $I_{CC\ (max)}$ spec from 6 mA to 9 mA Changed $I_{CC(typ)}$ from 4 mA to 7.5 mA at f = 1 MHz
*E	3177000	AJU	02/18/2011	Updated Features (Corrected $I_{CC(typ)}$ from 4 mA to 7.5 mA). Updated Pin Configuration (Renamed Figure 1 as "48-ball FBGA"). Updated Product Portfolio (Corrected $I_{CC(typ)}$ from 4 mA to 7.5 mA). Updated Electrical Characteristics (Included $\overline{BHE}$ and $\overline{BLE}$ in I_{SB2} test conditions to reflect Byte power down feature). Updated Table 1 on page 6 (AC Test Loads). Updated Data Retention Characteristics (Included $\overline{BHE}$ and $\overline{BLE}$ in I_{CCDR} test conditions to reflect Byte power down feature, corrected $t_{R(min)}$ from t_{RC} to 55 ns). Added Ordering Code Definitions. Updated Package Diagram. Added Acronyms and Units of Measure. Changed all instances of IO to I/O. Updated in new template.
*F	3282088	RAME	06/14/2011	Updated template as per current Cypress standards. Removed reference to AN1064 SRAM system guidelines. Changed the V_{IL} parameter max value to 0.8 V for test condition 2.7 V $\leq V_{CC} \leq$ 3.7 V and referenced to footnote # 6.
*G	3785005	TAVA	10/18/2012	Minor Text Modifications. Updated Package Diagram (from Rev *C to *D).

Document History Page *(continued)*

Document Title: CY62187EV30 MoBL®, 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	4101127	VINI	08/21/2013	Updated Switching Characteristics: Added Note 14 and referred the same note in “Parameter” column. Updated in new template. Completing Sunset Review.
*I	4114808	NILE	09/12/2013	Updated Electrical Characteristics: Updated Note 7. Updated Data Retention Characteristics: Updated Note 10.

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