1 Overview

The MPC8306S incorporates the e300c3 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8306S also includes two DMA engines and a 16-bit DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8306S. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8306S is shown in the following figure.

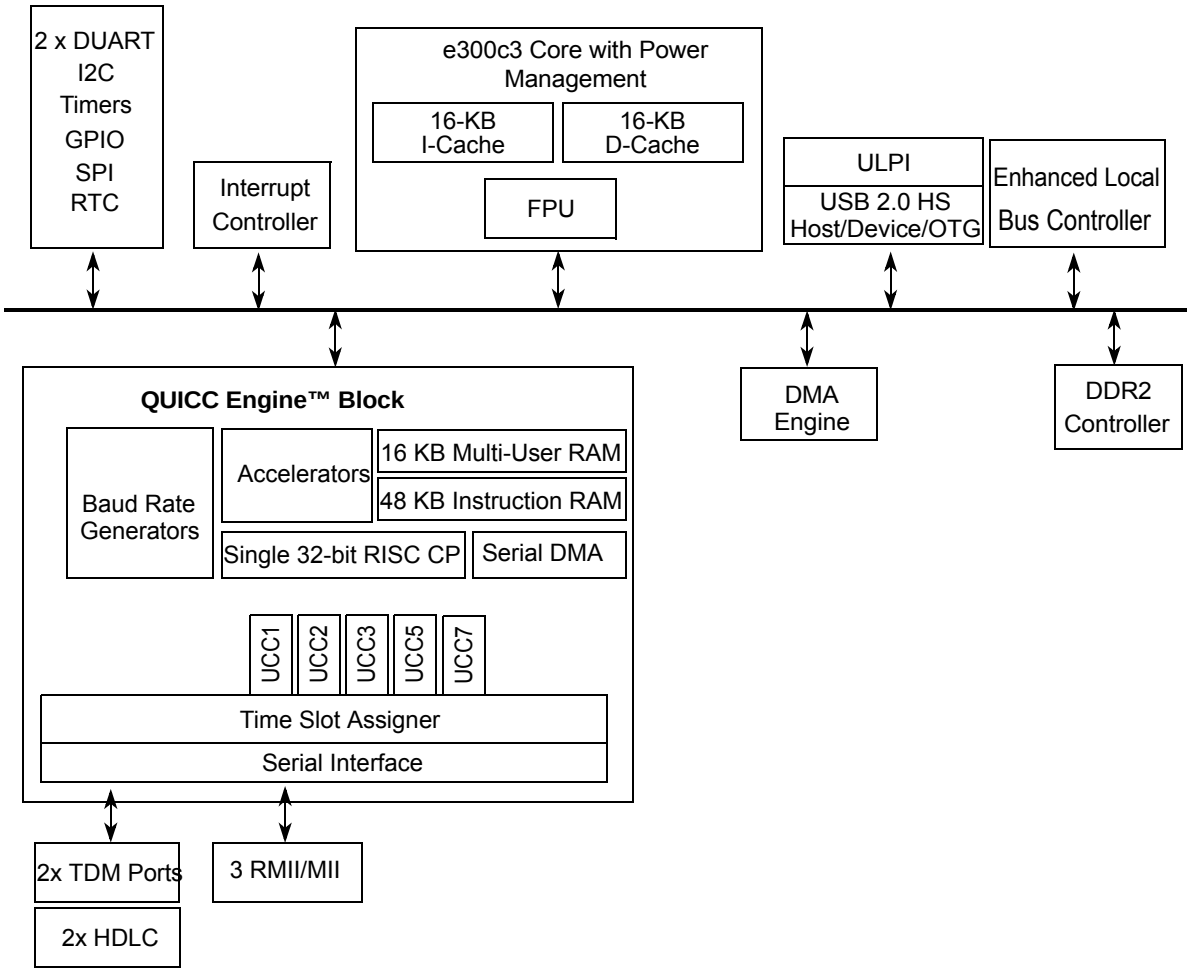


Figure 1. MPC8306S Block Diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8306S provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 Features

The major features of the device are as follows:

- e300c3 Power Architecture processor core
  - Enhanced version of the MPC603e core
  - High-performance, superscalar processor core with a four-stage pipeline and low interrupt latency times
  - Floating-point, dual integer units, load/store, system register, and branch processing units
  - 16-Kbyte instruction cache and 16-Kbyte data cache with lockable capabilities
  - Dynamic power management
  - Enhanced hardware program debug features
  - Software-compatible with Freescale processor families implementing Power Architecture technology
  - Separate PLL that is clocked by the system bus clock
  - Performance monitor
- QUICC Engine block
  - 32-bit RISC controller for flexible support of the communications peripherals with the following features:
    - One clock per instruction
    - Separate PLL for operating frequency that is independent of system's bus and e300 core frequency for power and performance optimization
    - 32-bit instruction object code
    - Executes code from internal IRAM
    - 32-bit arithmetic logic unit (ALU) data path
    - Modular architecture allowing for easy functional enhancements
    - Slave bus for CPU access of registers and multiuser RAM space
    - 48 Kbytes of instruction RAM
    - 16 Kbytes of multiuser data RAM
    - Serial DMA channel for receive and transmit on all serial channels
  - Five unified communication controllers (UCCs) supporting the following protocols and interfaces:
    - 10/100 Mbps Ethernet/IEEE Std. 802.3® through MII and RMII interfaces.
    - HDLC/Transparent (bit rate up to QUICC Engine operating frequency / 8)
    - HDLC Bus (bit rate up to 10 Mbps)
    - Asynchronous HDLC (bit rate up to 2 Mbps)

- Two TDM interfaces supporting up to 128 QUICC multichannel controller channels, each running at 64 kbps

For more information on QUICC Engine sub-modules, see *QUICC Engine Block Reference Manual with Protocol Interworking*.

- DDR SDRAM memory controller
  - Programmable timing supporting DDR2 SDRAM
  - Integrated SDRAM clock generation
  - 16-bit data interface, up to 266-MHz data rate
  - 14 address lines
  - The following SDRAM configurations are supported:
    - Up to two physical banks (chip selects), 256-Mbyte per chip select for 16 bit data interface.
    - 64-Mbit to 2-Gbit devices with x8/x16 data ports (no direct x4 support)
    - One 16-bit device or two 8-bit devices on a 16-bit bus,
  - Support for up to 16 simultaneous open pages for DDR2
  - One clock pair to support up to 4 DRAM devices
  - Supports auto refresh
  - On-the-fly power management using CKE
- Enhanced local bus controller (eLBC)
  - Multiplexed 26-bit address and 8-/16-bit data operating at up to 66 MHz
  - Eight chip selects supporting eight external slaves
    - Four chip selects dedicated
    - Four chip selects offered as multiplexed option
  - Supports boot from parallel NOR Flash and parallel NAND Flash
  - Supports programmable clock ratio dividers
  - Up to eight-beat burst transfers
  - 16- and 8-bit ports, separate $\overline{\text{LWE}}$ for each 8 bit
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - NAND Flash control machine (FCM)
  - Variable memory block sizes for FCM, GPCM, and UPM mode
  - Default boot ROM chip select with configurable bus width (8 or 16)
  - Provides two Write Enable signals to allow single byte write access to external 16-bit eLBC slave devices
- Integrated programmable interrupt controller (IPIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for external and internal discrete interrupt sources
  - Programmable highest priority request

  - Six groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Unique vector number for each interrupt source
- Universal serial bus (USB) dual-role controller
  - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - Supports operation as a stand-alone USB host controller
  - Supports operation as a stand-alone USB device
  - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- Dual I^2C interfaces
  - Two-wire interface
  - Multiple-master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - I^2C1 can be used as the boot sequencer
- DMA Engine
  - Support for the DMA engine with the following features:
    - Sixteen DMA channels
    - All data movement via dual-address transfers: read from source, write to destination
    - Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
    - Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
      - Explicit software initiation
      - Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
    - Support for fixed-priority and round-robin channel arbitration
    - Channel completion reported via optional interrupt requests
  - Support for scatter/gather DMA processing
- DUART
  - Two 2-wire interfaces (RxD, TxD)
    - The same can be configured as one 4-wire interface (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI)
  - Master or slave support
- Power managemnt controller (PMC)
  - Supports core doze/nap/sleep/ power management
  - Exits low power state and returns to full-on mode when
    - The core internal time base unit invokes a request to exit low power state

  - The power management controller detects that the system is not idle and there are outstanding transactions on the internal bus or an external interrupt.
- Parallel I/O
  - General-purpose I/O (GPIO)
    - 56 parallel I/O pins multiplexed on various chip interfaces
    - Interrupt capability
- System timers
  - Periodic interrupt timer
  - Software watchdog timer
  - Eight general-purpose timers
- Real time clock (RTC) module
  - Maintains a one-second count, unique over a period of thousands of years
  - Two possible clock sources:
    - External RTC clock (RTC_PIT_CLK)
    - CSB bus clock
- IEEE Std. 1149.1™ compliant JTAG boundary scan

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8306S. The MPC8306S is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage	AV_{DD1} AV_{DD2} AV_{DD3}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 1.98	V	—
Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, USB and JTAG I/O voltage	OV_{DD}	–0.3 to 3.6	V	2

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	3
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.
3. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

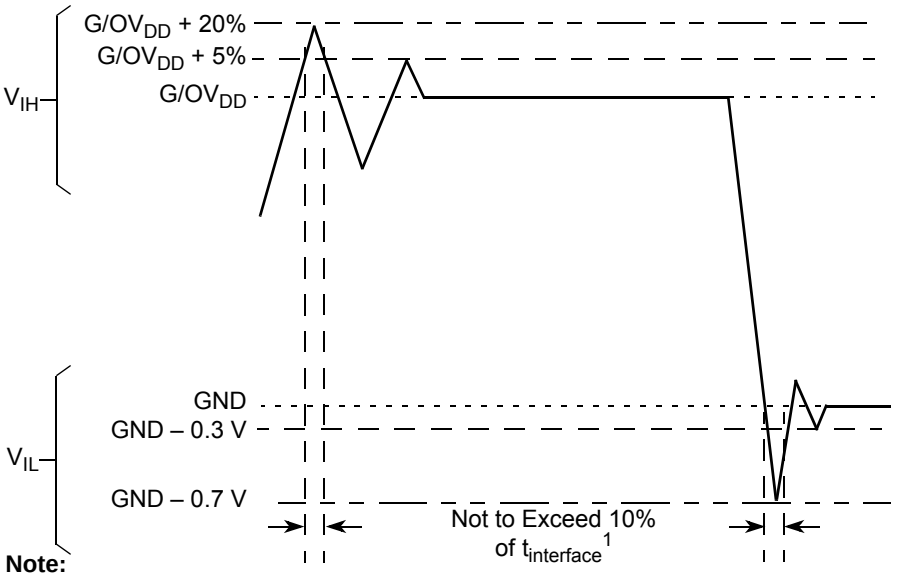
The following table provides the recommended operating conditions for the MPC8306S. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV_{DD1} AV_{DD2} AV_{DD3}	1.0 V ± 50 mV	V	1
DDR2 DRAM I/O voltage	GV_{DD}	1.8 V ± 100 mV	V	1
Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, USB and JTAG I/O voltage	OV_{DD}	3.3 V ± 300 mV	V	1, 3
Junction temperature	T_A/T_J	0 to 105	°C	2

Notes:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Minimum temperature is specified with T_A(Ambient Temperature); maximum temperature is specified with T_J(Junction Temperature).
3. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8306S



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}

2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage (V)
Local bus interface utilities signals	42	OV_{DD} = 3.3
DDR2 signal	18	GV_{DD} = 1.8
DUART, system control, I2C, SPI, JTAG	42	OV_{DD} = 3.3
GPIO signals	42	OV_{DD} = 3.3

2.1.4 Input Capacitance Specification

The following table describes the input capacitance for the SYS_CLK_IN pin in the MPC8306S.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input capacitance for all pins except SYS_CLK_IN and QE_CLK_IN	C_I	6	8	pF	—
Input capacitance for SYS_CLK_IN and QE_CLK_IN	C_{ICLK_IN}	10	—	pF	1

Note:
1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and I/O supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

NOTE

There is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

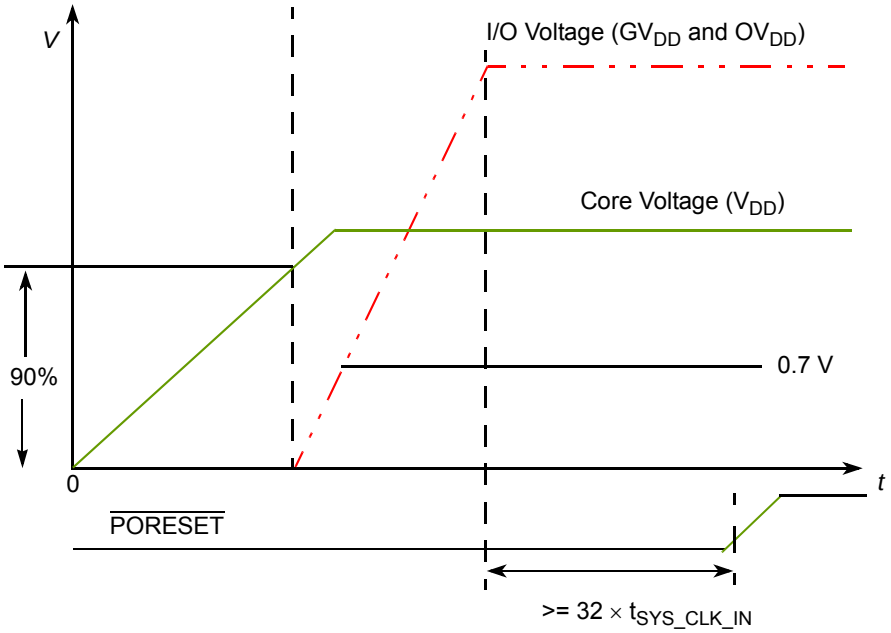


Figure 3. MPC8306S Power-Up Sequencing Example

3 Power Characteristics

The typical power dissipation for this family of MPC8306S devices is shown in the following table.

Table 5. MPC8306S Power Dissipation

Core Frequency (MHz)	QUICC Engine Frequency (MHz)	CSB Frequency (MHz)	Typical	Maximum	Unit	Note
133	133	133	0.272	0.618	W	1, 2, 3
200	233	133	0.291	0.631	W	1, 2, 3
266	233	133	0.451	0.925	W	1, 2, 3
333	233	133	0.471	0.950	W	1, 2, 3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}), but it does include V_{DD} and AV_{DD} power. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.
3. Maximum power is based on a voltage of V_{DD} = 1.05 V, WC process, a junction T_J = 105°C, and a smoke test code.

The following table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 1.8 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 16 bits	0.141	—	W	—
Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 26 bits	—	0.150	W	1
QUICC Engine block and other I/Os	TDM serial, HDLC/TRAN serial, DUART, MII, RMII, Ethernet management, USB, SPI, Timer output,				

Note:
1. Typical I/O power is based on a nominal voltage of V_{DD} = 3.3V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8306S.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of OV_{DD}; fall time refers to transitions from 90% to 10% of OV_{DD}.

4.1 DC Electrical Characteristics

The following table provides the clock input (SYS_CLK_IN) DC specifications for the MPC8306S. These specifications are also applicable for QE_CLK_IN.

Table 7. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0.5 V ≤ V_{IN} ≤ OV_{DD} – 0.5 V	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8306S is SYS_CLK_IN. The following table provides the clock input (SYS_CLK_IN) AC timing specifications for the MPC8306S. These specifications are also applicable for QE_CLK_IN.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1
SYS_CLK_IN cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	1.1	—	2.8	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.33 and 2.97 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33kHz (max rate).

5 RESET Initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8306S. The following table provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{SYS\_CLK\_IN}$	1
Required assertion time of PORESET with stable clock applied to SYS_CLK_IN	32	—	$t_{SYS\_CLK\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS\_CLK\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of $\overline{\text{PORESET}}$	4	—	$t_{SYS\_CLK\_IN}$	1, 2
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	1, 2

Notes:
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. For more details, see the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.
2. POR configuration signals consist of CFG_RESET_SOURCE[0:3].

The following table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8306S. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8306S when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MVREF is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.100 V, f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM (GV_{DD}(typ) = 1.8 V).

Table 14. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.25	V	—
AC input high voltage	V_{IH}	MVREF + 0.25	—	V	—

The following table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 15. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2

Table 15. DDR2 SDRAM Input AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
266 MHz		–750	750		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

The following figure shows the input timing diagram for the DDR controller.

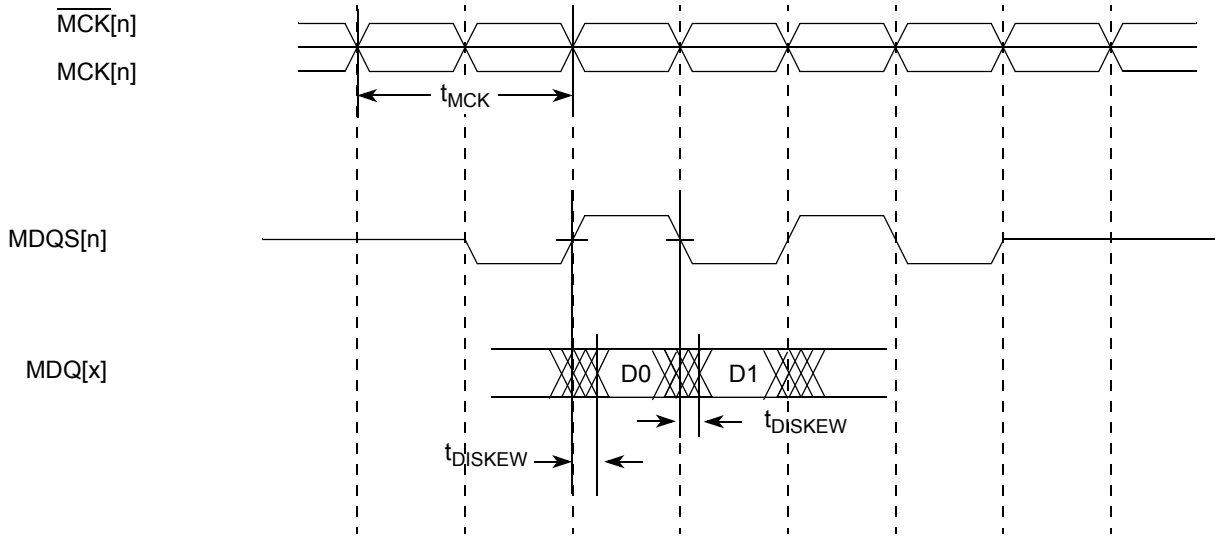


Figure 4. DDR Input Timing Diagram

6.2.2 DDR2 SDRAM Output AC Timing Specifications

The following table provides the output AC timing specifications for the DDR2 SDRAM interfaces.

Table 16. DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK cycle time, (MCK/$\overline{\text{MCK}}$ crossing)	t_{MCK}	5.988	8	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz	t_{DDKHAS}	 2.5	 —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz	t_{DDKHAX}	 2.5	 —	ns	3
$\overline{\text{MCS}}$ output setup with respect to MCK 266 MHz	t_{DDKHCS}	 2.5	 —	ns	3

Table 16. DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
$\overline{MCS}$ output hold with respect to MCK 266 MHz	t_{DDKHCX}	 2.5	 —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MDM output setup with respect to MDQS 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.9	 —	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100	 —	ps	5
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjusts in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. t_{DDKHMP} follows the symbol conventions described in note 1.

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

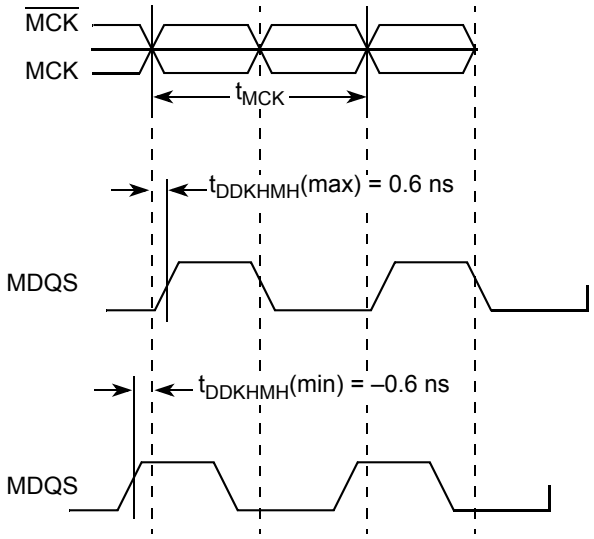


Figure 5. Timing Diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

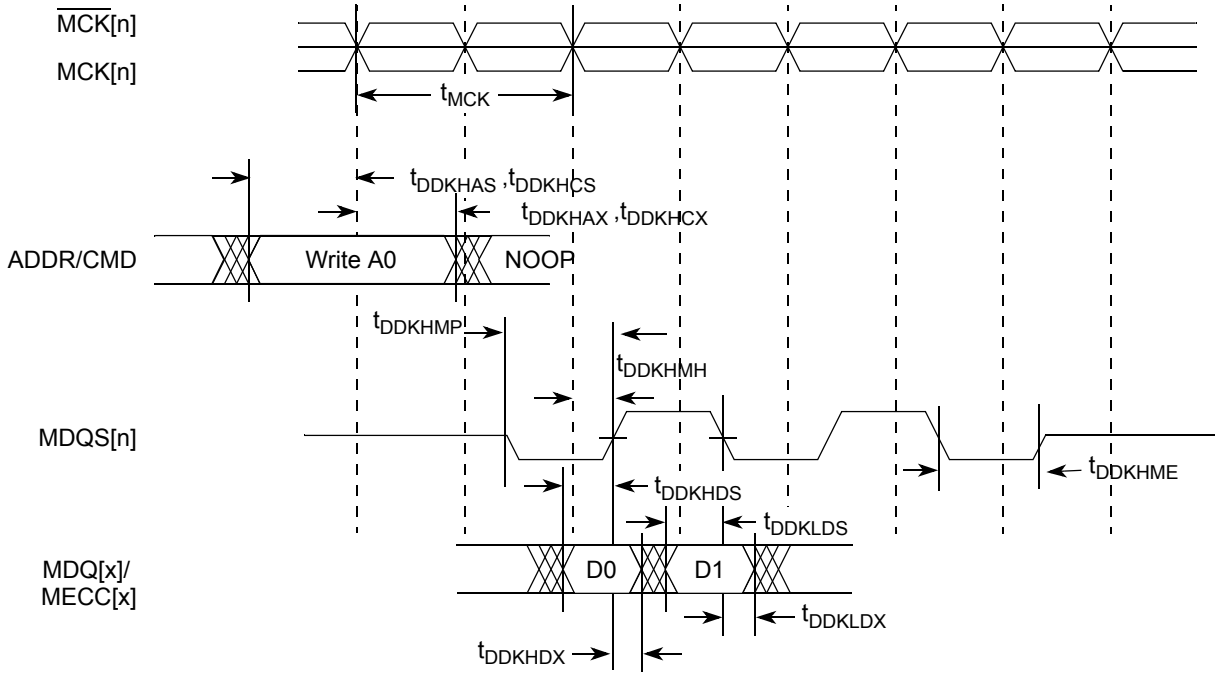


Figure 6. DDR2 SDRAM Output Timing Diagram

7 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8306S.

7.1 Local Bus DC Electrical Characteristics

The following table provides the DC electrical characteristics for the local bus interface.

Table 17. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	μA

7.2 Local Bus AC Electrical Specifications

The following table describes the general timing parameters of the local bus interface of the MPC8306S.

Table 18. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK*n*)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK*n*)	t_{LBIXKH}	1.0	—	ns	3, 4
Local bus clock (LCLK*n*) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK*n*) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

The following figure provides the AC test load for the local bus.

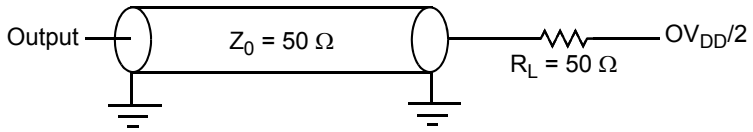


Figure 7. Local Bus AC Test Load

The following figures show the local bus signals. These figures has been given indicate timing parameters only and do not reflect actual functional operation of interface.

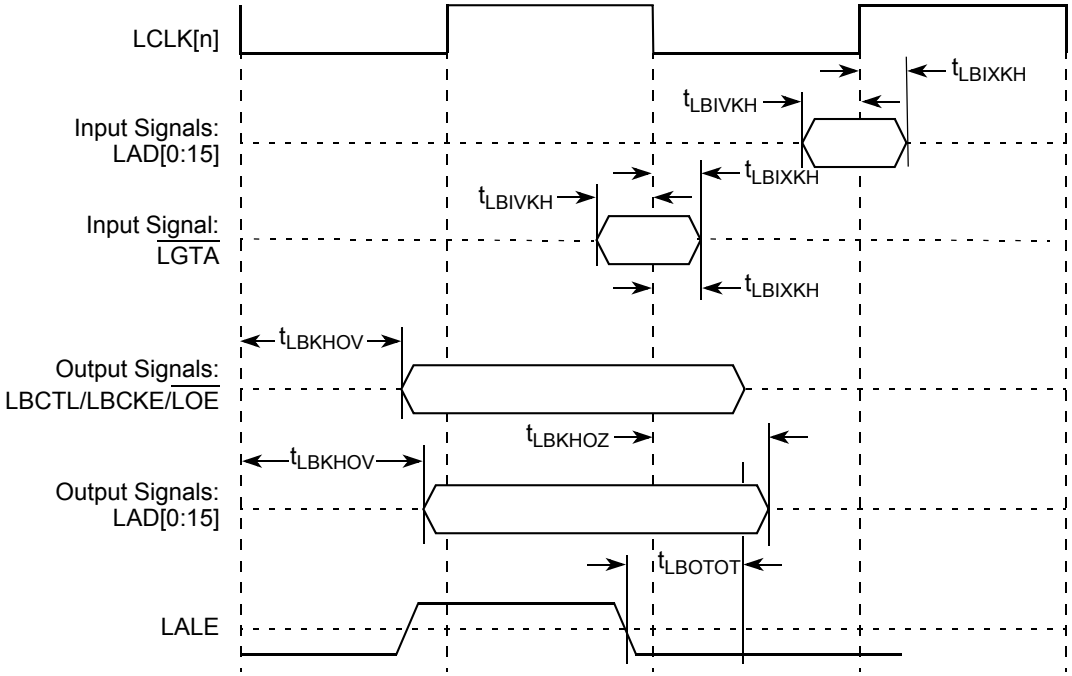


Figure 8. Local Bus Signals

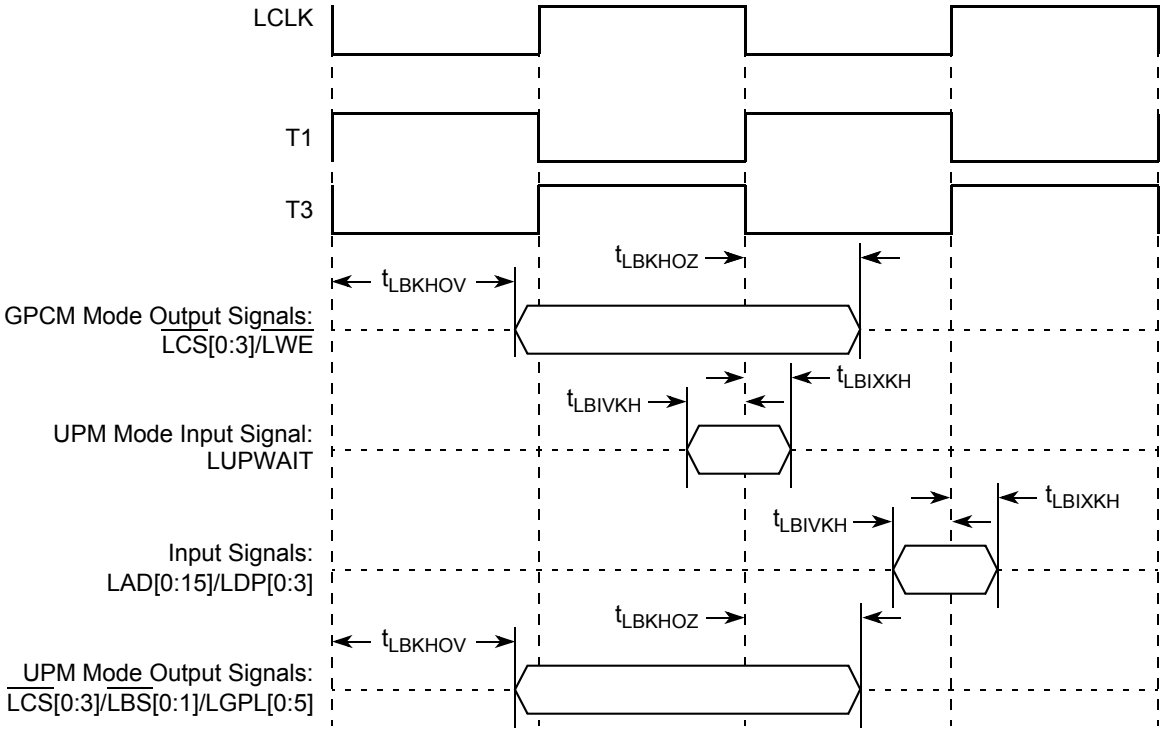


Figure 9. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

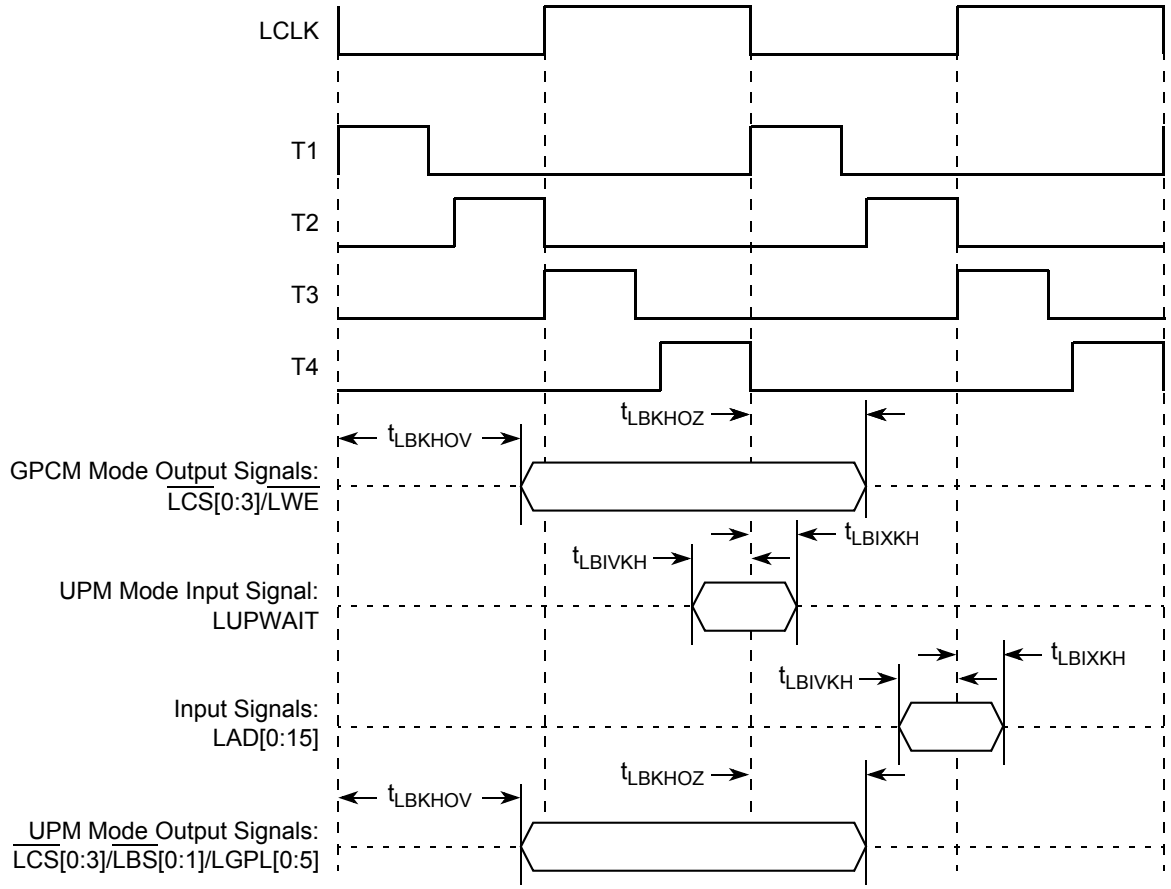


Figure 10. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

8 Ethernet and MII Management

This section provides the AC and DC electrical characteristics for Ethernet interfaces.

8.1 Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC (management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in The following table.

Table 19. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

The following table provides the MII transmit AC timing specifications.

Table 20. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

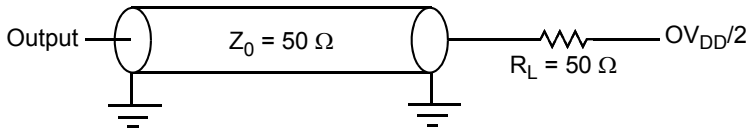


Figure 11. AC Test Load

The following figure shows the MII transmit AC timing diagram.

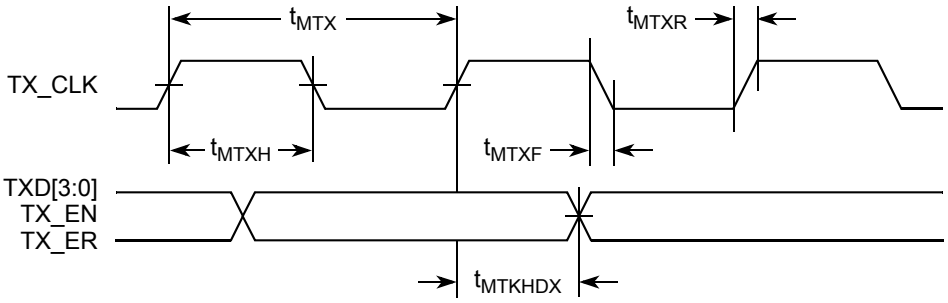


Figure 12. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

The following table provides the MII receive AC timing specifications.

Table 21. MII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII receive AC timing diagram.

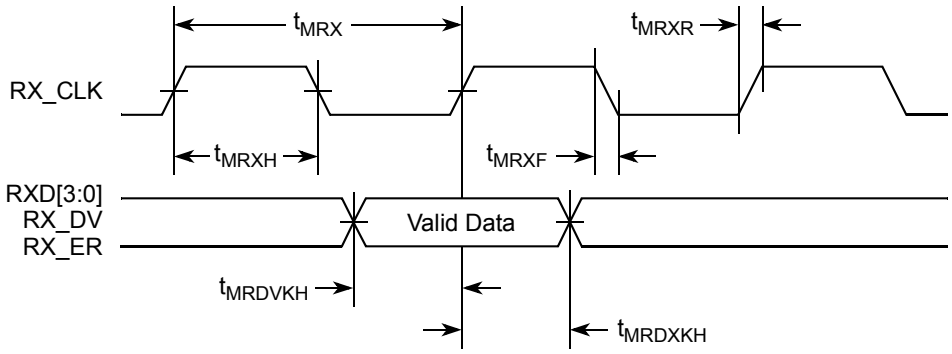


Figure 13. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII Transmit AC Timing Specifications

The following table provides the RMII transmit AC timing specifications.

Table 22. RMII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	13	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

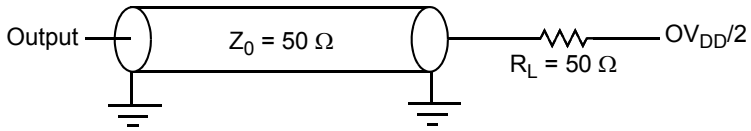


Figure 14. AC Test Load

The following figure shows the RMII transmit AC timing diagram.

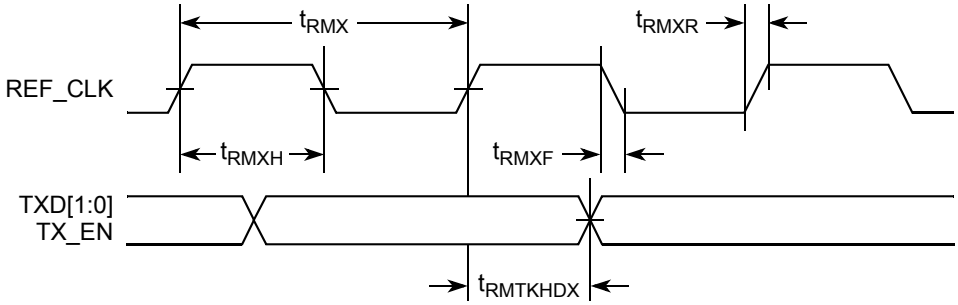


Figure 15. RMII Transmit AC Timing Diagram

8.2.2.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

Table 23. RMII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the RMII receive AC timing diagram.

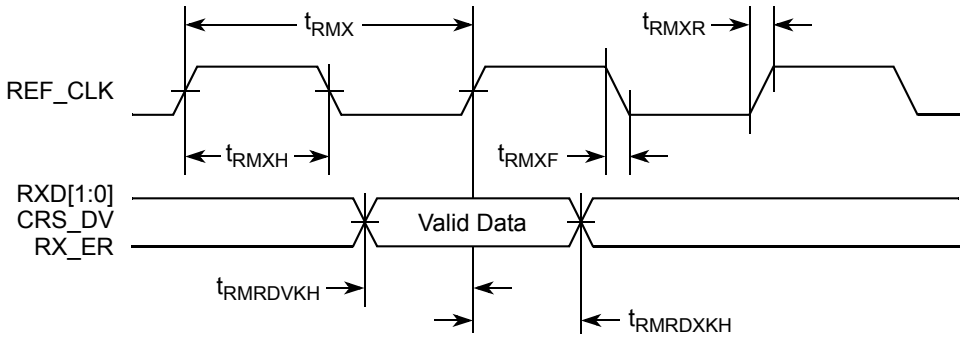


Figure 16. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in the following table.

Table 24. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII Management AC Electrical Specifications

The following table provides the MII management AC timing specifications.

Table 25. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—

Table 25. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	8.5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII management AC timing diagram.

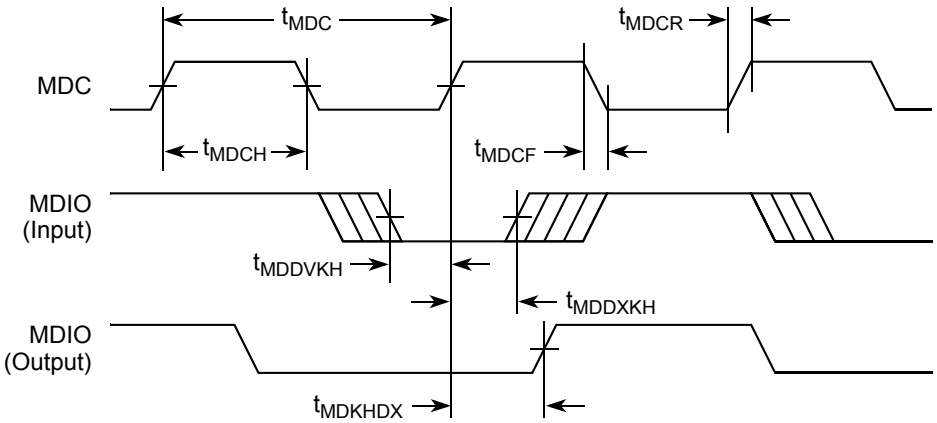


Figure 17. MII Management Interface Timing Diagram

9 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8306S.

9.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S TDM/SI.

Table 26. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

9.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

Table 27. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	14	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

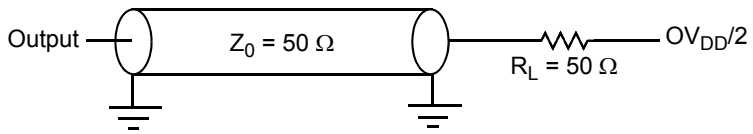
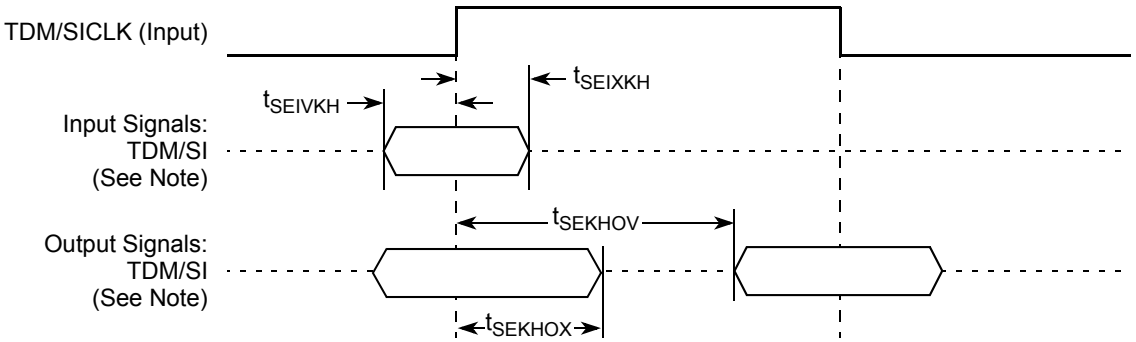


Figure 18. TDM/SI AC Test Load

The following figure represents the AC timing from Table 27. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 19. TDM/SI AC Timing (External Clock) Diagram

10 HDLC

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), of the MPC8306S.

10.1 HDLC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S HDLC protocol.

Table 28. HDLC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

10.2 HDLC AC Timing Specifications

The following table provides the input and output AC timing specifications for HDLC protocol.

Table 29. HDLC AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	9	ns
Outputs—External clock delay	t_{HEKHOV}	1	12	ns
Outputs—Internal clock high impedance	t_{HIKHOX}	0	5.5	ns

Table 29. HDLC AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	9	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load.

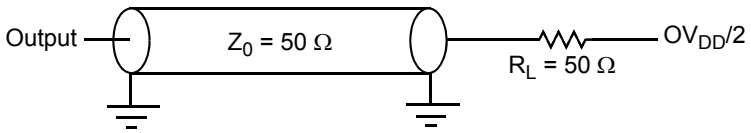
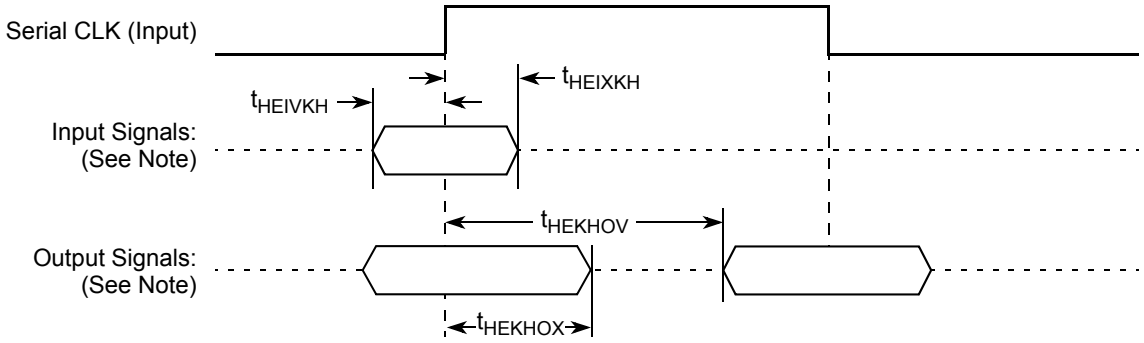


Figure 20. AC Test Load

Figure 21 and Figure 22 represent the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

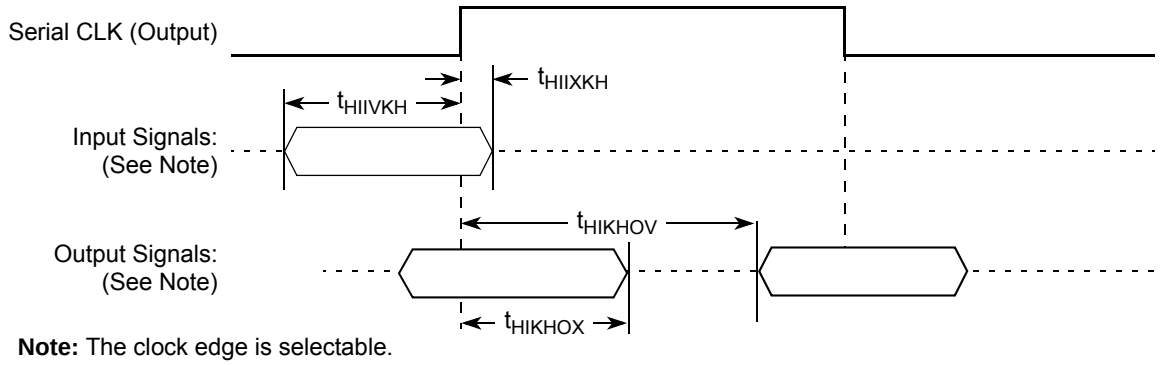
The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 21. AC Timing (External Clock) Diagram

The following figure shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 22. AC Timing (Internal Clock) Diagram

11 USB

11.1 USB Controller

This section provides the AC and DC electrical specifications for the USB (ULPI) interface.

11.1.1 USB DC Electrical Characteristics

The following table provides the DC electrical characteristics for the USB interface.

Table 30. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

11.1.2 USB AC Electrical Specifications

The following table describes the general timing parameters of the USB interface.

Table 31. USB General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	—
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	—
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	—
USB clock to output valid—all outputs (except USBDR_STP_USBDR_STP)	t_{USKHOV}	—	7	ns	—

Table 31. USB General Timing Parameters (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock to output valid—USBDR_STP	t_{USKHOV}	—	7.5	ns	—
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	—

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

The following figures provide the AC test load and signals for the USB, respectively.

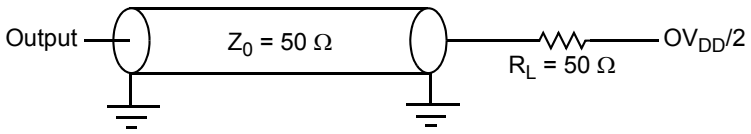


Figure 23. USB AC Test Load

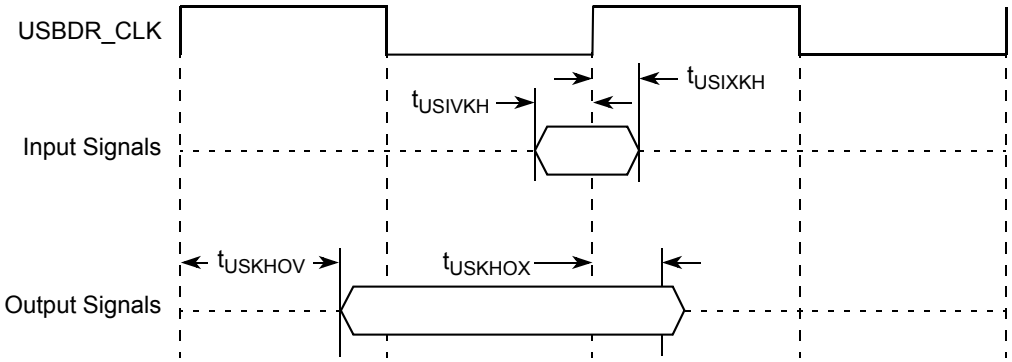


Figure 24. USB Signals

12 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8306S.

12.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface of the MPC8306S.

Table 32. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

12.2 DUART AC Electrical Specifications

The following table provides the AC timing parameters for the DUART interface of the MPC8306S.

Table 33. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

13 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface of the MPC8306S.

13.1 I^2C DC Electrical Characteristics

The following table provides the DC electrical characteristics for the I^2C interface of the MPC8306S.

Table 34. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

13.2 I^2C AC Electrical Specifications

The following table provides the AC timing parameters for the I^2C interface of the MPC8306S.

Table 35. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 34).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I^2C bus devices	t_{I2DXKL}	300	0.9[3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_B$[4]	300	ns

Table 35. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 34).

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_B[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8306S provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

The following figure provides the AC test load for the I²C.

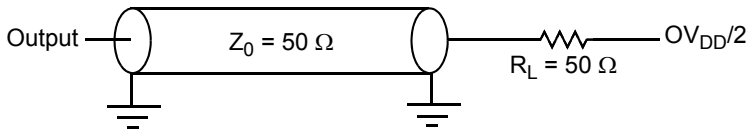


Figure 25. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

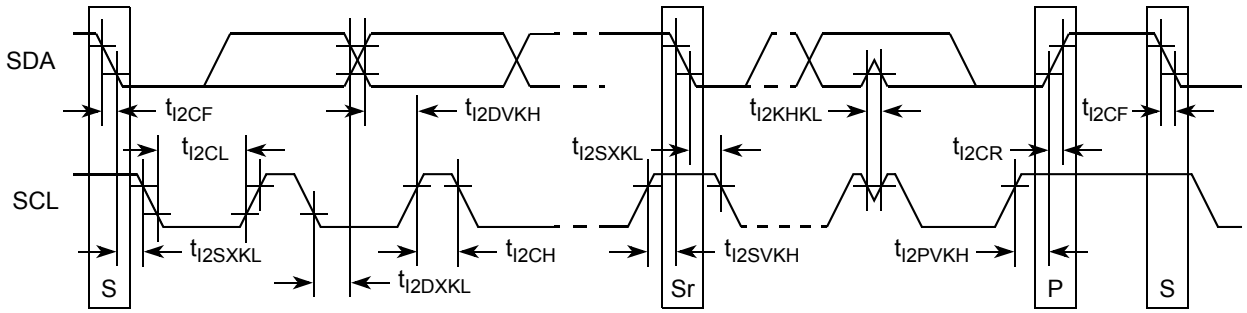


Figure 26. I²C Bus AC Timing Diagram

14 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8306S.

14.1 Timer DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_PIT_CLK.

Table 36. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

14.2 Timer AC Timing Specifications

The following table provides the timer input and output AC timing specifications.

Table 37. Timer Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

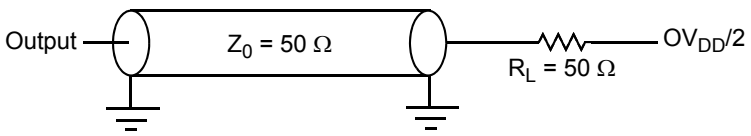


Figure 27. Timers AC Test Load

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8306S.

15.1 GPIO DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S GPIO.

Table 38. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

15.2 GPIO AC Timing Specifications

The following table provides the GPIO input and output AC timing specifications.

Table 39. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

The following figure provides the AC test load for the GPIO.

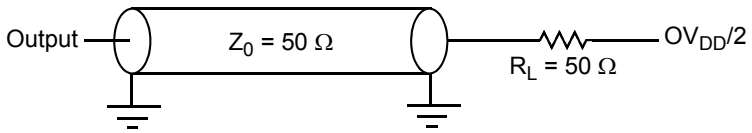


Figure 28. GPIO AC Test Load

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8306S.

16.1 IPIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins of the MPC8306S.

Table 40. IPIC DC Electrical Characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output High Voltage	V_{OH}	I_{OL} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$, $\overline{\text{MCP\_OUT}}$, and QE ports Interrupts.
2. $\overline{\text{MCP\_OUT}}$ is open drain pins, thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

The following table provides the IPIC input and output AC timing specifications.

Table 41. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

17 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8306S.

17.1 SPI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S SPI.

Table 42. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

17.2 SPI AC Timing Specifications

The following table and provide the SPI input and output AC timing specifications.

Table 43. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. All units of output delay must be enabled for 8306S output port spimosi (SPI Master Mode)
4. delay units must not be enabled for Slave Mode.

The following figure provides the AC test load for the SPI.

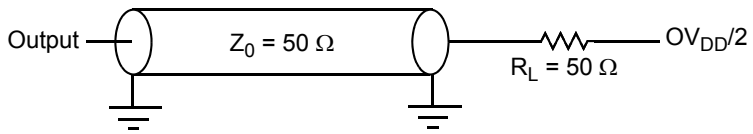
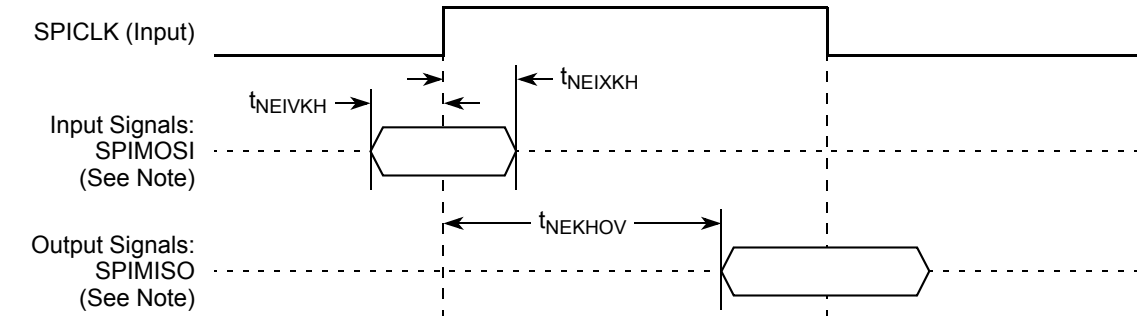


Figure 29. SPI AC Test Load

Figure 30 and Figure 31 represent the AC timing from Table 43. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

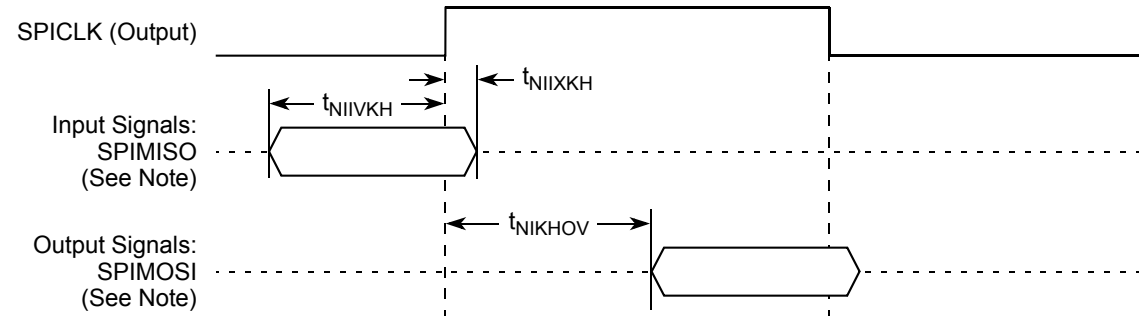
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 30. SPI AC Timing in Slave Mode (External Clock) Diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 31. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8306S.

18.1 JTAG DC Electrical Characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8306S.

Table 44. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Table 44. JTAG Interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

18.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8306S. The following table provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

Table 45. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 15 15	ns	5

Table 45. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	 5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	 5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

The following figure provides the AC test load for TDO and the boundary-scan outputs of the MPC8306S.

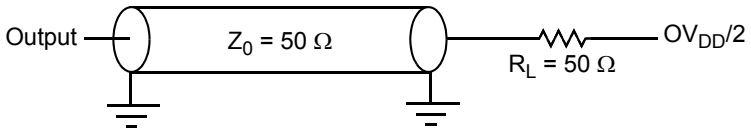


Figure 32. AC Test Load for the JTAG Interface

The following figure provides the JTAG clock input timing diagram.

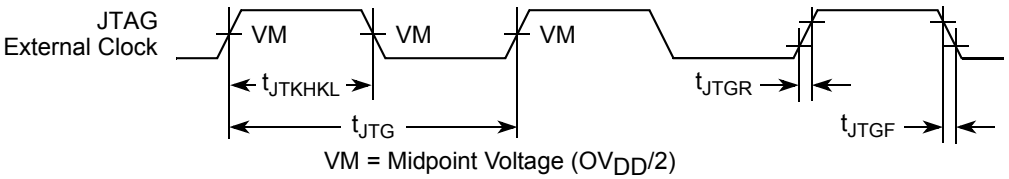


Figure 33. JTAG Clock Input Timing Diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

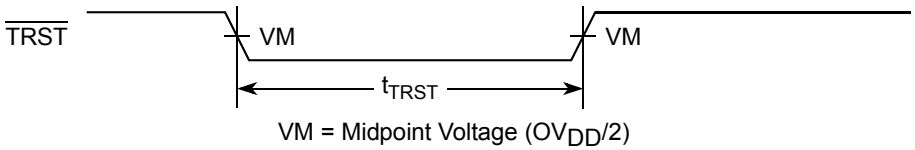


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

The following figure provides the boundary-scan timing diagram.

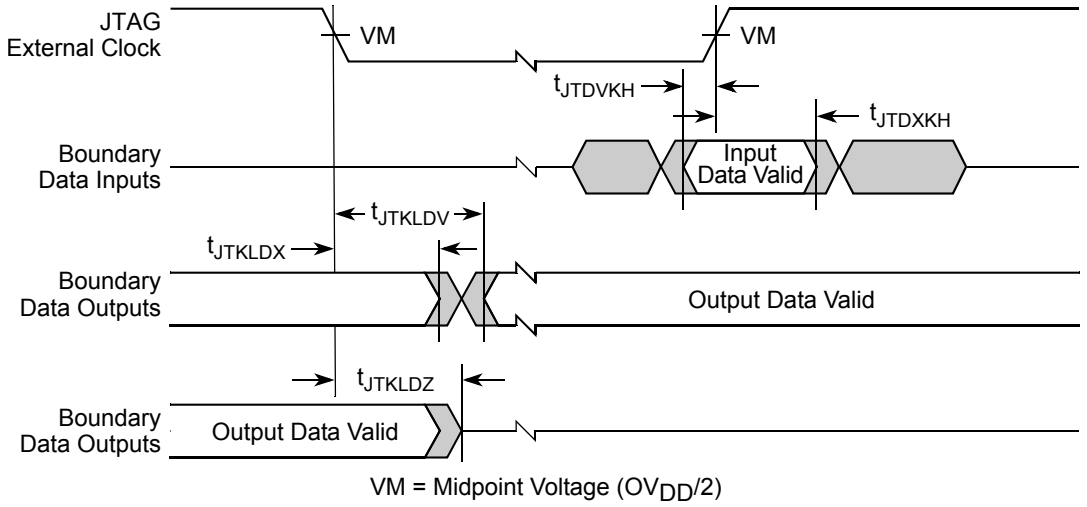


Figure 35. Boundary-Scan Timing Diagram

The following figure provides the test access port timing diagram.

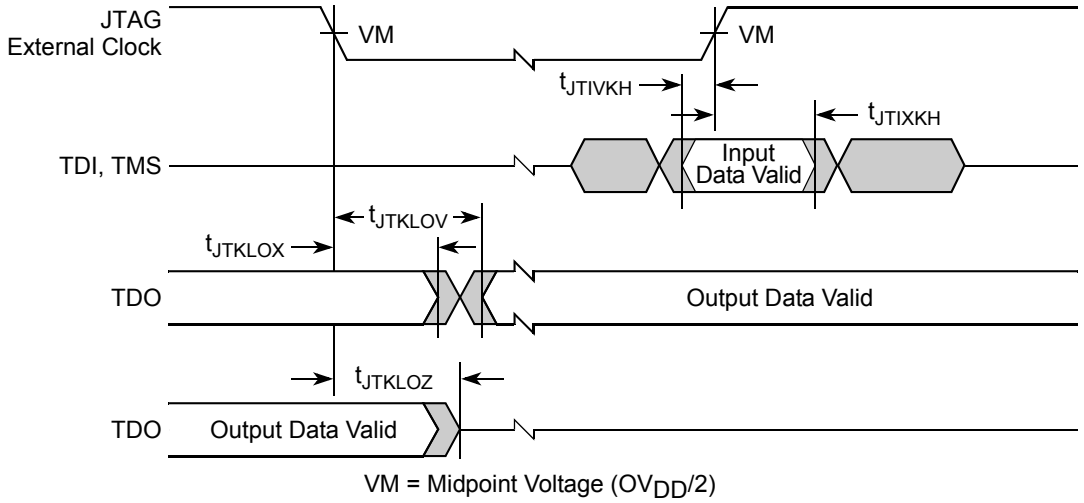


Figure 36. Test Access Port Timing Diagram

19 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8306S is available in a thermally enhanced MAPBGA (mold array process-ball grid array); see Section 19.1, “Package Parameters for the MPC8306S,” and Section 19.2, “Mechanical Dimensions of the MPC8306S MAPBGA,” for information on the MAPBGA.

19.1 Package Parameters for the MPC8306S

The package parameters are as provided in the following list.

Package outline	19 mm × 19 mm
Package Type	MAPBGA
Interconnects	369
Pitch	0.80 mm
Module height (typical)	1.48 mm; Min = 1.31mm and Max 1.61mm
Solder Balls	96 Sn / 3.5 Ag / 0.5 Cu (VM package)
Ball diameter (typical)	0.40 mm

19.2 Mechanical Dimensions of the MPC8306S MAPBGA

The following figure shows the mechanical dimensions and bottom surface nomenclature of the MPC8306S, 369-MAPBGA package.

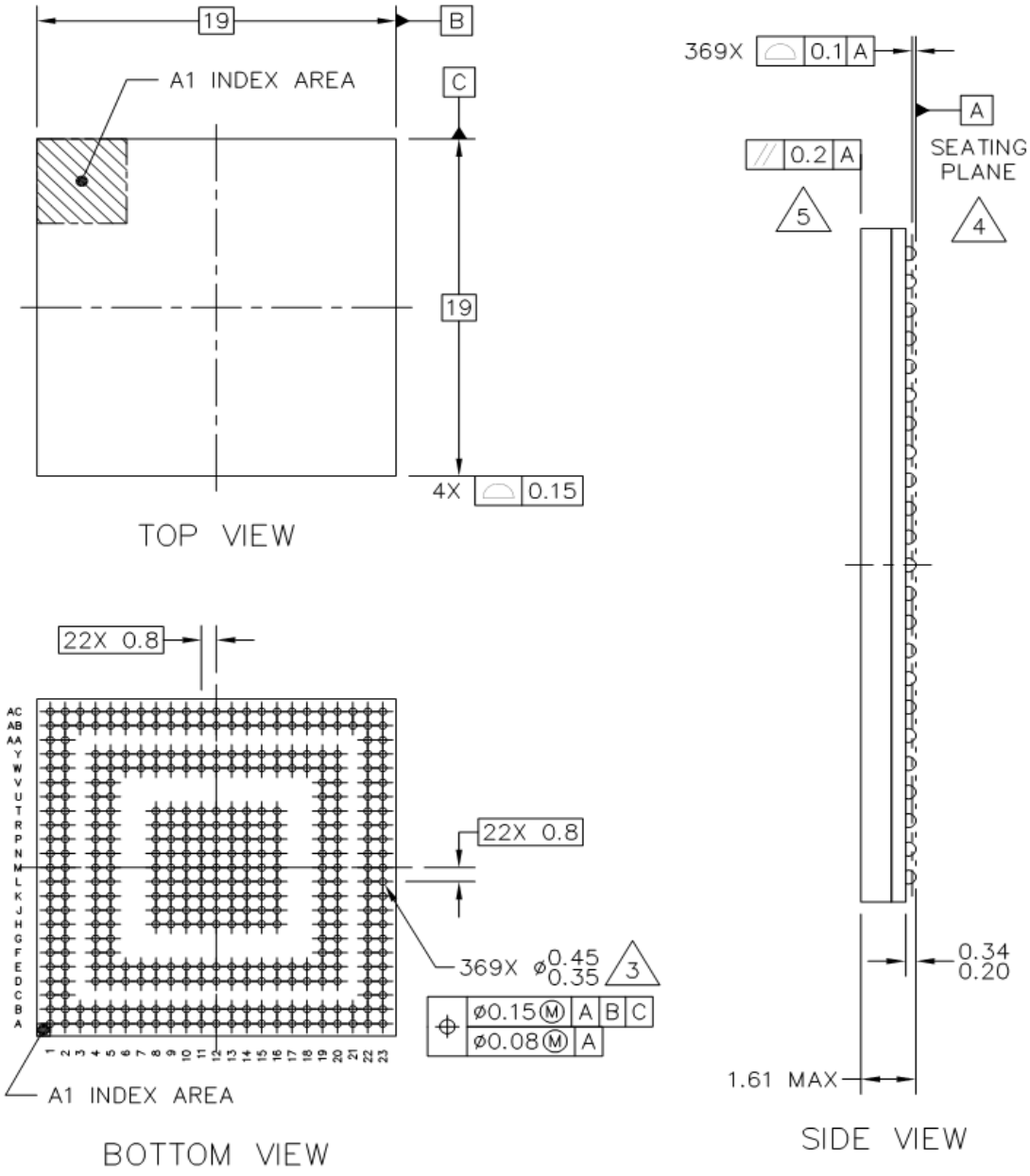


Figure 37. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8306S MAPBGA

Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

19.3 Pinout Listings

Following table shows the pin list of the MPC8306S.

Table 46. MPC8306S Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ[0]	W5	IO	GV_{DD}	—
MEMC_MDQ[1]	V4	IO	GV_{DD}	—
MEMC_MDQ[2]	Y4	IO	GV_{DD}	—
MEMC_MDQ[3]	AB1	IO	GV_{DD}	—
MEMC_MDQ[4]	AA1	IO	GV_{DD}	—
MEMC_MDQ[5]	Y2	IO	GV_{DD}	—
MEMC_MDQ[6]	Y1	IO	GV_{DD}	—
MEMC_MDQ[7]	W2	IO	GV_{DD}	—
MEMC_MDQ[8]	G2	IO	GV_{DD}	—
MEMC_MDQ[9]	G1	IO	GV_{DD}	—
MEMC_MDQ[10]	F1	IO	GV_{DD}	—
MEMC_MDQ[11]	E2	IO	GV_{DD}	—
MEMC_MDQ[12]	E1	IO	GV_{DD}	—
MEMC_MDQ[13]	E4	IO	GV_{DD}	—
MEMC_MDQ[14]	F4	IO	GV_{DD}	—
MEMC_MDQ[15]	D1	IO	GV_{DD}	—
MEMC_MDM[0]	AB2	O	GV_{DD}	—
MEMC_MDM[1]	G4	O	GV_{DD}	—
MEMC_MDQS[0]	V5	IO	GV_{DD}	—
MEMC_MDQS[1]	F5	IO	GV_{DD}	—
MEMC_MBA[0]	L2	O	GV_{DD}	—
MEMC_MBA[1]	L1	O	GV_{DD}	—
MEMC_MBA[2]	R4	O	GV_{DD}	—
MEMC_MA[0]	M1	O	GV_{DD}	—
MEMC_MA[1]	M4	O	GV_{DD}	—
MEMC_MA[2]	N1	O	GV_{DD}	—
MEMC_MA[3]	N2	O	GV_{DD}	—
MEMC_MA[4]	P1	O	GV_{DD}	—
MEMC_MA[5]	N4	O	GV_{DD}	—
MEMC_MA[6]	P2	O	GV_{DD}	—
MEMC_MA[7]	R1	O	GV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MA[8]	T1	O	GV_{DD}	—
MEMC_MA[9]	P4	O	GV_{DD}	—
MEMC_MA[10]	L4	O	GV_{DD}	—
MEMC_MA[11]	T2	O	GV_{DD}	—
MEMC_MA[12]	U1	O	GV_{DD}	—
MEMC_MA[13]	U2	O	GV_{DD}	—
MEMC_MWE_B	K1	O	GV_{DD}	—
MEMC_MRAS_B	K2	O	GV_{DD}	—
MEMC_MCAS_B	J1	O	GV_{DD}	—
MEMC_MCS_B[0]	J4	O	GV_{DD}	—
MEMC_MCS_B[1]	H1	O	GV_{DD}	—
MEMC_MCKE[0]	U4	O	GV_{DD}	—
MEMC_MCK[0]	V1	O	GV_{DD}	—
MEMC_MCK_B[0]	W1	O	GV_{DD}	—
MEMC_MODT[0]	H2	O	GV_{DD}	—
MEMC_MODT[1]	H4	O	GV_{DD}	—
MEMC_MVREF	L8		GV_{DD}	—
Local Bus Controller Interface				
LAD[0]	B7	IO	OV_{DD}	—
LAD[1]	D9	IO	OV_{DD}	—
LAD[2]	A6	IO	OV_{DD}	—
LAD[3]	B8	IO	OV_{DD}	—
LAD[4]	A7	IO	OV_{DD}	—
LAD[5]	A8	IO	OV_{DD}	—
LAD[6]	A9	IO	OV_{DD}	—
LAD[7]	D10	IO	OV_{DD}	—
LAD[8]	B10	IO	OV_{DD}	—
LAD[9]	A10	IO	OV_{DD}	—
LAD[10]	B11	IO	OV_{DD}	—
LAD[11]	D12	IO	OV_{DD}	—
LAD[12]	D11	IO	OV_{DD}	—
LAD[13]	A11	IO	OV_{DD}	—
LAD[14]	A12	IO	OV_{DD}	—
LAD[15]	B13	IO	OV_{DD}	—
LA[16]	A13	IO	OV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[17]	B14	O	OV_{DD}	—
LA[18]	A14	O	OV_{DD}	—
LA[19]	A15	O	OV_{DD}	—
LA[20]	A16	O	OV_{DD}	—
LA[21]	B16	O	OV_{DD}	—
LA[22]	A17	O	OV_{DD}	—
LA[23]	B17	O	OV_{DD}	—
LA[24]	A18	O	OV_{DD}	—
LA[25]	B19	O	OV_{DD}	—
LCS_B[0]	A19	O	OV_{DD}	3
LCS_B[1]	B20	O	OV_{DD}	3
LCS_B[2]	A20	O	OV_{DD}	3
LCS_B[3]	A21	O	OV_{DD}	3
LCLK[0]	D13	O	OV_{DD}	—
LGPL[0]	B22	O	OV_{DD}	—
LGPL[1]	D16	O	OV_{DD}	—
LGPL[2]	D19	O	OV_{DD}	—
LGPL[3]	D17	O	OV_{DD}	—
LGPL[4]	E18	IO	OV_{DD}	—
LGPL[5]	E19	O	OV_{DD}	—
LWE_B[0]	D15	O	OV_{DD}	—
LWE_B[1]	D14	O	OV_{DD}	—
LBCTL	A22	O	OV_{DD}	—
LALE	B23	O	OV_{DD}	—
JTAG				
TCK	A3	I	OV_{DD}	—
TDI	B5	I	OV_{DD}	3
TDO	D7	O	OV_{DD}	—
TMS	A4	I	OV_{DD}	3
TRST_B	D8	I	OV_{DD}	3
Test Interface				
TEST_MODE	A5	I	OV_{DD}	—
System Control Signals				
HRESET_B	U20	IO	OV_{DD}	1
PORESET_B	V20	I	OV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Clock Interface				
QE_CLK_IN	P23	I	OV_{DD}	—
SYS_CLK_IN	R23	I	OV_{DD}	—
RTC_PIT_CLOCK	V23	I	OV_{DD}	—
Miscellaneous Signals				
QUIESCE_B	A2	O	OV_{DD}	—
THERM0	D6	I	OV_{DD}	—
GPIO				
GPIO[0]/MSRCID0 (DDR ID)	E5	IO	OV_{DD}	—
GPIO[1]/MSRCID1 (DDR ID)	E6	IO	OV_{DD}	—
GPIO[2]/MSRCID2 (DDR ID)	D4	IO	OV_{DD}	—
GPIO[3]/MSRCID3 (DDR ID)	C2	IO	OV_{DD}	—
GPIO[4]/MSRCID4 (DDR ID)	C1	IO	OV_{DD}	—
GPIO[5]/MDVAL (DDR ID)	B1	IO	OV_{DD}	—
GPIO[6]/QE_EXT_REQ_3	B3	IO	OV_{DD}	—
GPIO[7]/QE_EXT_REQ_1	B2	IO	OV_{DD}	—
USB				
USBDR_PWRFAULT/IIC_SDA2/CE_PIO_1	AC4	IO	OV_{DD}	2
USBDR_CLK/UART2_SIN[2]/UART2_CTS_B[1]	Y9	I	OV_{DD}	
USBDR_DIR/IIC_SCL2	AC3	IO	OV_{DD}	2
USBDR_NXT/UART2_SIN[1]/QE_EXT_REQ_4	AC2	IO	OV_{DD}	—
USBDR_PCTL[0]/UART2_SOUT[1]/ LB_POR_CFG_BOOT_ECC	AB3	IO	OV_{DD}	—
USBDR_PCTL[1]/UART2_SOUT[2]/ UART2_RTS_B1/LB_POR_BOOT_ERR	Y8	O	OV_{DD}	—
USBDR_STP/QE_EXT_REQ_2	W6	IO	OV_{DD}	—
USBDR_TXDRXD[0]/UART1_SOUT[1]/ GPIO[32]/QE_TRB_O	AB7	IO	OV_{DD}	—
USBDR_TXDRXD[1]/UART1_SIN[1]/GPIO[33]/ QE_TRB_I	AB8	IO	OV_{DD}	—
USBDR_TXDRXD[2]/UART1_SOUT[2]/ UART1_RTS_B1/QE_BRG[1]	AC6	IO	OV_{DD}	—
USBDR_TXDRXD[3]/UART1_SIN[2]/ UART1_CTS_B1/QE_BRG[2]	AC5	IO	OV_{DD}	—
USBDR_TXDRXD[4]/GPIO[34]/QE_BRG[3]	AB5	IO	OV_{DD}	—
USBDR_TXDRXD[5]/GPIO[35]/QE_BRG[4]	Y7	IO	OV_{DD}	—
USBDR_TXDRXD[6]/GPIO[36]/QE_BRG[9]	Y6	IO	OV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USBDR_TXDRXD[7]/GPIO[37]/QE_BRG[11]	Y5	IO	OV_{DD}	—
DUART				
UART1_SOUT[1]/LSRCID4/LCS_B[4]	C23	O	OV_{DD}	—
UART1_SIN[1]/LDVAL/LCS_B[5]	F19	IO	OV_{DD}	—
UART1_SOUT[2]/UART1_RTS_B1/LCS_B[6]	D23	O	OV_{DD}	—
UART1_SIN[2]/UART1_CTS_B[1]/LCS_B[7]	D22	IO	OV_{DD}	—
Interrupts				
IRQ_B0_MCP_IN_B/CE_PI_0	E20	IO	OV_{DD}	—
IRQ_B1/MCP_OUT_B	E23	IO	OV_{DD}	—
IRQ_B2/CKSTOP_OUT_B	E22	IO	OV_{DD}	—
IRQ_B3/CKSTOP_IN_B	F20	I	OV_{DD}	—
I2C / SPI				
IIC_SDA1	G20	IO	OV_{DD}	2
IIC_SCL1	J20	IO	OV_{DD}	2
LCLK1/IIC_SCL2/CKSTOP_IN_B	H20	IO	OV_{DD}	2
SPISEL_BOOT/IIC_SDA2/CKSTOP_OUT_B	F23	O	OV_{DD}	2
SPIMOSI/LSRCID[2]	G22	IO	OV_{DD}	—
SPIMISO/LSRCID[3]	K20	IO	OV_{DD}	—
SPICLK/LSRCID[0]	G23	IO	OV_{DD}	—
SPISEL/LSRCID[1]	H22	I	OV_{DD}	—
FEC Management				
FEC_MDC	H23	O	OV_{DD}	—
FEC_MDIO	L20	IO	OV_{DD}	—
FEC1/GTM/GPIO				
FEC1_COL/GTM1_TIN[1]/GPIO[16]	AB20	IO	OV_{DD}	—
FEC1_CRS/GTM1_TGATE1_B/GPIO[17]	AC21	IO	OV_{DD}	—
FEC1_RX_CLK/GPIO[18]	Y17	IO	OV_{DD}	—
FEC1_RX_DV/GTM1_TIN[2]/GPIO[19]	Y18	IO	OV_{DD}	—
FEC1_RX_ER/GTM1_TGATE[2]_B/GPIO[20]	AB19	IO	OV_{DD}	—
FEC1_RXD0/GPIO[21]	AC20	IO	OV_{DD}	—
FEC1_RXD1/GTM1_TIN[3]/GPIO[22]	AC19	IO	OV_{DD}	—
FEC1_RXD2/GTM1_TGATE[3]_B/GPIO[23]	AC18	IO	OV_{DD}	—
FEC1_RXD3/GPIO[24]	AB17	IO	OV_{DD}	—
FEC1_TX_CLK/GTM1_TIN4/GPIO[25]	Y15	IO	OV_{DD}	—
FEC1_TX_EN/GTM1_TGATE[4]_B/GPIO[26]	Y16	IO	OV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FEC1_TX_ER/GTM1_TOUT[4]_B/GPIO[27]	AC17	IO	OV_{DD}	—
FEC1_TXD0/GTM1_TOUT[1]_B/GPIO[28]	AB16	IO	OV_{DD}	—
FEC1_TXD1/GTM1_TOUT[2]_B/GPIO[29]	AC16	IO	OV_{DD}	—
FEC1_TXD2/GTM1_TOUT[3]_B/GPIO[30]	AC15	IO	OV_{DD}	—
FEC1_TXD3/GPIO[31]	AB14	IO	OV_{DD}	—
FEC2/GPIO				
FEC2_COL/GPIO[32]	AC14	IO	OV_{DD}	—
FEC2_CRS/GPIO[33]	AB13	IO	OV_{DD}	—
FEC2_RX_CLK/GPIO[34]	Y14	IO	OV_{DD}	—
FEC2_RX_DV/GPIO[35]	AC13	IO	OV_{DD}	—
FEC2_RX_ER/GPIO[36]	Y13	IO	OV_{DD}	—
FEC2_RXD0/GPIO[37]	AC12	IO	OV_{DD}	—
FEC2_RXD1/GPIO[38]	AB11	IO	OV_{DD}	—
FEC2_RXD2/GPIO[39]	AC11	IO	OV_{DD}	—
FEC2_RXD3/GPIO[40]	AB10	IO	OV_{DD}	—
FEC2_TX_CLK/GPIO[41]	Y12	IO	OV_{DD}	—
FEC2_TX_EN/GPIO[42]	AC10	IO	OV_{DD}	—
FEC2_TX_ER/GPIO[43]	AC9	IO	OV_{DD}	—
FEC2_TXD0/GPIO[44]	AC8	IO	OV_{DD}	—
FEC2_TXD1/GPIO[45]	Y11	IO	OV_{DD}	—
FEC2_TXD2/GPIO[46]	AC7	IO	OV_{DD}	—
FEC2_TXD3/GPIO[47]	Y10	IO	OV_{DD}	—
FEC3/GPIO				
FEC3_COL/GPIO[48]	J23	IO	OV_{DD}	—
FEC3_CRS/GPIO[49]	K23	IO	OV_{DD}	—
FEC3_RX_CLK/GPIO[50]	M20	IO	OV_{DD}	—
FEC3_RX_DV/FEC1_TMR_TX_ESFD/GPIO[51]	K22	IO	OV_{DD}	—
FEC3_RX_ER/FEC1_TMR_RX_ESFD/GPIO[52]	L22	IO	OV_{DD}	—
FEC3_RXD0/FEC2_TMR_TX_ESFD/GPIO[53]	L23	IO	OV_{DD}	—
FEC3_RXD1/FEC2_TMR_RX_ESFD/GPIO[54]	M23	IO	OV_{DD}	—
FEC3_RXD2/TSEC_TMR_TRIG1/GPIO[55]	N22	IO	OV_{DD}	—
FEC3_RXD3/TSEC_TMR_TRIG2/GPIO[56]	N23	IO	OV_{DD}	—
FEC3_TX_CLK/TSEC_TMR_CLK/GPIO[57]	N20	IO	OV_{DD}	—
FEC3_TX_EN/TSEC_TMR_GCLK/GPIO[58]	P20	IO	OV_{DD}	—
FEC3_TX_ER/TSEC_TMR_PP1/GPIO[59]	P22	IO	OV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FEC3_TXD0/TSEC_TMR_PP2/GPIO[60]	R20	IO	OV_{DD}	—
FEC3_TXD1/TSEC_TMR_PP3/GPIO[61]	T22	IO	OV_{DD}	—
FEC3_TXD2/TSEC_TMR_ALARM1/GPIO[62]	T23	IO	OV_{DD}	—
FEC3_TXD3/TSEC_TMR_ALARM2/GPIO[63]	T20	IO	OV_{DD}	—
HDLC/GPIO/TDM				
HDLC1_RXCLK/TDM1_RCK/GPIO[1]	U23	IO	OV_{DD}	—
HDLC1_RXD/TDM1_RD/GPIO[3]	U22	IO	OV_{DD}	—
HDLC1_TXCLK/GPIO[0]/TDM1_TCK/ QE_BRG[5]	AC22	IO	OV_{DD}	—
HDLC1_TXD/GPIO[2]/TDM1_TD/ CFG_RESET_SOURCE[0]	W18	IO	OV_{DD}	—
HDLC1_CD_B/GPIO[4]/TDM1_TFS	W19	IO	OV_{DD}	—
HDLC1_CTS_B/GPIO[5]/TDM1_RFS	Y20	IO	OV_{DD}	—
HDLC1_RTS_B/GPIO[6]/TDM1_STROBE_B/ CFG_RESET_SOURCE[1]	AB22	IO	OV_{DD}	—
HDLC2_TXCLK/GPIO[16]/TDM2_TCK/ QE_BRG[7]	AB23	IO	OV_{DD}	—
HDLC2_RXCLK/GPIO[17]/TDM2_RCK/ QE_BRG[8]	AA23	IO	OV_{DD}	—
HDLC2_TXD/GPIO[18]/TDM2_TD/ CFG_RESET_SOURCE[2]	W20	IO	OV_{DD}	—
HDLC2_RXD/GPIO[19]/TDM2_RD	Y23	IO	OV_{DD}	—
HDLC2_CD_B/GPIO[20]/TDM2_TFS	Y22	IO	OV_{DD}	—
HDLC2_CTS_B/GPIO[21]/TDM2_RFS	W23	IO	OV_{DD}	—
HDLC2_RTS_B/GPIO[22]/TDM2_STROBE_B/ CFG_RESET_SOURCE[3]	W22	IO	OV_{DD}	—
Power				
AV_{DD1}	L16	—	—	—
AV_{DD2}	M16	—	—	—
AV_{DD3}	N8	—	—	—
GV_{DD}	G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5	—	—	—
OV_{DD}	E7,E8,E9,E10,E11,E12, E13,E14, E15, E16,E17,G19,H19,J19,K 19,L19,M19, N19,P19,R19,T19,U19, W7,W8,W9, W10,W11, W12,W13, W14,W15, W16, W17	—	—	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	H8,H9,H10,H11,H12,H13,H14,H15,H16,J8,J16,K8,K16,M8,N16,P8,P16,R8,R16,T8,T9,T10,T11,T12,T13,T14,T15,T16	—	—	—
VSS	A1,B4,B6,B9,B12,B15,B18,B21,C22,D2,D5,D18,D20,F2,F22,J2,J9,J10,J11,J12,J13,J14,J15,J22,K4,K9,K10,K11,K12,K13,K14,K15,L9,L10,L11,L12,L13,L14,L15,M2,M9,M10,M11,M12,M13,M14,M15,M22,N9,N10,N11,N12,N13,N14,N15,P9,P10,P11,P12,P13,P14,P15,R2,R9,R10,R11,R12,R13,R14,R15,R22,T4,V2,V19,V22,W4,Y19,AA2,AA22,AB4,AB6,AB9,AB12,AB15,AB18,AB21,AC1,AC23	—	—	—
NC	A23	—	—	—

Notes
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2-10 kΩ) should be placed on this pin to OV_{DD}
3. This pin has weak pull-up that is always enabled.

20 Clocking

The following figure Figure 39 shows the internal distribution of clocks within the MPC8306S.

Figure 38. MPC8306S Clock Subsystem

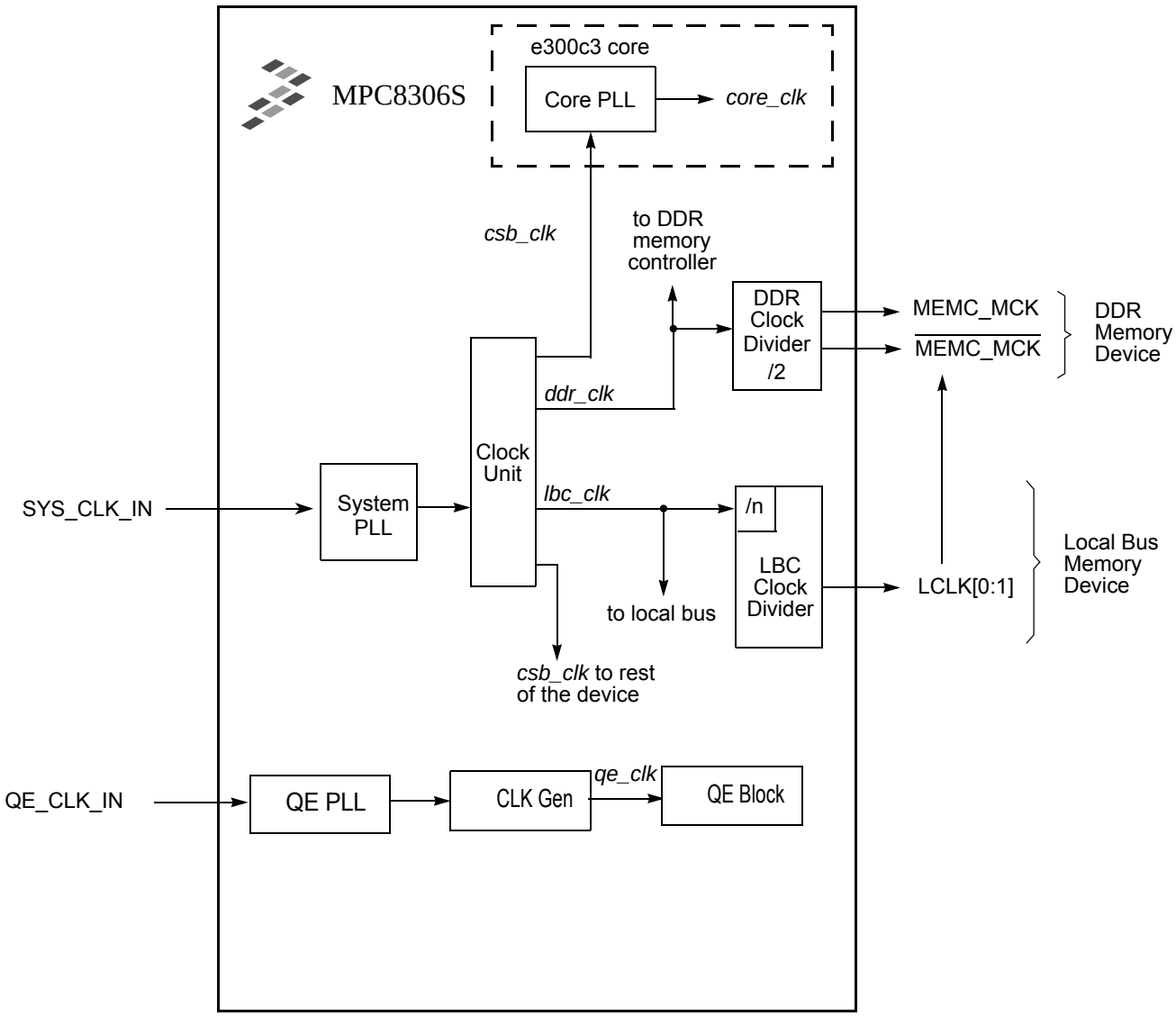


Figure 39. MPC8306S Clock Subsystem

The primary clock source for MPC8306S is SYS_CLK_IN.

Figure 40.

20.1 System Clock Domains

As shown in Figure 38, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create four major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*qe_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lbc_clk*)

The *csb_clk* frequency is derived from the following equation:

$$\textbf{\textit{csb\_clk}} = \text{SYS\_CLK\_IN} \times \text{SPMF} \qquad \textbf{\textit{Eqn. 1}}$$

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. For more information, see the Reset Configuration chapter in the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

The *qe_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF]) and the QUICC Engine PLL division factor (RCWL[CEPDF]) as the following equation:

$$\text{qe\_clk} = (\text{QE\_CLK\_IN} \times \text{CEPMF}) \div (1 + \text{CEPDF}) \qquad \textbf{Eqn. 2}$$

$$\textbf{\textit{qe\_clk = (QE\_CLK\_IN} \times \textit{CEPMF) } \div \textit{ (1 + CEPDF)}} \qquad \textbf{\textit{Eqn. 3}}$$

For more information, see the QUICC Engine PLL Multiplication Factor section and the “QUICC Engine PLL Division Factor” section in the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LCLK). The LBC clock divider ratio is controlled by LCRR[CLKDIV]. For more information, see the LBC Bus Clock and Clock Ratios section in the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset.

The following table specifies which units have a configurable clock frequency. For detailed description, refer to the “System Clock Control Register (SCCR)” section in the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

Table 47. Configurable Clock Units

Unit	Default Frequency	Options
I2C,SDHC, USB, DMA Complex	*csb_clk*	Off, csb_clk, *csb_clk*/2, *csb_clk*/3

NOTE

Setting the clock ratio of these units must be performed prior to any access to them.

The following table provides the maximum operating frequencies for the MPC8306S MAPBGA under recommended operating conditions (see Table 2).

Table 48. Operating Frequencies for MAPBGA

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	266	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
QUICC Engine frequency (*qe_clk*)	233	MHz
DDR2 memory bus frequency (MCLK)[2]	167	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting csb_clk, MCLK, LCLK, and core_clk frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR2 data rate is 2× the DDR2 memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the lb_clk frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the csb_clk frequency (depending on RCWL[LBCM]).

20.2 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 49 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider). The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

As described in Section 20, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (*SYS_CLK_IN)* and the internal

Table 49. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

coherent system bus clock (*csb_clk*). The following table shows the expected frequency values for the CSB frequency for selected *csb_clk* to *SYS_CLK_IN* ratios.

Table 50. CSB Frequency Options

SPMF	csb_clk : sys_clk_in Ratio	SYS_CLK_IN(MHz)		
		25	33.33	66.67
		csb_clk Frequency (MHz)		
0010	2:1			133
0011	3:1			
0100	4:1		133	
0101	5:1	125	167	
0110	6:1			

20.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

Table 51. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8

Table 51. e300 Core PLL Configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
00	0001	1	1.5:1	÷ 2
01	0001	1	1.5:1	÷ 4
10	0001	1	1.5:1	÷ 8
11	0001	1	1.5:1	÷ 8
00	0010	0	2:1	÷ 2
01	0010	0	2:1	÷ 4
10	0010	0	2:1	÷ 8
11	0010	0	2:1	÷ 8
00	0010	1	2.5:1	÷ 2
01	0010	1	2.5:1	÷ 4
10	0010	1	2.5:1	÷ 8
11	0010	1	2.5:1	÷ 8
00	0011	0	3:1	÷ 2
01	0011	0	3:1	÷ 4
10	0011	0	3:1	÷ 8
11	0011	0	3:1	÷ 8

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]), must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

20.4 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. The following table shows the multiplication factor encodings for the QUICC Engine PLL.

Table 52. QUICC Engine PLL Multiplication Factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6

Table 52. QUICC Engine PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in the following table.

Table 53. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	2
01	4
10	8
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

qe_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QUICC Engine VCO Frequency = *qe_clk* × VCO divider × (1 + CEPDF)

20.5 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8306S might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs is configured separately.

The following table shows suggested PLL configurations for 33 and 66 MHz input clocks.

Table 54. Suggested PLL Configurations

Conf No.	SPMF	Core PLL	CEPMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0111	0	33.33	133.33	266.66	233
2	0010	0000100	0111	1	66.67	133.33	266.66	233
3	0100	0000101	0111	0	33.33	133.33	333.33	233
4	0101	0000101	1001	0	25	125	312.5	225
5	0010	0000101	0111	1	66.67	133.33	333.33	233

21 Thermal

This section describes the thermal specifications of the MPC8306S.

21.1 Thermal Characteristics

The following table provides the package thermal characteristics for the 369, 19 × 19 mm MAPBGA of the MPC8306S.

Table 55. Package Thermal Characteristics for MAPBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	39	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	24	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	32	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	21	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	14	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.1.1 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.1.2 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 1}$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

21.1.3 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \qquad \text{Eqn. 2}$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

21.1.4 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \text{Eqn. 3}$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

21.1.5 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance as shown in the following equation:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

21.2 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint

lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

21.2.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface.

From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance using the following equation:

$$T_J = T_C + (R_{\theta JC} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_C = case temperature of the package (°C)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

22 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8306S.

22.1 System Clocking

The MPC8306S includes three PLLs.

- The system PLL (AV_{DD2}) generates the system clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the system and SYS_CLK_IN is selected using the system PLL ratio configuration bits as described in Section 20.2, “System PLL Configuration.”
- The e300 core PLL (AV_{DD3}) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 20.3, “Core PLL Configuration.”
- The QUICC Engine PLL (AV_{DD1}) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each $AV_{DD}n$ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 41, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

The following figure shows the PLL power supply filter circuit.

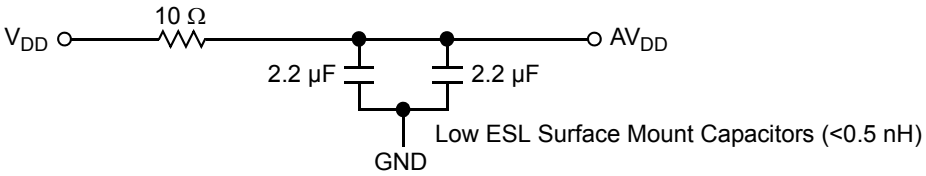


Figure 41. PLL Power Supply Filter Circuit

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8306S can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8306S system, and MPC8306S itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8306S. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias

to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

22.4 Output Buffer DC Impedance

For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 42). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

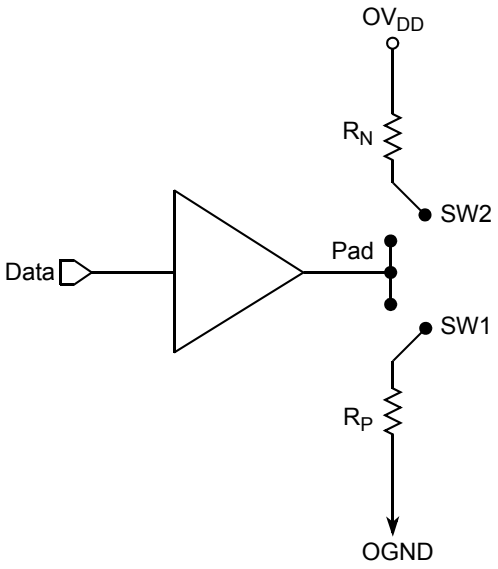


Figure 42. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

The following table summarizes the signal impedance targets. The driver impedance is targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 56. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration and Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	Ω
R_P	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

22.5 Configuration Pin Multiplexing

The MPC8306S provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (Refer to the “Reset, Clocking and Initialization” of *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

23 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 23.1, “Part Numbers Fully Addressed by This Document.”

23.1 Part Numbers Fully Addressed by This Document

The following table provides the Freescale part numbering nomenclature for the MPC8306S family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

Table 57. Part Numbering Nomenclature

MPC	*nnnn*	*C*	*VM*	*AF*	*D*	*C*	*A*
Product Code	**Part Identifier**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR2 Frequency**	**QUICC Engine Frequency**	**Revision Level**
MPC	8306S	Blank = 0 to 105°C C = –40 to 105°C	VM = Pb-free	AB = 133MHz AC = 200 MHz AD = 266 MHz AF = 333 MHz	D = 266 MHz F = 333 MHz	C = 233 MHz	Contact local Freescale sales office

Notes:
1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 19, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

23.2 Part Marking

Parts are marked as in the example shown in the following figure.

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 43. Freescale Part Marking for MAPBGA Devices

The following table shows the SVR Settings.

Table 58. SVR Settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)
MPC8306S	MAPBGA	0x8110_0210	0x8110_0211
Note: PVR = 0x8085_0020			

24 Document Revision History

The following table provides a revision history for this document.

Table 59. Document Revision History

Rev. No.	Date	Substantive Change(s)
1	09/2011	• Added Power numbers for core frequency of 333 MHz in Table 5. • Updated QUICC Engine frequency in Table 5. • Added SPISEL_BOOT in MPC8306 Pin out Listing Table 46. • Corrected SPISEL Pin Type in Table 46 • Updated QUICC Engine frequency from 200 MHz to 233 MHz in Table 48. • Added new PLL configurations as per new core frequency in Table 54. • Updated CEPMF and CEDF as per new QE frequency in Table 54. • Added AF to indicate 333 MHz in Table 57 • Updated QE Frequency to 233 MHz in Table 57.
0	03/2011	Initial Release

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MPC8306SEC
Rev. 1
09/2011

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

MPC8306CVMABDCA MPC8306CVMACDCA MPC8306CVMADDCA MPC8306SCVMABDCA MPC8306SCVMACDCA MPC8306SCVMADDCA MPC8306SVMABDCA MPC8306SVMACDCA MPC8306SVMADDCA MPC8306VMABDCA MPC8306VMACDCA MPC8306VMADDCA MPC8306SCVMAFDCA MPC8306VMAFDCA MPC8306CVMAFDCA MPC8306SVMAFDCA PPC8306SCVMADDCA