

CS2841B

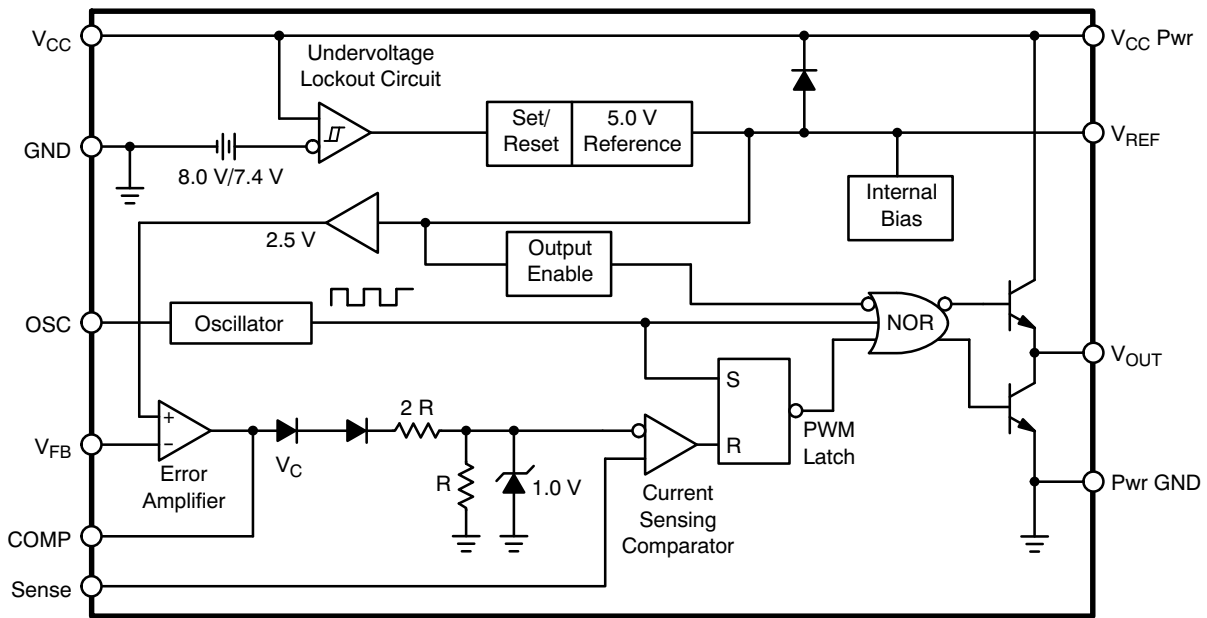


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Value	Unit	
Supply Voltage (Low Impedance Source)	40	V	
Output Current	±1.0	A	
Output Energy (Capacitive Load)	5.0	μJ	
Analog Inputs (V _{FB} , Sense)	-0.3 to 5.5	V	
Error Amp Output Sink Current	10	mA	
Lead Temperature Soldering	Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2	260 peak 230 peak	°C °C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 10 seconds max
2. 60 seconds max above 183°C

ORDERING INFORMATION

Device	Package	Shipping [†]
CS2841BEBN8	PDIP-8	50 Units / Rail
CS2841BEBN8G	PDIP-8 (Pb-Free)	50 Units / Rail
CS2841BED14	SOIC-14	55 Units / Rail
CS2841BED14G	SOIC-14 (Pb-Free)	55 Units / Rail
CS2841BEDR14	SOIC-14	2500 / Tape & Reel
CS2841BEDR14G	SOIC-14 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

CS2841B

ELECTRICAL CHARACTERISTICS ($-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $R_T = 680\text{ k}\Omega$, $C_T = 0.022\text{ }\mu\text{F}$ for Triangular Mode, $V_{CC} = 15\text{ V}$ (Note 3), $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$ for Sawtooth Mode (see Figure 7); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
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Reference Section

Output Voltage	$T_J = 25^{\circ}\text{C}$, $I_{OUT} = 1.0\text{ mA}$	4.9	5.0	5.1	V
Line Regulation	$8.4 \leq V_{CC} \leq 16\text{ V}$	-	6.0	20	mV
Load Regulation	$1.0 \leq I_{OUT} \leq 20\text{ mA}$	-	6.0	25	mV
Temperature Stability	Note 4	-	0.2	0.4	mV/ $^{\circ}\text{C}$
Total Output Variation	Line, Load, Temp. Note 4	4.82	-	5.18	V
Output Noise Voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$, $T_J = 25^{\circ}\text{C}$. Note 4	-	50	-	μV
Long Term Stability	$T_A = 125^{\circ}\text{C}$, 1000 Hrs. Note 4	-	5.0	25	mV
Output Short Circuit	$T_A = 25^{\circ}\text{C}$	-30	-100	-180	mA

Oscillator Section

Initial Accuracy	Sawtooth Mode: $T_J = 25^{\circ}\text{C}$. See Figure 7.	47	52	57	kHz
	Sawtooth Mode: $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	44	52	60	kHz
	Triangular Mode: $T_J = 25^{\circ}\text{C}$. See Figure 7.	44	52	60	kHz
Voltage Stability	$8.4 \leq V_{CC} \leq 16\text{ V}$	-	0.2	1.0	%
Temperature Stability	Sawtooth Mode: $T_{MIN} \leq T_A \leq T_{MAX}$. Note 4	-	5.0	-	%
	Triangular Mode: $T_{MIN} \leq T_A \leq T_{MAX}$. Note 4	-	8.0	-	%
Amplitude	V_{OSC} (Peak to Peak)	-	1.7	-	V
Discharge Current	$T_J = 25^{\circ}\text{C}$	7.4	8.3	9.2	mA
	$T_{MIN} \leq T_A \leq T_{MAX}$	7.2	-	9.4	mA

Error Amp Section

Input Voltage	$V_{COMP} = 2.5\text{ V}$	2.42	2.5	2.58	V
Input Bias Current	$V_{FB} = 0\text{ V}$	-	-0.3	-2.0	μA
A_{VOL}	$2.0 \leq V_{OUT} \leq 4.0\text{ V}$	65	90	-	dB
Unity Gain Bandwidth	Note 4	0.7	1.0	-	MHz
PSRR	$8.4\text{ V} \leq V_{CC} \leq 16\text{ V}$	60	70	-	dB
Output Sink Current	$V_{FB} = 2.7\text{ V}$, $V_{COMP} = 1.1\text{ V}$	2.0	6.0	-	mA
Output Source Current	$V_{FB} = 2.3\text{ V}$, $V_{COMP} = 5.0\text{ V}$	-0.5	-0.8	-	mA
V_{OUT} High	$V_{FB} = 2.3\text{ V}$, $R_L = 15\text{ k}\Omega$ to Ground	5.0	6.0	-	V
V_{OUT} Low	$V_{FB} = 2.7\text{ V}$, $R_L = 15\text{ k}\Omega$ to V_{REF}	-	0.7	1.1	V

Current Sense Section

Gain	Notes 5 and 6	2.85	3.0	3.15	V/V
Maximum Input Signal	$V_{COMP} = 5.0\text{ V}$. Note 5	0.9	1.0	1.1	V
PSRR	$12\text{ V} \leq V_{CC} \leq 25\text{ V}$. Note 5	-	70	-	dB
Input Bias Current	$V_{Sense} = 0\text{ V}$	-	-2.0	-10	μA
Delay to Output	$T_J = 25^{\circ}\text{C}$. Note 4	-	150	300	ns

- Adjust V_{CC} above the start threshold before setting at 15 V
- These parameters, although guaranteed, are not 100% tested in production
- Parameter measured at trip point of latch with $V_{FB} = 0$
- Gain defined as:

$$A = \frac{\Delta V_{COMP}}{\Delta V_{Sense}}; 0 \leq V_{Sense} \leq 0.8\text{ V}.$$

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Characteristic	Test Conditions	Min	Typ	Max	Unit
----------------	-----------------	-----	-----	-----	------

Output Section

Output Low Level	$I_{\text{SINK}} = 20\text{ mA}$	-	0.1	0.4	V
	$I_{\text{SINK}} = 200\text{ mA}$	-	1.5	2.2	V
Output High Level	$I_{\text{SOURCE}} = 20\text{ mA}$	13	13.5	-	V
	$I_{\text{SOURCE}} = 200\text{ mA}$	12	13.5	-	V
Rise Time	$T_J = 25^{\circ}\text{C}$, $C_L = 1.0\text{ nF}$. Note 7	-	50	150	ns
Fall Time	$T_J = 25^{\circ}\text{C}$, $C_L = 1.0\text{ nF}$. Note 7	-	50	150	ns
Output Leakage	Undervoltage Active, $V_{\text{OUT}} = 0$	-	-0.01	-10	μA

Total Standby Current

Startup Current	-	-	0.5	1.0	mA
Operating Supply Current I_{CC}	$V_{\text{FB}} = V_{\text{Sense}} = 0\text{ V}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$	-	11	17	mA

Undervoltage Lockout Section

Start Threshold	-	7.6	8.0	8.4	V
Min. Operating Voltage	After Turn On	7.0	7.4	7.8	V

7. These parameters, although guaranteed, are not 100% tested in production.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #		PIN SYMBOL	FUNCTION
PDIP-8	SOIC-14		
1	1	COMP	Error Amp Output, Used to Compensate Error Amplifier
2	3	V_{FB}	Error Amp Inverting Input
3	5	Sense	Noninverting Input to Current Sense Comparator
4	7	OSC	Oscillator Timing Network with Capacitor to Ground, Resistor to V_{REF}
5	8	GND	Ground
	9	Pwr GND	Output Driver Ground
6	10	V_{OUT}	Output Drive Pin
	11	V_{CC} Pwr	Output Driver Positive Supply
7	12	V_{CC}	Positive Power Supply
8	14	V_{REF}	Output of 5.0 V Internal Reference
	2, 4, 6, 13	NC	No Connection

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TYPICAL PERFORMANCE CHARACTERISTICS

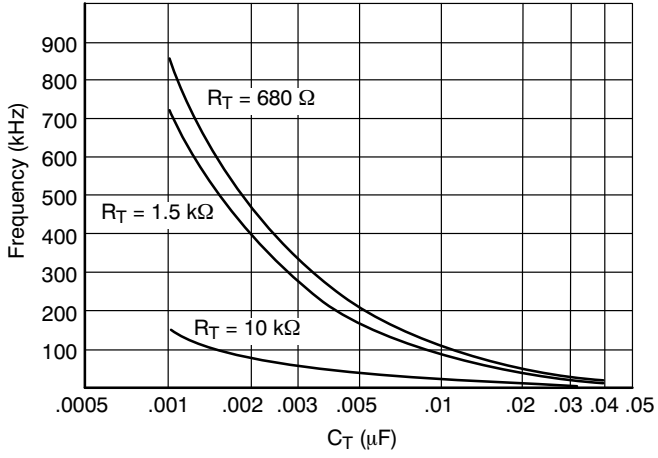


Figure 2. Oscillator Frequency vs. C_T

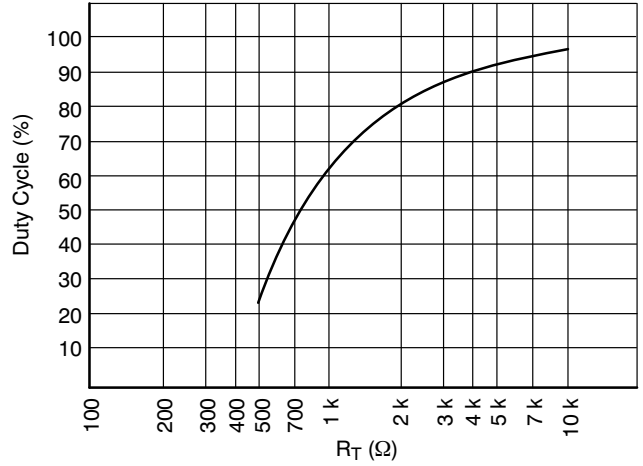


Figure 3. Oscillator Duty Cycle vs. R_T

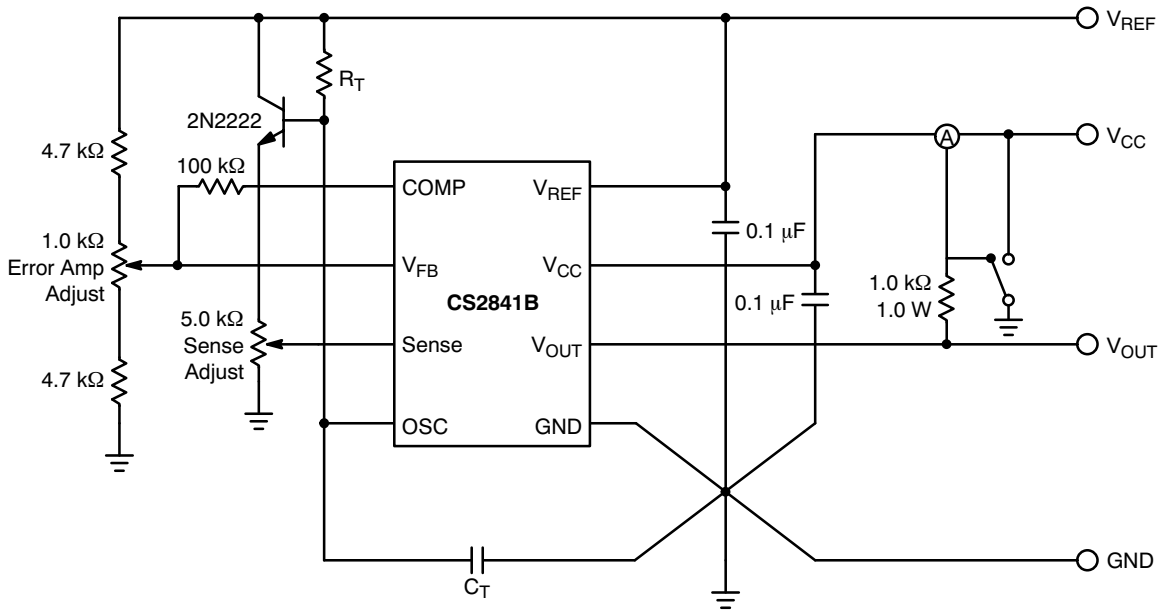


Figure 4. Test Circuit

CIRCUIT DESCRIPTION

Undervoltage Lockout

During Undervoltage Lockout (Figure 5), the output driver is biased to a high impedance state. The output should be shunted to ground with a resistor to prevent output leakage current from activating the power switch.

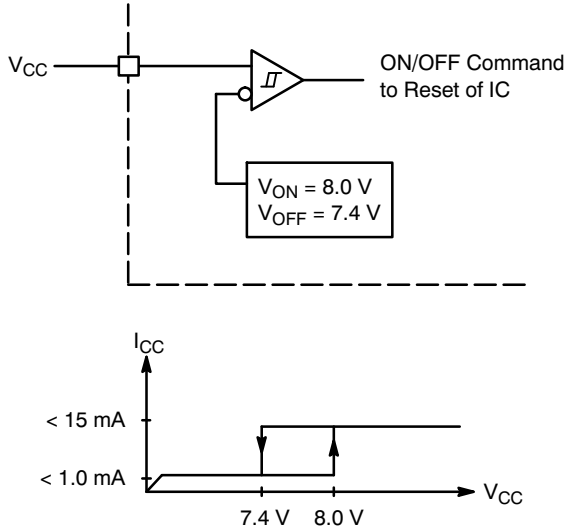


Figure 5. Typical Undervoltage Characteristics

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal representing the peak output inductor current (Figure 6). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

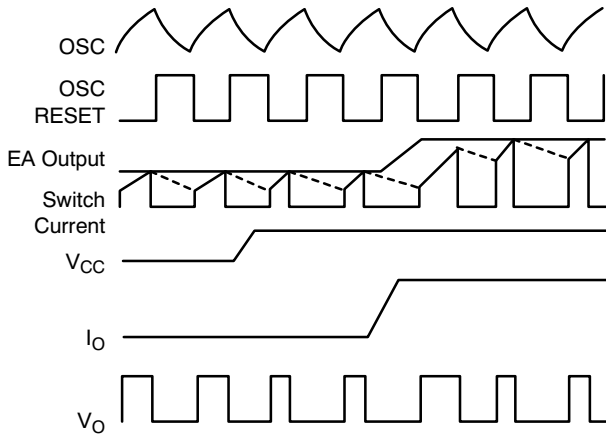
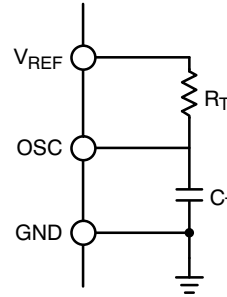
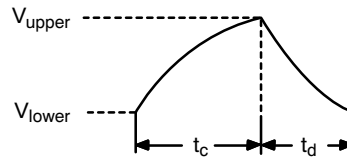


Figure 6. Timing Diagram for Key CS2841B Parameters

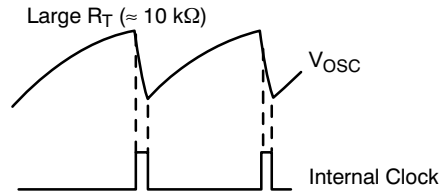
When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of OSC components.



Timing Parameters



Sawtooth Mode



Triangular Mode

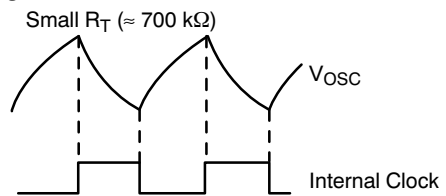


Figure 7. Oscillator Timing Network and Parameters

Setting the Oscillator

Oscillator timing capacitor, C_T , is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the Low state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the general formulas:

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$$t_c = R_T C_T \ln \left(\frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}} \right)$$

$$t_d = R_T C_T \ln \left(\frac{V_{REF} - I_d R_T - V_{upper}}{V_{REF} - I_d R_T - V_{lower}} \right)$$

Substituting in typical values for the parameters in the above formulas:

- $V_{REF} = 5.0 \text{ V}$
- $V_{upper} = 2.7 \text{ V}$
- $V_{lower} = 1.0 \text{ V}$
- $I_d = 8.3 \text{ mA}$
- $t_c \approx 0.5534 R_T C_T$

The frequency and maximum duty cycle can be determined from the Typical Performance Characteristic graphs.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to GND pin in a single point ground.

The transistor and 5.0 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

$$t_d = R_T C_T \ln \left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T} \right)$$

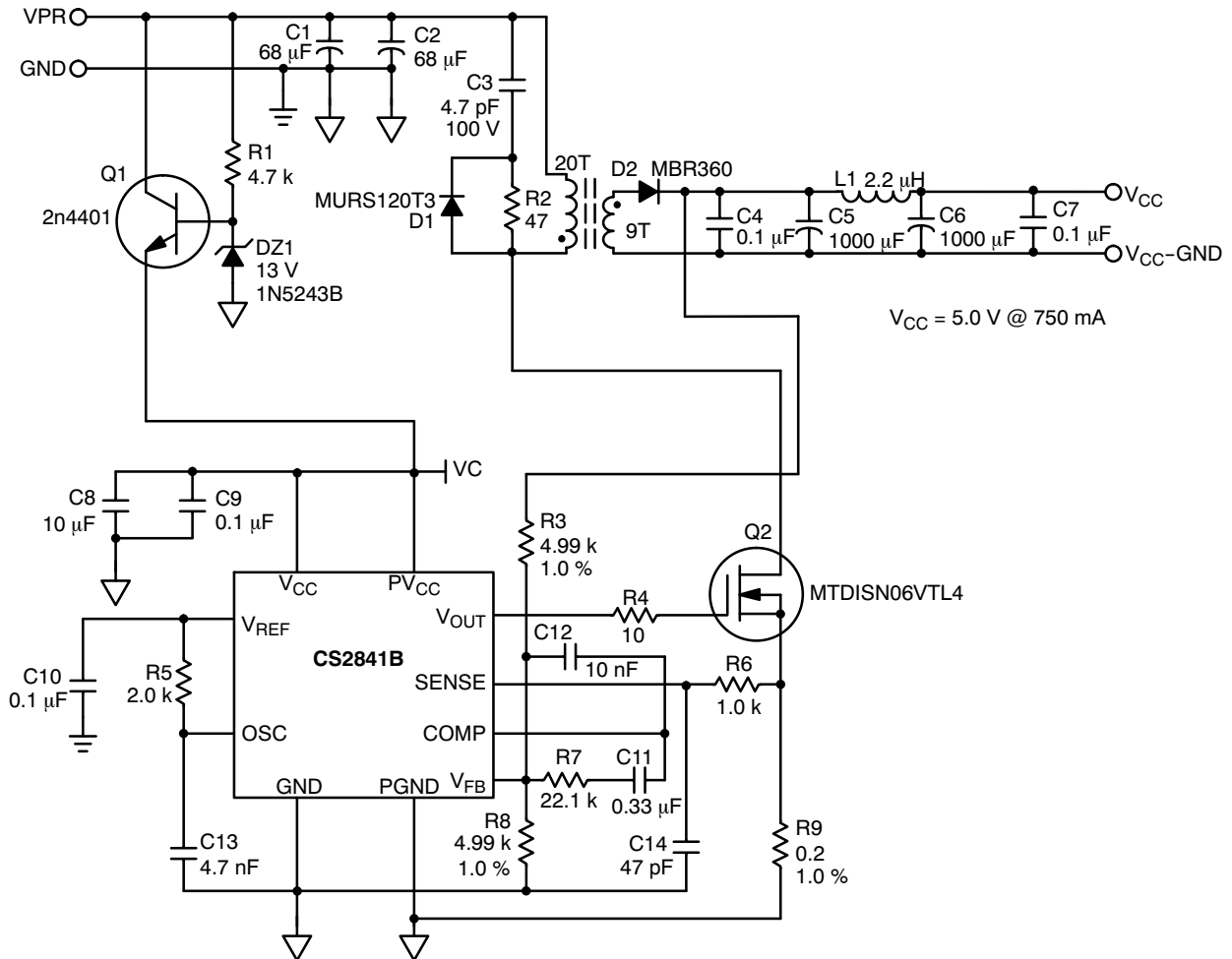


Figure 8. Flyback Application

CS2841B

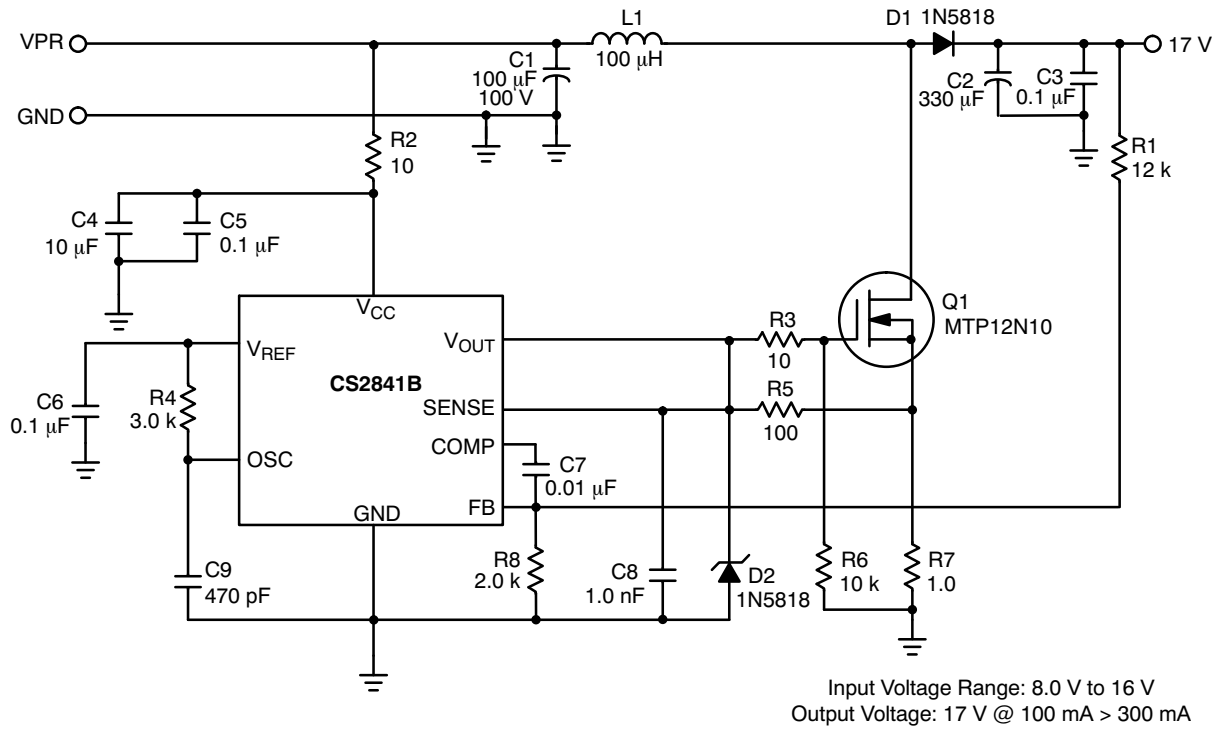


Figure 9. Boost Application

PACKAGE THERMAL DATA

Parameter		PDIP-8	SOIC-14	Unit
$R_{\theta JC}$	Typical	52	30	°C/W
$R_{\theta JA}$	Typical	100	125	°C/W

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC
MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

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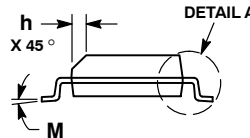
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SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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