Key Advantages (Continued)

- x4, x8, or x16, depending on Port configuration; x4 can down-train to x1 and x2 width
- Configurable through serial EEPROM, I2C, SMBus, and/or Host port

• Standards Compliant
- PCI Express Base Specification, r3.1 (backward compatible w/ PCIe r2.0, & r1.0a/1.1)
- PCI Power Management Spec, r1.2

• High Performance
- Full line rate on all ports

• Cut-Thru packet latency of less than 150ns (x16 to x16)
- 2KB Max Payload Size
- Multicast through DMA

• Quality of Service (QoS)
- 8 Traffic Classes (TC) supported

• Reliability, Availability, Serviceability
- visionPAK
- performance PAK
- DPC/eDPC Support
- Read Tracking for surprise removal
- All ports Hot-Plug capable thru I2C –SSC isolation on all ports
- SRIS support
- ECRC and Poison bit support
- Port Status bits and GPIO available

Downstream Port Containment (DPC/eDPC)

Most servers have difficulty handling serious errors, especially when a PCIe end-point disappears from the system. DPC/eDPC allows a downstream link to be disabled after an uncorrectable error, making recovery possible in a controlled and robust manner.

Flexible Topologies

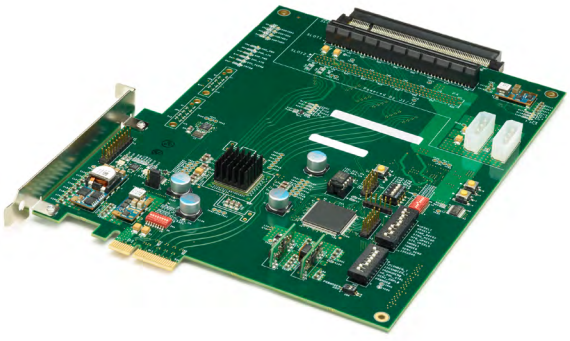
PEX9700 switches eliminate the topology restrictions of PCIe. The switch allows other topologies such as mesh, I/O Expansion Box with Multiple Hosts, and many others. And it does this while allowing the components to remain architecturally and software compatible with standard PCIe.

Improved SSC Isolation

The switches offer several mechanisms for supporting multi-clock domains that include spread spectrum clocking; eliminating the need to pass a common clock across a backplane. In addition to the standard Avago approach to the problem, a new PCI-SIG approach called SRIS (Separate Refclk Independent SSC Architecture) is now available.

Applications

Products based on ExpressFabric technology can help deliver an outstanding solution for designing a heterogeneous system with a requirement for a flexible mix of processors, storage elements, and communication devices.



HPC Clusters

HPC clusters are made up of high-performance processing elements that communicate through high bandwidth, low latency pathways in order to execute applications such as medical imaging, financial trading, data warehousing, etc. PEX9700 switches can be used in switch fabric applications for HPC clustering. The processing subsystems can be connected to the PCIe fabric while running the same application software. PCIe switch based clustering eliminates expensive protocol bridging devices resulting in lower cost and power. And clustering systems can be built with I/O sharing as an additional native capability when needed.

Software Development Kit (SDK)

The SDK for the PEX9700 series includes drivers, source code and GUI interfaces to aid in configuring and debugging. Both the performancePAK™ and visionPAK™ are exclusive to Avago and are supported by its RDK and SDK, which are the industry's most advanced hardware-and software development kits.

performancePAK

The performancePAK is a suite of unique and innovative performance features that allows Avago Gen 3 switches to be the highest performing switches in the market today.

visionPAK

The visionPAK is a debug diagnostics suite of integrated hardware and software instruments that allows users to help bring their systems to market faster.

PEX9700 Series

Part Number	Lanes	Ports	Latency (ns)	HPC*	Aggregate Bandwidth	SSC*	Dedicated x1 mCPU Port	DMA Multi-cast	Package Size (mm^2)	Typical Power Modes			
										Power Typ. (W)	Peer-to-Peer	Fanout	Fabric
PEX9797	97	25	150	6	1536GT (8.0 GT/s/Lane x 96 SerDes x2 (full-duplex))	24	Yes	Yes	35x35	23.9	24.3	20.6	25.0
PEX9781	81	21	150	5	1280GT (8.0 GT/s/Lane x 80 SerDes x2 (full-duplex))	20	Yes	Yes	35x35	21.5	22.5	19.6	23.3
PEX9765	65	17	150	4	1024GT (8.0 GT/s/Lane x 64 SerDes x2 (full-duplex))	16	Yes	Yes	35x35	15.9	16.2	13.9	16.9
PEX9749	49	13	150	4	768GT (8.0 GT/s/Lane x 48 SerDes x2 (full-duplex))	12	Yes	Yes	27x27	13.5	14.5	12.8	15.2
PEX9733	33	9	150	2	512GT (8.0 GT/s/Lane x 32 SerDes x2 (full-duplex))	8	Yes	Yes	27x27	7.9	8.1	7.2	8.9
PEX9716	16	5	154	1	256GT (8.0 GT/s/Lane x 16 SerDes x2 (full-duplex))	4	No	No	19x19	4.0	4.0	3.8	4.8
PEX9712	12	5	158	1	192GT (8.0 GT/s/Lane x 12 SerDes x2 (full-duplex))	4	No	No	19x19	3.5	3.7	3.4	4.4

Product Ordering Information

Switch Part Numbers	Description	Rapid Development Kit (RDK) Part Number
PEX9797-B080BC G	97-Lane, 25-Port ExpressFabric Device (35 × 35 mm^2)	PEX9797-B0RDK
PEX9781-B080BC G	81-Lane, 21-Port ExpressFabric Device (35 × 35 mm^2)	PEX9797-B0RDK
PEX9765-B080BC G	65-Lane, 17-Port ExpressFabric Device (35 × 35 mm^2)	PEX9797-B0RDK
PEX9749-B080BC G	49-Lane, 13-Port ExpressFabric Device (27 × 27 mm^2)	PEX9749-B0RDK
PEX9733-B080BC G	33-Lane, 9-Port ExpressFabric Device (27 × 27 mm^2)	PEX9749-B0RDK
PEX9716-B080BC G	16-Lane, 5-Port ExpressFabric Device (19 ×19 mm^2)	PEX9716-B0RDK
PEX9712-B080BC G	12-Lane, 5-Port ExpressFabric Device (19 × 19 mm^2)	PEX9716-B0RDK

Acronym Guide

HPC Hot-Plug Controllers
TWC Tunneled Window Connection
SSC Spread Spectrum Clock Isolation
MSI-X Message Signaled Interrupts
SRIS Separate Refclk Independent SSC Architecture
DPC Downstream Port Containment
eDPC Enhanced DPC
Commercial Temperature Range 0 to +70°C

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