+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

ABSOLUTE MAXIMUM RATINGS

V_{DD}, SCLK, DIN, $\overline{CS}$, $\overline{LDAC}$, OUT_ to GND .....-0.3V to 6V
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current (any pin) .....±50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
µMAX (derate 4.10mW/°C above +70°C) 330mW

Operating Temperature Ranges
MAX5_ _AC_ A.....0°C to +70°C
MAX5_ _AE_ A.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic	MAX5_ _AEUA (Note 1)			±0.9	LSB
			All others			±0.9	
Total Unadjusted Error	TUE		MAX5_ _AEUA (Note 1)			±1	LSB
			All others			±1	
Zero-Code Error	ZCE					±1	LSB
Full-Scale Error	FSE					±1	LSB
REFERENCE INPUT							
Reference Input Voltage Range	V_{REF}	MAX549A/MAX550A for specified performance		2.5		V_{DD}	V
Reference Input Resistance DAC Code = 55 Hex (Note 2)	R_{REF}	MAX549A			16.7		kΩ
		MAX550A			33.3		
Reference Input Current DAC Code = 55 Hex (Note 3)	I_{REF}	MAX549A	V_{DD} = V_{REF} = 5.5V		330	550	µA
			V_{DD} = V_{REF} = 2.5V		150	250	
		MAX550A	V_{DD} = V_{REF} = 5.5V		165	275	
			V_{DD} = V_{REF} = 2.5V		75	125	
DAC OUTPUT							
DAC Output Voltage Swing		MAX548A		0		V_{DD}	V
		MAX549A/MAX550A		0		V_{REF}	
DAC Output Resistance	R_{OUT}				33.3		kΩ
DAC Output Resistance Matching	$\Delta R_{OUT}/R_{OUT}$	MAX548A/MAX549A			±0.2		%
DIGITAL INPUTS							
Input High Voltage	V_{IH}			0.7V_{DD}			V
Input Low Voltage	V_{IL}					0.3V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance (Note 4)	C_{IN}					10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Digital Feedthrough and Crosstalk		$\overline{CS}$ = high, all digital inputs from 0V to V_{DD}			50		nV-sec
Voltage-Output Settling Time		To ±1/2LSB, C_L = 20pF			4		µs
Voltage-Output Slew Rate		C_L = 20pF	V_{DD} = 2.5V		1.4		V/µs
			V_{DD} = 5.5V		3.1		
Wake-Up Time at Power-Up		C_L = 20pF			4		µs
POWER SUPPLIES							
Supply Voltage Range	V_{DD}	Outputs unloaded, all inputs = GND or V_{DD}		2.5		5.5	V
Supply Current (MAX548A)	I_{DD}	Outputs unloaded, all inputs = GND or V_{DD} (Note 5)	V_{DD} = 5.5V		330	550	µA
			V_{DD} = 2.5V		150	250	
Supply Current (MAX549A/MAX550A)	I_{DD}	Outputs unloaded, all inputs = GND or V_{DD}; V_{DD} = 5.5V			0.3	10	µA
Shutdown Current		Shutdown mode			0.3		µA

TIMING CHARACTERISTICS

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Digital inputs switching from 0V to V_{DD}.) (Figure 3) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
DIN to SCLK High Setup	t_{DS}		30			ns
DIN to SCLK High Hold	t_{DH}	V_{DD} = 2.5V	0			ns
		V_{DD} = 5.5V	10			
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		30			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		30			ns
SCLK High to CS Low Hold	t_{CSH0}		10			ns
Delay, SCLK High to $\overline{CS}$ High	t_{CSH1}	V_{DD} = 2.5V	10			ns
		V_{DD} = 5.5V	20			
$\overline{CS}$ Pulse Width High	t_{CSW}		40			ns
SCLK Period	t_{CP}		80			ns
$\overline{LDAC}$ Pulse Width Low	$t_{\overline{LDAC}}$	MAX548A/MAX550A only	50			ns
CS High to $\overline{LDAC}$ Low	t_{CSLD}	MAX548A/MAX550A only	50			ns
V_{DD} High to $\overline{CS}$ Low			5			µs

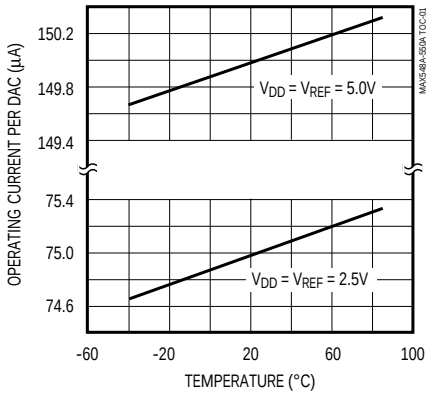
Note 1: Cold temperature specifications (to -40°C) guaranteed by design using six sigma design limits.
Note 2: Worst-case input resistance at REF occurs at DAC code 55 hex.
Note 3: Worst-case reference input current occurs at DAC code 55 hex.
Note 4: Guaranteed by design. Not production tested.
Note 5: I_{DD} measured with DACs loaded with worst-case DAC code 55 hex.

+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

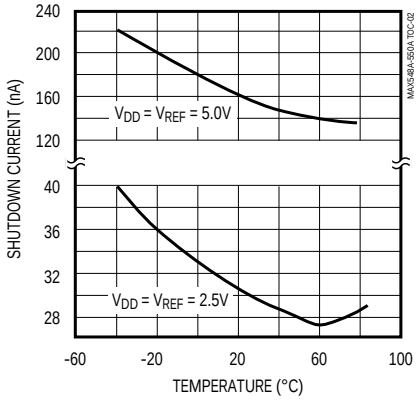
Typical Operating Characteristics

(V_{DD} = V_{REF} = 2.5V, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

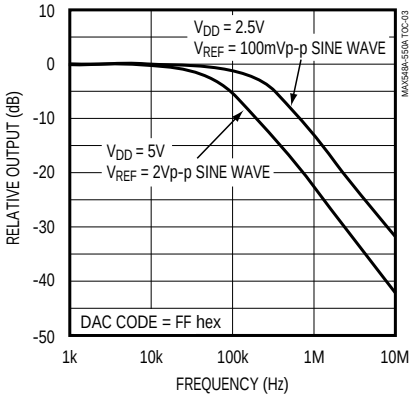
OPERATING CURRENT PER DAC vs. TEMPERATURE



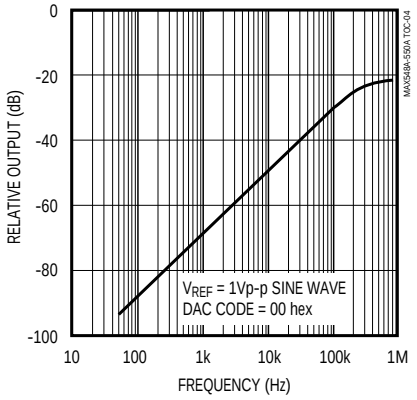
SHUTDOWN CURRENT vs. TEMPERATURE



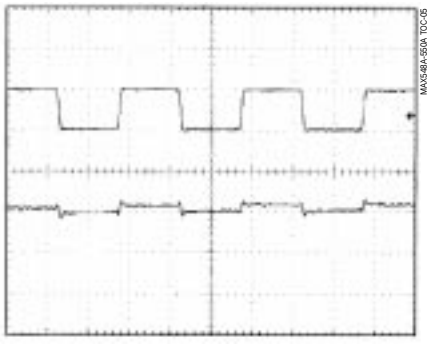
MAX549A/MAX550A REFERENCE SMALL-SIGNAL FREQUENCY RESPONSE



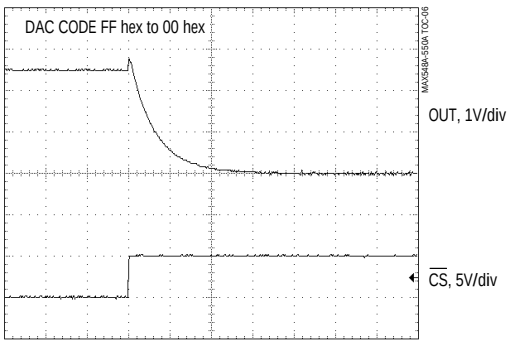
MAX549A/MAX550A REFERENCE AC FEEDTHROUGH vs. FREQUENCY



DIGITAL FEEDTHROUGH



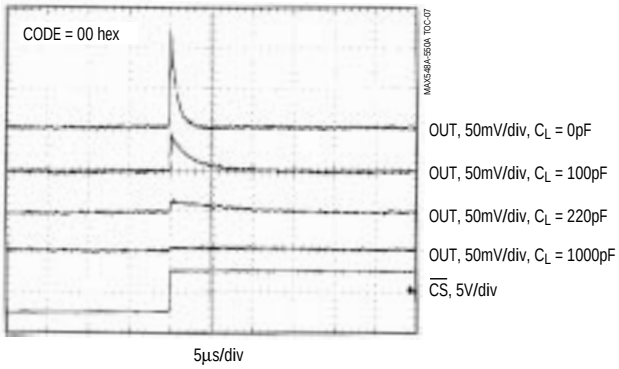
SETTLING TIME (FALLING)



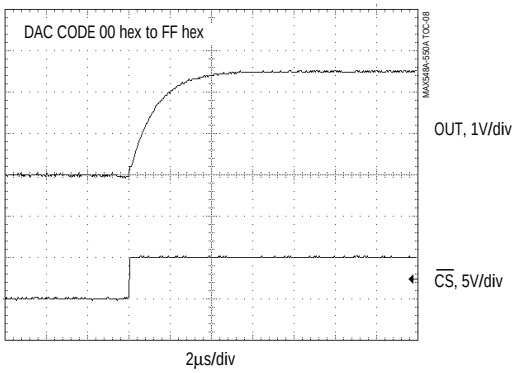
Typical Operating Characteristics (continued)

(V_{DD} = V_{REF} = 2.5V, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

OUTPUT GLITCH FILTERING



SETTLING TIME (RISING)



Pin Description

PIN			NAME	FUNCTION
MAX548A	MAX549A	MAX550A		
1	1	1	GND	Ground
2	2	—	OUTA	DAC A Output Voltage
—	—	2	OUT	DAC Output Voltage
3	3	3	$\overline{CS}$	Chip-Select Input. A logic low on $\overline{CS}$ enables serial data to be clocked into the input shift register. Programming commands are executed at $\overline{CS}$'s rising edge.
4	4	4	DIN	Serial-Data Input. Data is clocked into the 16-bit input shift register on SCLK's rising edge.
5	5	5	SCLK	Serial-Clock Input. Data is clocked in on SCLK's rising edge.
6	—	6	$\overline{LDAC}$	Load DAC Input. After $\overline{CS}$ goes high and if programmed by the control word, a falling edge on $\overline{LDAC}$ updates the DAC latch(es). Connect $\overline{LDAC}$ to V_{DD} if unused.
7	6	—	OUTB	DAC B Output Voltage
—	7	7	REF	External Reference Voltage Input for DAC(s)
8	8	8	V_{DD}	Positive Power Supply (+2.5V to +5.5V)

+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

Detailed Description

Analog Section

The MAX548A/MAX549A/MAX550A are 8-bit, voltage-output digital-to-analog converters (DACs). The MAX548A/MAX549A are dual DACs, and the MAX550A is a single DAC. Each DAC consists of an R-2R ladder network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage (Figure 1).

The DACs feature double-buffered inputs and unbuffered outputs. The MAX549A/MAX550A require an external reference. The MAX548A's reference inputs are internally connected to V_{DD}. The power-supply range is from +2.5V to +5.5V.

Reference Input

The voltage applied at REF (V_{DD} for the MAX548A) sets the full-scale output for all the DACs and may range from +2.5V to V_{DD}. The REF input resistance is code dependent, with the lowest value occurring with code 01010101 (55 hex). To minimize INL errors, the reference voltage source should have less than 3Ω output impedance.

DAC Output

The MAX548A/MAX549A/MAX550A contain DACs with unbuffered outputs; each output connects directly to an R-2R ladder. Typical output impedance is 33.3kΩ. This configuration minimizes power consumption and reduces offset errors. For highest accuracy, apply high resistive loads (1MΩ and up). Lower resistive loads can be driven, but output loading increases full-scale error. The magnitude of the expected error is the ratio of the DAC output resistance to the DC load resistance at the output.

Typically, an energy pulse is coupled into the DAC output on $\overline{CS}$'s rising edge. Since each DAC output is unbuffered, connecting a small capacitor (200pF to 1000pF) from the output to ground creates a lowpass filter that effectively suppresses the pulse for sensitive applications (see *Typical Operating Characteristics*).

Shutdown Mode

When the MAX548A/MAX549A/MAX550A are in shutdown mode, the R-2R ladder disconnects from the reference source. The MAX549A/MAX550A supply current does not change, but the REF input current decreases to less than 1µA. This allows the externally applied system reference to remain active with minimal power consumption. The MAX548A supply current also decreases to less than 1µA in shutdown mode. When the MAX548A/MAX549A/MAX550A exit shutdown mode, recovery time is equivalent to the DAC's settling time.

Serial Interface

The serial interface is SPI/QSPI and Microwire compatible. An active-low chip select ($\overline{CS}$) enables the input shift register to receive data from the serial input (DIN). Data is clocked into the shift register on the rising edge of the serial-clock signal (SCLK). The clock frequency can be as high as 10MHz.

Transmit data MSB first in one 16-bit word or two 8-bit bytes. The write cycle can be segmented to allow two 8-bit-wide transfers when $\overline{CS}$ remains low. After all 16 bits are clocked into the input shift register, a rising

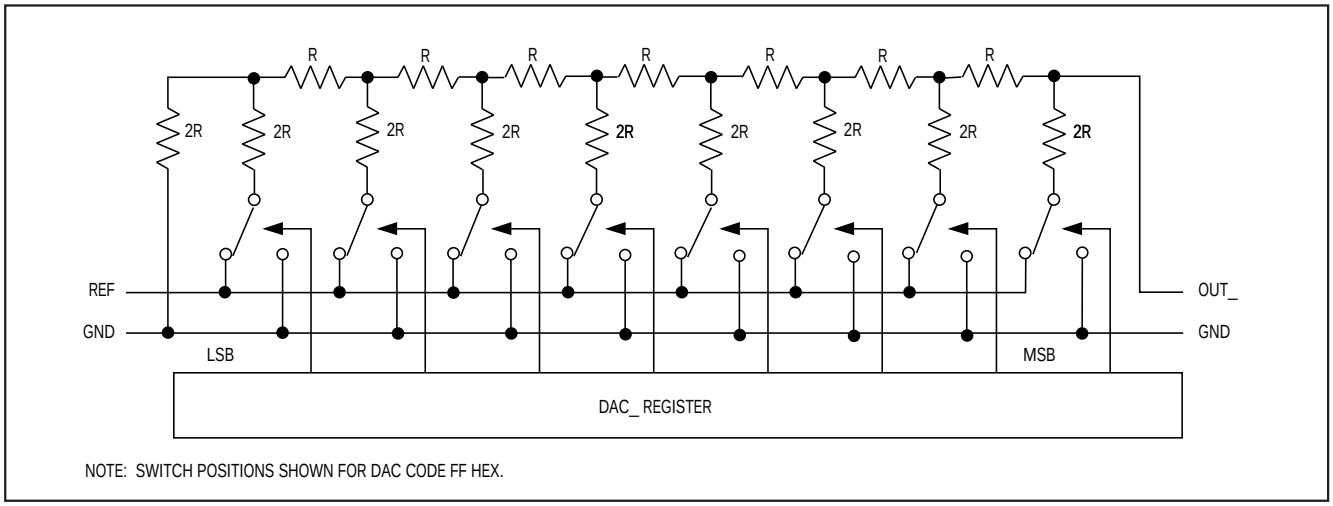


Figure 1. DAC Simplified Circuit Diagram

edge on $\overline{CS}$ programs the DAC. The input registers can be loaded independently or simultaneously without updating the DAC registers. This allows both DAC registers to be updated simultaneously with different digital values. The DAC outputs reflect the data stored in the DAC registers. $\overline{LDAC}$ can be used to asynchronously update the DAC registers independently of $\overline{CS}$ (MAX548A/MAX550A). With C1 set high, setting C0 in the control word forces the DAC register(s) to be updated on $\overline{LDAC}$'s falling edge, rather than $\overline{CS}$'s rising edge (Table 1).

Initialization

The MAX548A/MAX549A/MAX550A have an internal power-on reset. At power-up, all internal registers are reset to zero; therefore, an initialization write sequence is not necessary.

Serial-Input Data Format and Control Codes

The control byte determines which input registers/DAC registers are updated (Table 1). The DAC input registers are updated on the rising edge of $\overline{CS}$. The DAC registers can be updated on $\overline{CS}$'s rising edge or on $\overline{LDAC}$'s falling edge after $\overline{CS}$ goes high. Bit C0 of the control byte determines how the DAC registers are updated for the MAX548A/MAX550A. The MAX549A has no $\overline{LDAC}$ pin; the DAC registers are always updated on $\overline{CS}$'s rising edge (C0 in the control byte has no effect).

Tables 2, 3, and 4 list the serial-input command format for the MAX548A, MAX549A, and MAX550A, respectively. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The control byte is not decoded internally. Every control bit performs one

Table 1. Control-Byte/Input-Word Bit Definitions

	BIT NAME	STATE	OPERATION
CONTROL BYTE	UB1*	X	Unassigned Bit 1
	UB2	X	Unassigned Bit 2
	UB3	X	Unassigned Bit 3
	C2	0	Power-Up Mode
	C2	1	Power-Down Mode
	C1	0	DAC Register Load Operation Disabled
	C1	1	DAC Register Load Operation Enabled
	C0	0	DAC Register Updated on $\overline{CS}$'s Rising Edge
	C0	1	DAC Register Updated on $\overline{LDAC}$'s Falling Edge (MAX549A = Don't Care)
	A1	0	Do Not Address DAC B (MAX550A = Don't Care)
	A1	1	Address DAC B (MAX550A = Don't Care)
	A0	0	Do Not Address DAC A
	A0	1	Address DAC A
DATA BYTE	D7	—	DAC Data Bit 7 (MSB)
	D6	—	DAC Data Bit 6
	D5	—	DAC Data Bit 5
	D4	—	DAC Data Bit 4
	D3	—	DAC Data Bit 3
	D2	—	DAC Data Bit 2
	D1	—	DAC Data Bit 1
	D0**	—	DAC Data Bit 0 (LSB)

X = Don't care **Clocked in first* ***Clocked in last*

function. Data is clocked in starting with unassigned bit 1 (UB1), followed by the remaining control bits and the DAC data byte. The data byte's LSB (D0) is the last bit clocked into the input register (Figure 2).

Table 5 is an example of a 16-bit input word that performs the following functions:

- Loads 80 hex (128 decimal) into the DAC input register (DAC A for the MAX548A/MAX549A)
- Updates the DAC register(s) on $\overline{CS}$'s rising edge.

Table 6 shows how to calculate the output voltage based on the input code. Figure 3 gives detailed timing information.

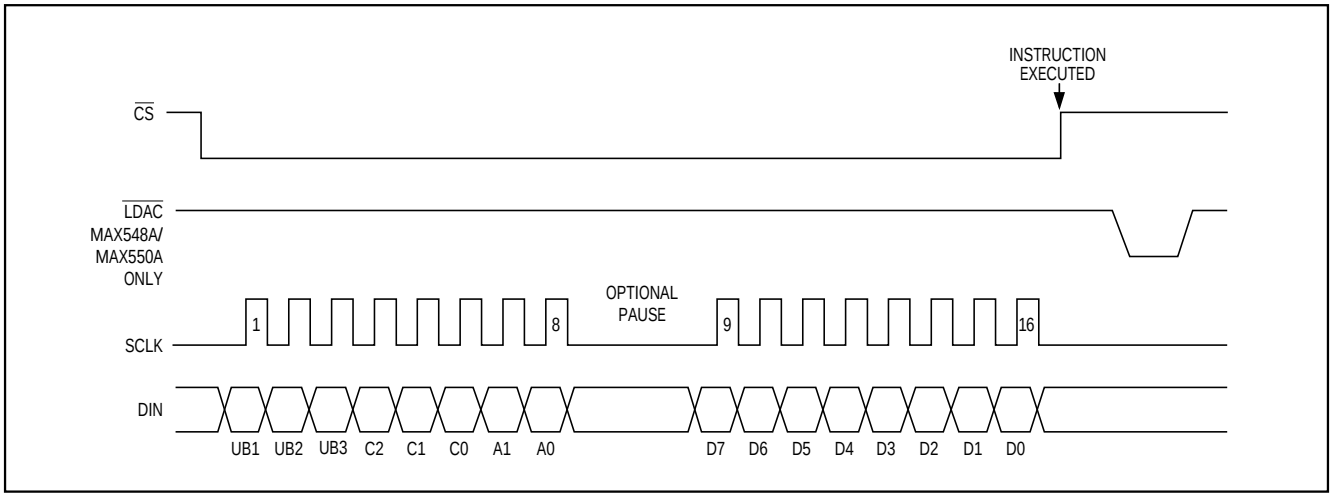


Figure 2. Serial-Interface Timing Diagram

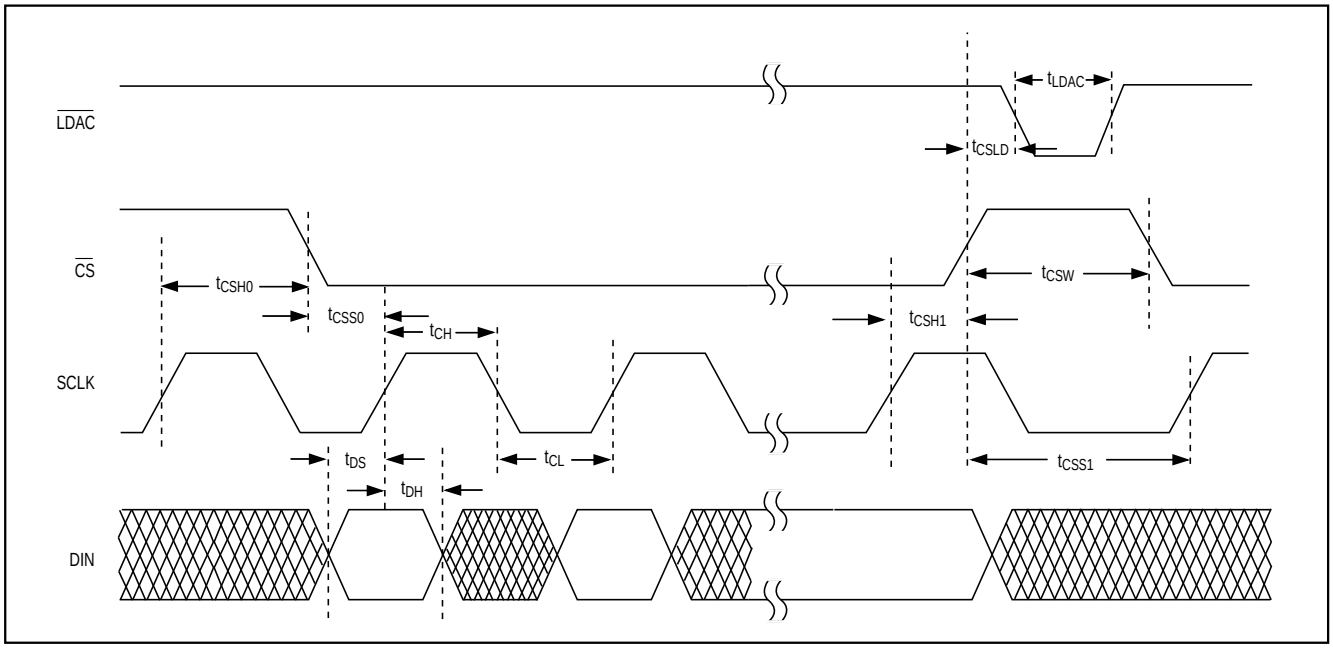


Figure 3. Detailed Serial-Interface Timing Diagram

Table 2. MAX548A Serial-Interface Programming Commands

CONTROL BYTE								DATA BYTE	LDAC	COMMAND (Commands executed on CS's rising edge)
Loaded First								Loaded Last		
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7.....D0	Pin 6	
UNASSIGNED COMMANDS										
X	X	X	0	0	X	0	0	XXXXXXXX	X	Unassigned command
X	X	X	1	X	X	0	0	XXXXXXXX	X	Unassigned operation
COMMANDS LOADING INPUT REGISTER(S) ONLY										
X	X	X	0	0	X	0	1	8-Bit DAC Data	X	Load DAC A input register. DAC B input register and both DAC registers unchanged.
X	X	X	0	0	X	1	0	8-Bit DAC Data	X	Load DAC B input register. DAC A input register and both DAC registers unchanged.
X	X	X	0	0	X	1	1	8-Bit DAC Data	X	Load both DAC input registers. Both DAC registers unchanged.
COMMANDS UPDATING DAC REGISTER(S)										
X	X	X	0	1	0	0	0	XXXXXXXX	X	Update both DAC registers with current contents of their input registers. Both input registers unchanged.
X	X	X	0	1	0	0	1	8-Bit DAC Data	X	Load DAC A input register and update both DAC registers. DAC B input register unchanged.
X	X	X	0	1	0	1	0	8-Bit DAC Data	X	Load DAC B input register and update both DAC registers. DAC A input register unchanged.
X	X	X	0	1	0	1	1	8-Bit DAC Data	X	Load both DAC input registers and update both DAC registers.
X	X	X	0	1	1	0	0	XXXXXXXX	0	Update both DAC registers with current contents of their input registers. Both input registers unchanged.
X	X	X	0	1	1	0	1	8-Bit DAC Data	0	Load DAC A input register and update both DAC registers. DAC B input register unchanged.
X	X	X	0	1	1	1	0	8-Bit DAC Data	0	Load DAC B input register and update both DAC registers. DAC A input register unchanged.
X	X	X	0	1	1	1	1	8-Bit DAC Data	0	Load both DAC input registers and update both DAC registers.
COMMANDS UTILIZING THE ASYNCHRONOUS LOAD FUNCTION										
X	X	X	0	1	1	0	0	XXXXXXXX	1	After CS's rising edge and on LDAC's falling edge, update both DAC registers with current contents of their input registers. Both input registers unchanged.
X	X	X	0	1	1	0	1	8-Bit DAC Data	1	Load DAC A input register. After CS's rising edge and on LDAC's falling edge, update both DAC registers.
X	X	X	0	1	1	1	0	8-Bit DAC Data	1	Load DAC B input register. After CS's rising edge and on LDAC's falling edge, update both DAC registers.
X	X	X	0	1	1	1	1	8-Bit DAC Data	1	Load both DAC input registers. After CS's rising edge and on LDAC's falling edge, update both DAC registers.

Table 2. MAX548A Serial-Interface Programming Commands (continued)

COMMANDS FOR POWERING DOWN

CONTROL BYTE Loaded First								DATA BYTE Loaded Last	LDAC	COMMAND (Commands executed on CS's rising edge)
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7.....D0	Pin 6	
COMMANDS POWERING DOWN AND LOADING INPUT REGISTER(S) ONLY										
X	X	X	1	0	X	0	1	8-Bit DAC Data	X	Load DAC A input register and power down DAC A. DAC B registers unchanged.
X	X	X	1	0	X	1	0	8-Bit DAC Data	X	Load DAC B input register and power down DAC B. DAC A registers unchanged.
X	X	X	1	0	X	1	1	8-Bit DAC Data	X	Load both DAC input registers and power down both DACs. Both DAC registers unchanged
COMMANDS POWERING DOWN AND UPDATING DAC REGISTER(S)										
X	X	X	1	1	0	0	1	8-Bit DAC Data	X	Load DAC A input register, power down DAC A, and update both DAC registers. DAC B input register unchanged.
X	X	X	1	1	0	1	0	8-Bit DAC Data	X	Load DAC B input register, power down DAC B, and update both DAC registers. DAC A input register unchanged.
X	X	X	1	1	0	1	1	8-Bit DAC Data	X	Load both DAC input registers, power down both DACs, and update both DAC registers.
X	X	X	1	1	1	0	1	8-Bit DAC Data	0	Load DAC A input register, power down DAC A, and update both DAC registers. DAC B input register unchanged.
X	X	X	1	1	1	1	0	8-Bit DAC Data	0	Load DAC B input register, power down DAC B, and update both DAC registers. DAC A input register unchanged.
X	X	X	1	1	1	1	1	8-Bit DAC Data	0	Load both DAC input registers and power down both DACs. Update both DAC registers.
COMMANDS POWERING DOWN AND UTILIZING THE ASYNCHRONOUS LOAD FUNCTION										
X	X	X	1	1	1	0	1	8-Bit DAC Data	1	Load DAC A input register and power down DAC A. While powered down, on LDAC's falling edge, update both DAC registers. DAC B input register unchanged.
X	X	X	1	1	1	1	0	8-Bit DAC Data	1	Load DAC B input register and power down DAC B. While powered down, on LDAC's falling edge, update both DAC registers. DAC A input register unchanged.
X	X	X	1	1	1	1	1	8-Bit DAC Data	1	Load both DAC input registers and power down both DACs. While powered down, on LDAC's falling edge, update both DAC registers.

X = Don't care

Table 3. MAX549A Serial-Interface Programming Commands

CONTROL BYTE								DATA BYTE	COMMAND (Commands executed on $\overline{CS}$'s rising edge)
Loaded First								Loaded Last	
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7.....D0	
UNASSIGNED COMMAND									
X	X	X	X	0	X	0	0	XXXXXXXX	Unassigned command
COMMANDS LOADING INPUT REGISTER(S) ONLY									
X	X	X	0	0	X	0	1	8-Bit DAC Data	Load DAC A input register. DAC registers unchanged.
X	X	X	0	0	X	1	0	8-Bit DAC Data	Load DAC B input register. DAC registers unchanged.
X	X	X	0	0	X	1	1	8-Bit DAC Data	Load both DAC input registers. DAC registers unchanged.
COMMANDS UPDATING DAC REGISTER(S)									
X	X	X	X	1	X	0	0	XXXXXXXX	Update both DAC registers with current contents of their input registers. Both input registers unchanged.
X	X	X	0	1	X	0	1	8-Bit DAC Data	Load DAC A input register and update both DAC registers. DAC B input register unchanged.
X	X	X	0	1	X	1	0	8-Bit DAC Data	Load DAC B input register and update both DAC registers. DAC A input register unchanged.
X	X	X	0	1	X	1	1	8-Bit DAC Data	Load both DAC input registers and update both DAC registers.
COMMANDS POWERING DOWN AND LOADING INPUT REGISTER(S) ONLY									
X	X	X	1	0	X	0	1	8-Bit DAC Data	Load DAC A input register and power down DAC A. DAC B input register and both DAC registers unchanged.
X	X	X	1	0	X	1	0	8-Bit DAC Data	Load DAC B input register and power down DAC B. DAC A input register and both DAC registers unchanged.
X	X	X	1	0	X	1	1	8-Bit DAC Data	Load both DAC input registers and power down both DACs. Both DAC registers unchanged.
COMMANDS POWERING DOWN AND UPDATING DAC REGISTER(S)									
X	X	X	1	1	X	0	1	8-Bit DAC Data	Load DAC A input register, power down DAC A, and update both DAC registers. DAC B input register unchanged.
X	X	X	1	1	X	1	0	8-Bit DAC Data	Load DAC B input register, power down DAC B, and update both DAC registers. DAC A input register unchanged.
X	X	X	1	1	X	1	1	8-Bit DAC Data	Load both DAC input registers, power down both DACs, and update both DAC registers.

X = Don't care

Table 4. MAX550A Serial-Interface Programming Commands

CONTROL BYTE								DATA BYTE	$\overline{LDAC}$	COMMAND (Commands executed on $\overline{CS}$'s rising edge)
Loaded First								Loaded Last		
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7.....D0	Pin 6	
UNASSIGNED COMMANDS										
X	X	X	0	0	X	X	0	XXXXXXXX	X	Unassigned command
X	X	X	1	X	X	X	0	XXXXXXXX	X	Unassigned operation
COMMANDS LOADING INPUT REGISTER ONLY										
X	X	X	0	0	X	X	1	8-Bit DAC Data	X	Load DAC input register. DAC register unchanged.
COMMANDS LOADING DAC REGISTER										
X	X	X	0	1	0	X	0	XXXXXXXX	X	Update DAC register with current contents of input register. Input register unchanged.
X	X	X	0	1	0	X	1	8-Bit DAC Data	X	Load DAC input register and update DAC register.
X	X	X	0	1	1	X	0	XXXXXXXX	0	Update DAC register with current contents of input register. Input register unchanged.
X	X	X	0	1	1	X	1	8-Bit DAC Data	0	Load DAC input register and update DAC register.
COMMANDS UTILIZING THE ASYNCHRONOUS LOAD FUNCTION										
X	X	X	0	1	1	X	0	XXXXXXXX	1	After $\overline{CS}$'s rising edge and on $\overline{LDAC}$'s falling edge, update DAC register with current contents of input register. Input register unchanged.
X	X	X	0	1	1	X	1	8-Bit DAC Data	1	Load DAC input register. After $\overline{CS}$'s rising edge and on $\overline{LDAC}$'s falling edge, update DAC register.
COMMAND POWERING DOWN AND LOADING INPUT REGISTER ONLY										
X	X	X	1	0	X	X	1	8-Bit DAC Data	X	Load DAC input register and power down DAC.
COMMANDS POWERING DOWN AND UPDATING DAC REGISTER										
X	X	X	1	1	0	X	1	8-Bit DAC Data	X	Load DAC input register, power down DAC, and update DAC register.
X	X	X	1	1	1	X	1	8-Bit DAC Data	0	Load DAC input register, power down DAC, and update DAC register.
COMMAND POWERING DOWN AND UTILIZING THE ASYNCHRONOUS LOAD FUNCTION										
X	X	X	1	1	1	X	1	8-Bit DAC Data	1	Load DAC input register and power down DAC. While powered down, on $\overline{LDAC}$'s falling edge, update DAC register.

X = Don't care

Table 5. Example Input Word

CONTROL BYTE								DATA BYTE							
Loaded First								Loaded Last							
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	1	0	0	1	1	0	0	0	0	0	0	0

X = Don't care

Microprocessor Interfacing

The MAX548A/MAX549A/MAX550A serial interface is SPI/QSPI and Microwire compatible. For SPI/QSPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the clock idle state to zero, and CPHA = 0 changes data at SCLK's falling edge. This is the Microwire default condition. If a serial port is not available on your microprocessor, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Operate the serial clock only when necessary, to minimize digital feedthrough at the DAC registers.

Applications Information

Power-Supply and Ground Considerations

Connect GND to the highest quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. The reference input can be used without bypassing. However, for optimum line/load-transient response and noise performance, bypass the reference input with a 0.1µF to 4.7µF capacitor to GND.

Careful PC board layout minimizes crosstalk in DAC registers, the reference, and the digital inputs. Separate analog traces by running ground traces between them. Make sure that high-frequency digital lines are not routed parallel to analog lines.

AC Considerations

Digital Feedthrough

High-speed data at any of the digital input pins can couple through a DAC's internal stray package capacitance and cause noise (digital feedthrough) at the DAC output, even though $\overline{LDAC}$ and/or $\overline{CS}$ are held high (see *Typical Operating Characteristics*). Test digital feedthrough by holding $\overline{LDAC}$ and/or $\overline{CS}$ high and toggling the digital inputs from all 1s to all 0s.

Analog Feedthrough

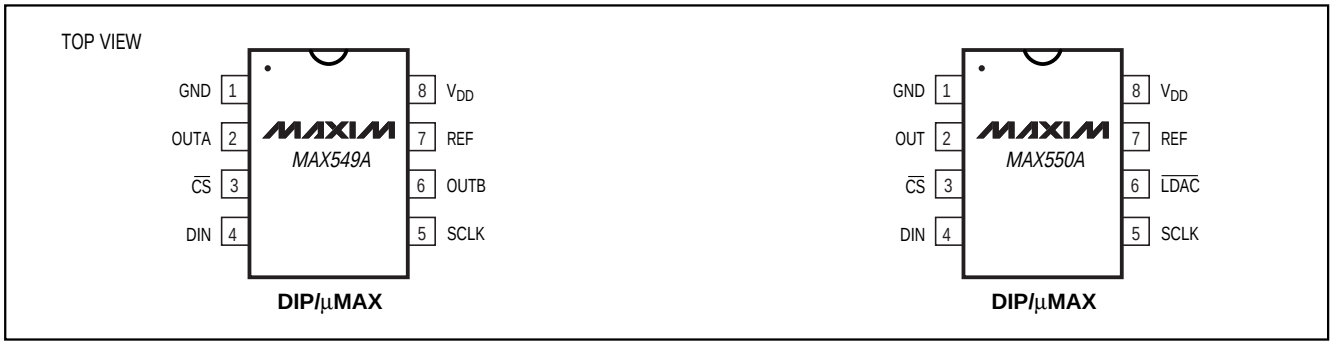
Due to internal stray capacitance, higher frequency analog input signals at REF can couple to the output, even when the input digital code is all 0s. This condition is shown in the MAX549A/MAX550A Reference AC Feedthrough vs. Frequency graph in the *Typical Operating Characteristics*. Test analog feedthrough by setting all DAC outputs to 0V and sweeping REF.

Table 6. Analog Output vs. Code

DAC CONTENTS								ANALOG OUTPUT (V)
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	$+V_{REF}(255 / 256)$
1	0	0	0	0	0	0	1	$+V_{REF}(129 / 256)$
1	0	0	0	0	0	0	0	$+V_{REF}(128 / 256) = +V_{REF} / 2$
0	1	1	1	1	1	1	1	$+V_{REF}(127 / 256)$
0	0	0	0	0	0	0	1	$+V_{REF}(1 / 256)$
0	0	0	0	0	0	0	0	0

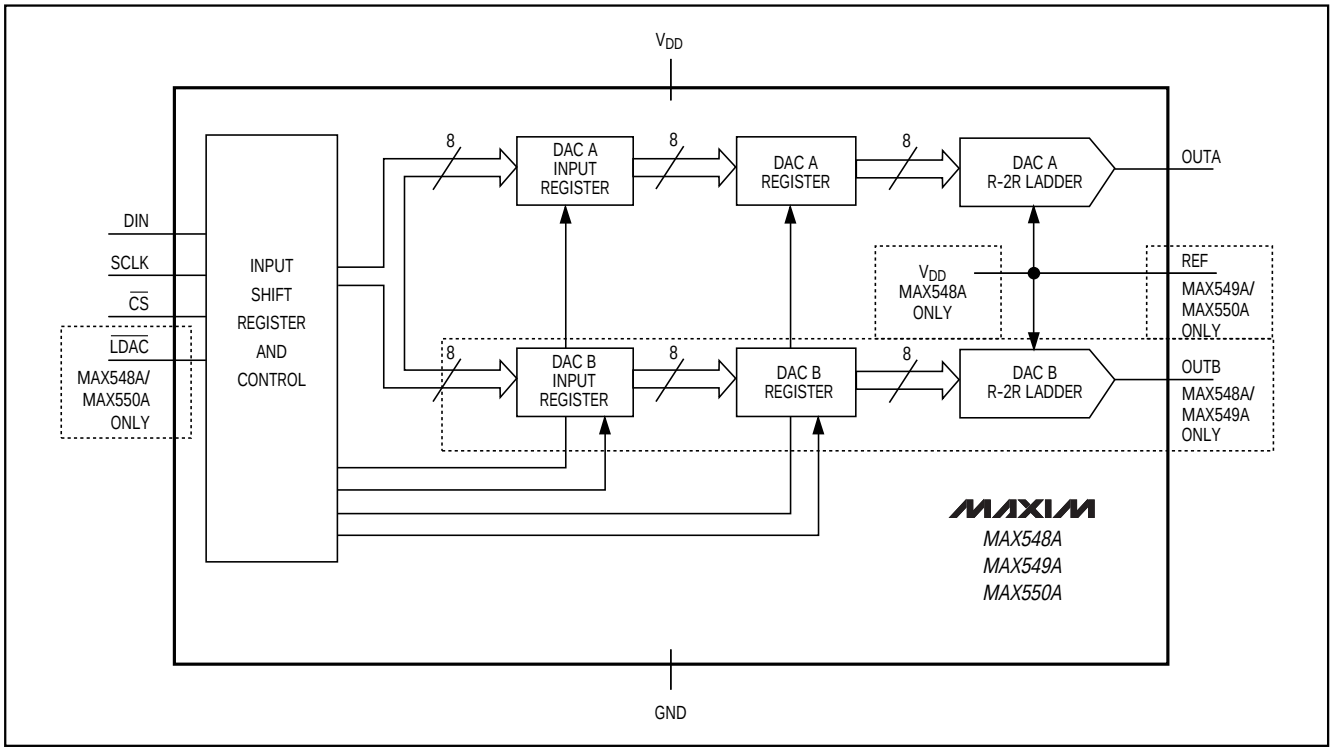
Note: 1LSB = $V_{REF} \times 2^{-8} = V_{REF}(1 / 256)$; ANALOG OUTPUT = $+V_{REF}(I / 256)$, where I = Integer Value of Digital Input.

Pin Configurations (continued)



+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

Functional Diagram



Ordering Information (continued)

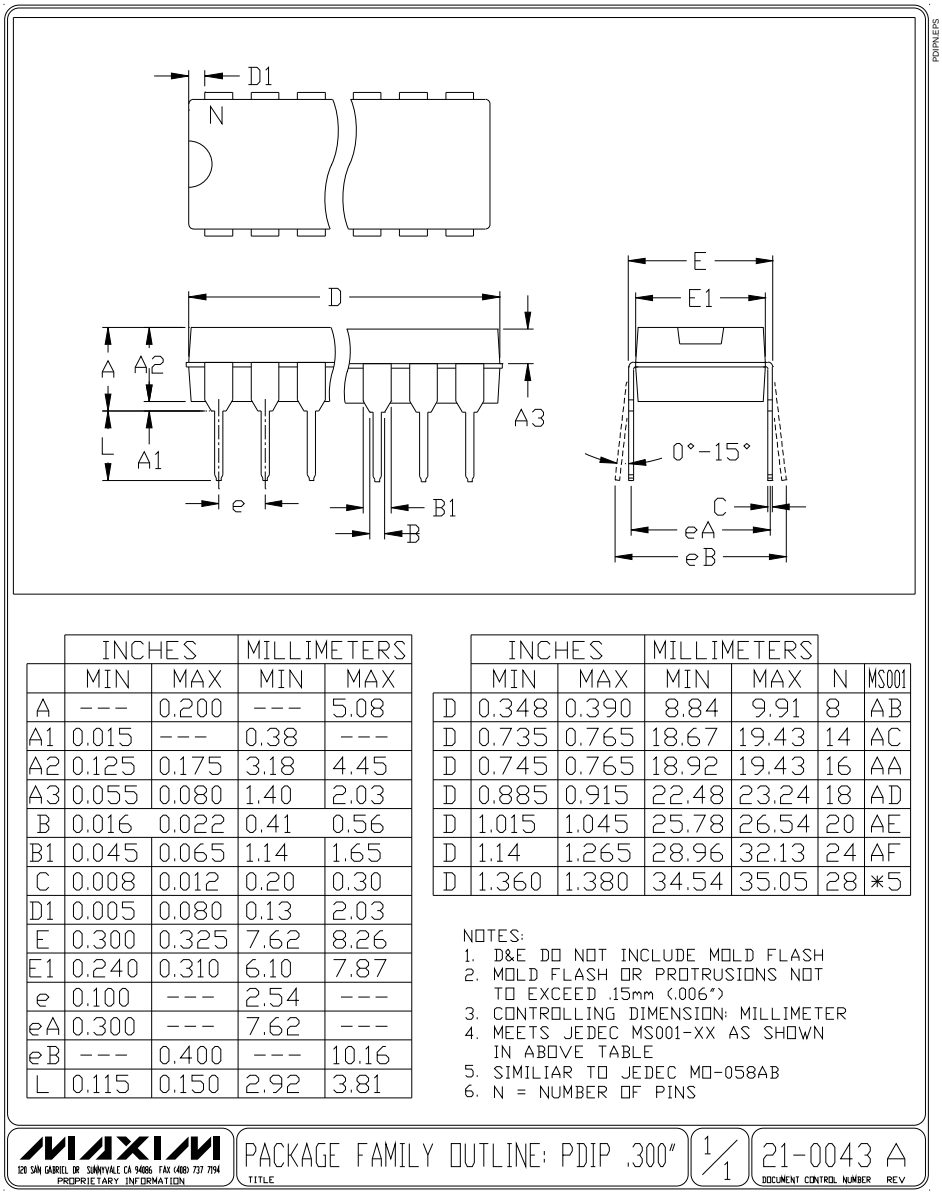
PART	TEMP. RANGE	PIN-PACKAGE
MAX549ACPA	0°C to +70°C	8 Plastic DIP
MAX549ACUA	0°C to +70°C	8 µMAX
MAX549AC/D	0°C to +70°C	Dice*
MAX549AEPA	-40°C to +85°C	8 Plastic DIP
MAX549AEUA	-40°C to +85°C	8 µMAX
MAX550ACPA	0°C to +70°C	8 Plastic DIP
MAX550ACUA	0°C to +70°C	8 µMAX
MAX550AC/D	0°C to +70°C	Dice*
MAX550AEPA	-40°C to +85°C	8 Plastic DIP
MAX550AEUA	-40°C to +85°C	8 µMAX

**Dice are specified at T_A = +25°C, DC parameters only.*

Chip Information

TRANSISTOR COUNT: 1562

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	∗5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: PDIP .300" TITLE

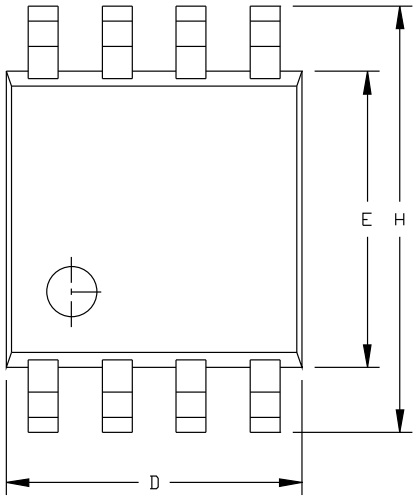
1/1

21-0043 A DOCUMENT CONTROL NUMBER REV.

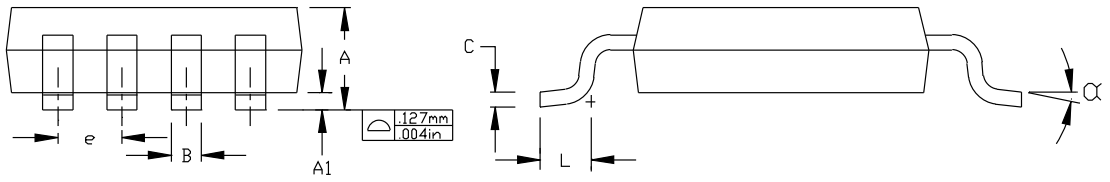
+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

Package Information (continued)

8LUMAXD.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION

TITLE:
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APPROVAL	DOCUMENT CONTROL NO.	REV	
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